RESEARCH ARTICLE

Current-Voltage Modeling of Transistors Based on Two-Dimensional Molybdenum Disulfide

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ABSTRACT This paper presents a compact model for the current-voltage (I–V) characteristics of field-effect transistors (FETs) based on two-dimensional molybdenum disulfide (MoS_2) channels. The proposed model is fully analytical, explicit, and physics-based, ensuring compatibility with circuit simulators while providing a comprehensive description of the device behavior. A key starting point is the derivation of a closed-form expression for the electrostatic potential, achieved through a novel solution of the Poisson equation, by means of a Taylor series expansion method using a sliding expansion point. Our modelling approach avoids iterative procedures and special functions commonly used in the literature and allows a more detailed and physically grounded analysis of device operation into a unified analytical framework, including effects often overlooked or fragmented in previous works, as the model incorporates critical non-idealities, such as short-channel effects, interface traps, carrier mobility degradation, and velocity saturation. The results are validated against experimental and simulation data from the literature, demonstrating excellent agreement. This work offers a robust and accessible modeling approach for 2D-FETs, enabling the design of high-performance integrated circuits and favoring the practical implementation of two-dimensional materials in nanoelectronics.

INDEX TERMS Nanotransistors, molybdenum disulfide, compact model, analytical model, two-dimensional materials.

I. INTRODUCTION

The aspects of band theory related to graphite have been known since 1947, through the pioneering work of Wallace [1]. The possibility of isolating a single layer of the material was also predicted by Boehm as early as 1962 [2]. Nevertheless, it was only in mid-2004 that Novoselov et al. experimentally demonstrated the material that became known as graphene [3]. From the outset, this material exhibited remarkable properties for microelectronics, such as extremely high carrier mobility, as well as a promise of improved electrostatic control due to the atomic thickness of the channel layer [4]. Thus, graphene was immediately seen as a strong candidate to replace silicon as the main material for high-performance transistors.

However, this groundbreaking material displays a zero bandgap, as demonstrated early on (see note 18 of [3]). The

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presence of a bandgap is crucial for digital electronics applications, as it strongly affects the ON-OFF current ratio. In any case, despite this shortcoming, the discovery of graphene stimulated research groups worldwide to seek other materials, beyond carbon, which could be isolated in one or a few layers [5]. What followed was the discovery and synthesis of a large variety of two-dimensional materials. Among these, molybdenum disulfide (MoS_2) stands apart as a material with a direct bandgap of 1.8 eV in its two-dimensional form. The first MoS_2-based transistor was demonstrated in 2011, registering an electron mobility of 200 $cm^2V^{-1}s^{-1}$ and an ON-OFF ratio of 10^8 [6]. Since then, MoS_2 has been one of the most investigated two-dimensional materials for nanoelectronics.

Regarding practical applications, a significant portion of early field-effect transistors based on two-dimensional materials (2D-FETs) were back-gate devices where the channel material was obtained by mechanical exfoliation, revealing the immature state of manufacturing

processes. More recently, significant advances in the growth techniques of these materials have been registered [7], and several integrated circuits based on 2D-FETs have been demonstrated [8]. Thus, it is expected that 2D-FETs with a structure similar to conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) will start to boost high-performance integrated circuits and other applications in the next decade [9], [10].

In this framework, developing compact models able to capture the unique characteristics of MoS_2-based transistors becomes crucial. Several analytical or semi-analytical treatments have been proposed in the past [11], [12], [13], [14], [15], [16], [17]. However, many of these formulations require iterative procedures to solve transcendental equations. Other approaches use special functions or require the numerical solution of integrals, which is inconvenient for application in integrated circuit simulators. Furthermore, few works incorporate important non-idealities to ensure the robustness and accuracy of the proposed models.

Our work aims to contribute to the compact modeling of transistors based on molybdenum disulfide by providing a fully analytical, explicit, and physics-based framework. A core novelty lies in the derivation of a novel closed-form solution of the Poisson equation in the channel, obtained by means of a Taylor series expansion method with a sliding reference point. From this electrostatic potential expression, our approach builds up a fully analytical and easy to understand model, providing excellent agreement with numerical solutions. Our model also unifies several critical non-idealities, such as interface traps, short-channel effects, mobility degradation, and velocity saturation, into a single analytical formulation. A more detailed treatment of the device physics is also provided, consolidating aspects that are often dispersed in previous works.

The text is structured as follows: Section II discusses the relevant properties of transition metal dichalcogenides, a family of materials that includes molybdenum disulfide. Section III presents the device and its electrostatic modeling, including the analysis of carrier concentration, conduction band diagram, and approximate analytical solutions for the Poisson equation considering long-channel and short-channel devices. Semiconductor defects such as interface traps and their influence on electrostatic control are also discussed. Section IV describes the current characteristics in the drift-diffusion regime, including the effects of carrier mobility degradation and carrier velocity saturation. In Section V, we validate the model considering experimental and simulation data available in the literature, covering all characteristics discussed earlier. Finally, we draw our conclusions in Section VI.

II. TRANSITION METAL DICHALCOGENIDES

Transition metal dichalcogenides (TMDs) are layered materials composed of an MX_2-type structure, where M is a transition metal atom, and X is a chalcogen atom (sulfur, selenium, or tellurium). These materials can also be isolated
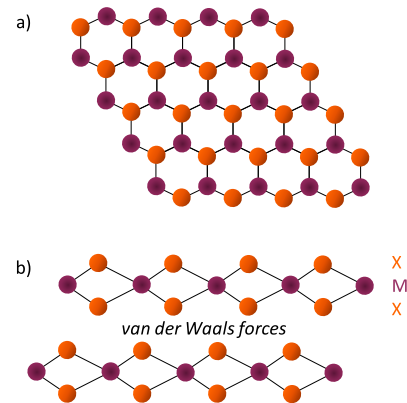

FIGURE 1. Typical crystal structure of two-dimensional transition metal dichalcogenides. a) Top view. b) Side view of two layers, where M is a transition metal atom, and X is a chalcogen atom. In the case of MoS_2, M is Mo (molybdenum), and X is S (sulfur).

in single or few-layers configurations. In a monolayer configuration, the atoms are arranged in a hexagonal crystal lattice through covalent bonds, while in the transverse plane, they form an X-M-X arrangement. As a result, the thickness of a single layer of these compounds is approximately 0.65 nm, with subsequent layers bonded by weak van der Waals forces. Fig. 1 illustrates the typical structure of a 2D TMD.

About a year after the discovery of graphene, Novoselov et al. [18] also demonstrated two-dimensional forms of molybdenum disulfide (MoS_2) and niobium diselenide ($NbSe_2$), with the former being a semiconductor and the latter a semimetal. However, the measured carrier mobilities were disappointedly low, between 0.5 and 3 $cm^2V^{-1}s^{-1}$, revealing that these early experiments were far from exploring the maximum potential of these materials.

Later, in 2010, it was experimentally demonstrated that two-dimensional MoS_2 is a direct bandgap semiconductor, unlike its bulk form [19]. Fabrication processes had evolved and, in the same year, Radisavljevic et al. [6] produced the first transistor based on a single layer of MoS_2. Using hafnium dioxide (HfO_2) as the gate oxide, they achieved an electron mobility of 200 $cm^2V^{-1}s^{-1}$, higher than achieved for ultrathin (i.e., less than 5 nm) silicon films. Since monolayer MoS_2 has a bandgap of 1.8 eV, the current ON-OFF ratio reaches levels as high as 10^8, which is quite suitable for digital microelectronics.

The two-dimensional form of MoS_2 has a direct bandgap at the K point of the first Brillouin zone. In addition, it presents a second valley in the conduction band, at a slightly higher energy than the primary valley. This second valley is located at the Q point, an intermediate to the K and Γ points, and computational calculations indicate that it significantly contributes to the total current of MoS_2-based 2D-FETs [20]. Fig. 2 shows the band structure of MoS_2 monolayers as obtained by *ab initio* methods [21], [22], highlighting the energy difference $\Delta\mathcal{E}_c$ between the two main valleys in the conduction band and the bandgap.
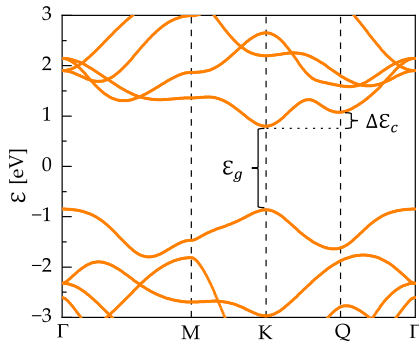
FIGURE 2. Band structure of monolayer MoS$_2$ calculated from *ab initio* methods. [21], [22]. The material presents two valleys in the conduction band, both significantly contributing to the carrier density. The primary valley is at the K point (direct bandgap, $\mathcal{E}_g$), while the secondary valley is at the Q point within the first Brillouin zone. The energy difference between both is denoted as $\Delta\mathcal{E}_c$. In our model, we assume $\mathcal{E}_g = 1.8$ eV and $\Delta\mathcal{E}_c = 0.1$ eV. Also, both valleys present near-parabolical shapes, so the effective mass approximation is adopted with $m_K^* = 0.457m_0$ and $m_Q^* = 0.543m_0$.

These features are considered when calculating the density of states. Assuming a parabolic approximation for the dispersion relation, the density of states is given by [12]

$$g_{2D}(\mathcal{E}) = \sum_\ell \left(\frac{g_s g_\ell m_\ell^*}{2\pi\hbar^2} \right) \quad \ell = 1, 2, \ldots \quad (1)$$

where $\hbar$ is the reduced Planck's constant, $g_s = 2$ is the degeneracy factor due to spin, g_ℓ and m_ℓ^* are, respectively, the degeneracy factor and the effective mass corresponding to the ℓth valley considered. Given the crystal lattice structure of MoS$_2$, we have $g_K = 2$ and $g_Q = 6$, which also increases the contribution of the secondary valley to the current composition.

III. ELECTROSTATIC MODELING

The initial stage of our modeling consists of establishing a charge-control relation between the carrier concentration in the channel and the voltage applied to the gate terminal, in the absence of current flow. In this context, $V_{ds} = 0$, and the potential of the Fermi level along the channel is fixed as an invariant reference value expressed as V.

The device to be modeled is presented in Fig. 3. From bottom up, it comprises a substrate, usually made of highly doped silicon, and an insulator, typically thermally-grown silicon dioxide. The two-dimensional semiconductor (MoS$_2$) channel is placed on top of the insulator, with the gate oxide located above it. As in state-of-the-art transistors, this gate oxide can be made of silicon dioxide or some other insulating material with a high dielectric constant. Finally, the source, drain, and gate contacts are made of metals.

Since the first demonstration, transistors fabricated with MoS$_2$ channels have been known to be naturally n-type, favoring electron conduction, regardless of the number of layers or the type of metal used in the contacts [6]. Recently, this behavior has been attributed to unintentional carbon doping
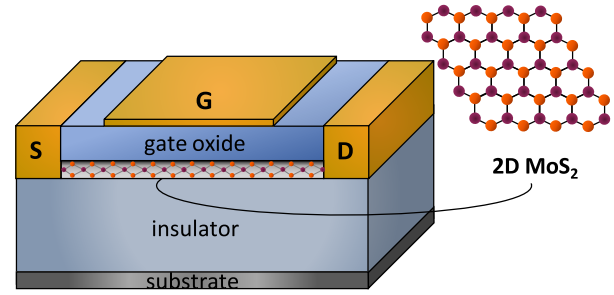
FIGURE 3. Three-dimensional schematic of a 2D-FET with a MoS$_2$ channel.

of the MoS$_2$ samples [23]. Therefore, in this work, an n-type device is assumed, with a donor density, N_D, given in cm^{-2}.

A. CARRIER CONCENTRATION

The electron concentration in the two-dimensional channel is given by:

$$n_{2D} = \int_{\mathcal{E}_c}^{\infty} g_{2D}(\mathcal{E}) f(\mathcal{E} - \mathcal{E}_F) d\mathcal{E}, \quad (2)$$

In the above equation, $f(\mathcal{E} - \mathcal{E}_F)$ is the Fermi-Dirac distribution, where $\mathcal{E}_F$ the Fermi level energy. Regarding the integration limits, the conduction band of the MoS$_2$ channel consists of discrete levels. However, carriers are confined within a thickness of ~ 1 nm and these levels are widely spaced, in such way that only the first energy level needs to be taken into account, because it will be the only significantly occupied by electronic carriers. This first energy sub-band corresponds to the bottom of the conduction band for the MoS$_2$ channel and will be denoted as $\mathcal{E}_c$ in the remainder of this paper.

In order to calculate the carrier concentration, we assume $\mathcal{E}_c = -q\varphi$, where φ is the channel electrostatic potential energy. Also, $\mathcal{E}_F = -qV$, as mentioned earlier. Thus, assuming the Boltzmann approximation to solve eq. (2), we have:

$$n_{2D} = N_{\text{DoS}} \exp\left(\frac{\varphi - V}{\phi_T} \right), \quad (3)$$

where

$$N_{\text{DoS}} = \frac{g_K m_K^* k_B T}{\pi\hbar^2} + \frac{g_Q m_Q^* k_B T}{\pi\hbar^2} \exp\left(-\frac{\Delta\mathcal{E}_c}{k_B T} \right), \quad (4)$$

and $\phi_T = k_B T/q$ is the thermal voltage, where k_B is the Boltzmann constant, and T is temperature.

The doping level in MoS$_2$ transistors is generally quite low, on account of the difficulties of intentional doping in two-dimensional semiconductors. Also, as Cao et al. [12] pointed out, the high density of states in MoS$_2$ makes the channel potential less dependent on the gate voltage. In other words, it prevents the Fermi level from deeply entering the conduction band, which could lead the semiconductor to a degenerate state. All factors considered, the Boltzmann approximation provides an accurate description for the carrier concentration.
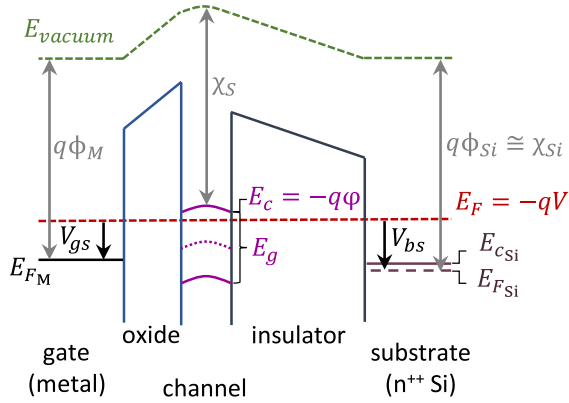
FIGURE 4. Conduction band diagram of a 2D-FET, where a highly doped n-type silicon substrate is assumed. The device is biased with $V_{gs} > V_{FB}$, as evidenced by the bending of the conduction band in the semiconductor channel region.

FIGURE 5. Schematic for electrostatic analysis of a 2D-FET. A region of infinitesimal width, where Gauss law is applied, it is highlighted in the channel. The gate oxide, semiconductor, and insulator have thicknesses t and permittivities ε labeled with their respective subscripts.
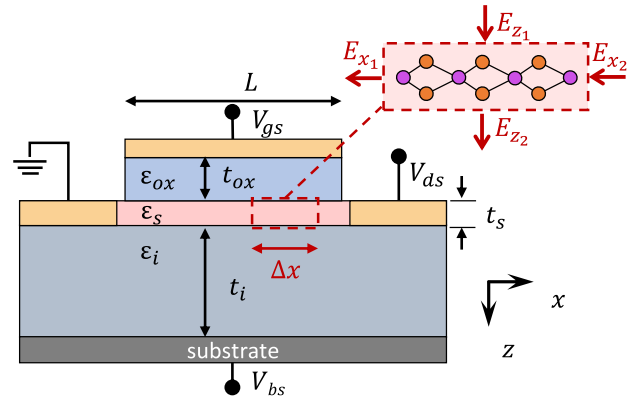
B. CONDUCTION BAND PROFILE

Fig. 4 shows the conduction band energy profile for a 2D-FET. From top to bottom (i.e., left to right in the figure), we first have the metal gate contact, characterized by the work function ϕ_M [eV]. The applied gate voltage (V_{gs}) shifts the Fermi level at the metal contact with respect to the semiconductor. As a consequence, there is a potential drop across the gate oxide (φ_{ox}) and the semiconductor channel, which is characterized by an electron affinity χ_S [eV] and bandgap energy $\mathcal{E}_g$. The work function of the two-dimensional semiconductor can be calculated by:

$$\phi_S = \frac{\chi_S}{q} + \frac{\mathcal{E}_g}{2q} - \phi_T \ln\left(\frac{n_{2D}}{n_i}\right), \quad (5)$$

where n_i is the intrinsic electron concentration. On account of the immature fabrication processes, the doping densities are rather low in these devices, in such way that $n_{2D} \cong n_i$ at flatband condition, thereby placing the Fermi level in the semiconductor near the mid-gap. Accordingly, even if a slightly higher intentional doping level is assumed in the source and drain regions, these 2D-FETs will be accumulation-type transistors. Specifically, they operate in a carrier depletion regime in the off-state and a carrier accumulation regime in the on-state [24], in a very similar way to junctionless transistors [25]. The flatband voltage is defined from the diagram simply as $V_{FB} = \phi_{MS}$.

Moving forward, we reach the substrate insulator. It should be stressed that the diagram in Fig. 4 is not on scale. While the 2D channel typically has a thickness of ∼1 nm, the insulator thickness is on the order of hundreds of nanometers. Finally, the substrate is usually made of highly doped silicon. In this case, n-type doping is assumed so that the work function of silicon is approximately χ_{Si}/q. A fixed voltage V_{bs} can be applied to the substrate to shift the Fermi level and, consequently, alter the electrostatic characteristics of the transistor. For instance, this technique is often used in MOSFETs to adjust the threshold voltage. For 2D-FETs, it can also be used to provide the so-called electrostatic doping since the substrate extends to the region of the contacts.

C. POISSON EQUATION

To establish the charge control relation, it is first necessary to write the Poisson equation governing this device. Fig. 5 shows the scheme proposed initially by Cao et al. [12] to analyze the electric field $\bar{E}$ in an infinitesimal section of the channel (Δx), by using Gauss law.

In this two-dimensional representation, the gate voltage is applied along the z-axis, and the current flow occurs in the x-direction. Consequently, there is no potential difference applied along the y-axis, parallel to the cross-section of the device. Given that there is no electric field applied along the y-direction and that the channel is formed by just a few layers of MoS$_2$, it is fair to assume that $\varphi(x, y, z) \approx \varphi(x)$ in the channel.

The Poisson equation for this device is then written as

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x)}{\lambda^2} + \frac{C_{ox}\left(V_{gs} - V_t\right)}{\varepsilon_s t_s}$$
$$= \frac{qN_{DoS}}{\varepsilon_s t_s} \exp\left[\frac{\varphi(x) - V(x)}{\phi_T}\right], \quad (6)$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance, and λ is the characteristic length of the 2D-FET, given by

$$\lambda = \sqrt{\frac{\varepsilon_s t_s t_{ox} t_i}{\varepsilon_{ox} t_i + \varepsilon_i t_{ox}}}, \quad (7)$$

and V_t is the threshold voltage, given as

$$V_t = V_{FB} + \frac{C_i\left(V_{bs} - V_i\right) - qN_D}{C_{ox}}, \quad (8)$$

where the term V_i corresponds to the difference between the work functions of the semiconductor and the substrate, and $C_i = \varepsilon_i/t_i$ is the capacitance of the insulator.

Once the Poisson equation governing the electrostatic behavior of the device is established, the next step towards a full description of the I–V characteristics is to obtain an

analytical solution for the electrostatic potential along the channel. The analysis is carried out considering two distinct cases. In the first, the device is long enough to allow the gradual channel approximation. In the second case, we account for short-channel effects, which may lead to degraded electrostatic control.

D. ANALYTICAL SOLUTION FOR LONG-CHANNEL DEVICES

Considering the gradual channel approximation, one can take $d^2\varphi(x)/dx^2 = 0$ in eq. (6). Thus, rearranging the terms, we have an implicit relationship between the electrostatic potential in the channel and the applied voltage at the gate contact:

$$(C_{ox} + C_i)\varphi(x) + qN_{DoS}\exp\left[\frac{\varphi(x) - V(x)}{\phi_T}\right]$$
$$= C_{ox}(V_{gs} - V_t). \tag{9}$$

Eq. 9 is a transcendental equation for $\varphi(x)$, so it is necessary to introduce some analytical approximations to make it an explicit relation regarding the dependence of the channel potential with respect to the bias voltages. To do so, a useful first step is to know the asymptotic behavior of $\varphi(x)$ for $V_{gs} \ll V_t$ and $V_{gs} \gg V_t$.

In eq. (9), the first term on the left-hand side relates to the capacitive control of the channel by the gate contact, while the second term corresponds to the accumulated charge density. Without loss of generality, we can set $V(x) = 0$ to easy the analysis. For $V_{gs} \ll V_t$, the transistor operates in the subthreshold region, and $n_s(x) \cong 0$. Therefore, we have:

$$\varphi(x) \cong \frac{C_{ox}}{C_{ox} + C_i}(V_{gs} - V_t), \tag{10}$$

that is, the electrostatic potential of the channel varies linearly with the applied gate voltage.

As the gate voltage approaches the threshold value, the accumulated charge density grows exponentially. In the limit, when $V_{gs} \gg V_t$, we have:

$$\varphi(x) \cong \phi_T \ln\left[\frac{C_{ox}}{qN_{DoS}}(V_{gs} - V_t)\right], \tag{11}$$

i.e., the potential grows less sharply with the applied gate voltage. Fig. 6 illustrates these asymptotic behaviors, when compared to the exact solution of eq. (9).

In order to solve the transcendental equations, such as eq. (9), and obtain an explicit analytical expression for the channel potential $\varphi(x)$ as a function of the bias voltages, a usually employed technique is to expand the exponential term in eq. (9) into a Taylor series. Taking an arbitrary point Φ as a reference, one gets:

$$\exp\left(\frac{\varphi}{\phi_T}\right) \cong \exp\left(\frac{\Phi}{\phi_T}\right)\sum_{j=0}^{n}\frac{1}{j!}\left(\frac{\varphi - \Phi}{\phi_T}\right)^j. \tag{12}$$

The accuracy of this expansion within a given interval will primarily depend on two factors: the number of terms (n) retained in the approximation and the choice of the expansion
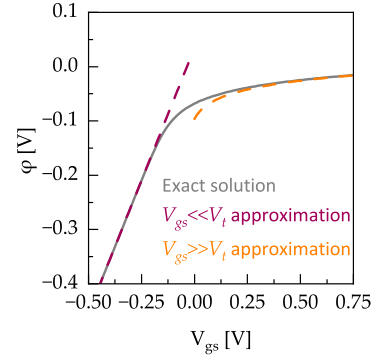
FIGURE 6. Asymptotic behavior of the electrostatic potential below and above threshold, respectively. Simulation parameters: monolayer MoS$_2$ channel with $N_D = 3.5 \times 10^{11}$ cm^{-2}, SiO$_2$ gate oxide and insulator with $t_{ox} = 5$ nm and $t_i = 90$ nm, Al gate, and n^{++} Si substrate.

point Φ. Since the expansion results in a polynomial function, retaining n terms implies finding the roots of an nth-degree polynomial, which can be quite difficult for $n > 2$.

As an alternative, we have developed a new approach to solve transcendental equations, which we applied in the context of the compact modeling of ballistic 2D-FETs [26], [27], [28]. In this approach, we still use a Taylor series expansion, but employ a sliding expansion point Φ, which is determined by a mapping function, obtained by inspecting the behavior of φ within a given interval.

Following this principle, a typical mapping function for $\Phi(V_{gs})$ is

$$\Phi = 2\phi_T + \frac{2[\alpha(V_0 - V_t) - 2\phi_T]}{1 + \exp[d(V_{gs} - V_0)]}, \tag{13}$$

where V_0 and d are fixed parameters, and $\alpha = C_{ox}/(C_{ox} + C_i)$. The parameter V_0 is dominant for $V_{gs} \ll V_t$, so it can be chosen, for instance, as $V_0 = V_t - 1.65$. Meanwhile, the parameter d determines the smoothness of the transition in the asymptotic behavior of φ as $V_{gs} \approx V_t$. In this case, choosing $d = 2$ results in a good match.

Moving forward with the analysis of eq. (9), our study indicated that, with the new approach, retaining just the first two terms of the expansion, eq. (12), is sufficient to achieve the desired accuracy. Thus, a fully explicit and analytical expression for $\varphi(V_{gs})$ is written as

$$\varphi = \frac{qN_{DoS}(\Phi - \phi_T)\exp[\Phi/\phi_T] + \phi_T C_{ox}(V_{gs} - V_t)}{qN_{DoS}\exp[\Phi/\phi_T] + \phi_T(C_{ox} + C_i)}. \tag{14}$$

Fig. 7-a illustrates a typical example, providing excellent matching between the exact behavior and the proposed approximation, retaining only the first two terms in eq. (12). Even when only the first term is used, the relative error remains below 8.43% near the threshold voltage, already demonstrating fair accuracy. Otherwise, the accuracy can be further improved by keeping one more term ($n = 2$) in eq. (12) and finding the roots of a second-degree polynomial.
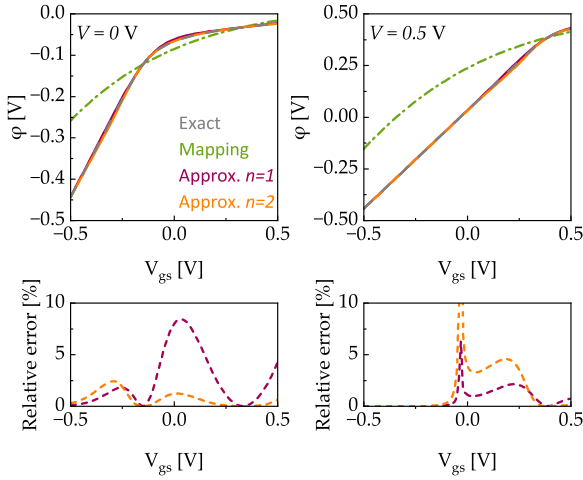
FIGURE 7. Comparison between the exact solution and the approximate expression for the electrostatic potential considering $n = 1$ and $n = 2$. Specifications: monolayer MoS$_2$ channel with $N_D = 3.5 \times 10^{12}$ cm^{-2}, HfO$_2$ gate oxide (t_{ox} =2 nm), SiO$_2$ insulator (t_i = 90 nm), Cr gate, and n^{++} Si substrate. The respective mapping functions $\Phi(V_{gs})$ used for the calculations are also shown. a) $V = 0$ V. b) $V = 0.5$ V.

In this case, for $n = 2$, the maximum relative error is only 2.41%.

In the more general, case where $V(x) \neq 0$, the same method can be applied. by considering the expansion variable as the difference $\varphi(x) - V(x)$ and carrying the same analysis. Fig. 7-b depicts an analysis similar to the one discussed earlier, but now considering $V = 0.5$ V. In this case, the relative error is kept below 5% for most of the interval.

In summary, a fully analytical and explicit expression for $\varphi(V_{gs}, V_{ds})$ was obtained for long-channel transistors. As it will be shown later, from this analysis, it is possible to calculate the carrier density in the channel $n_{2D}(V_{gs}, V_{ds})$ and obtain an expression for the current characteristics.

E. ANALYTICAL SOLUTION FOR SHORT-CHANNEL DEVICES

The gradual channel approximation is inappropriate for the modeling of very short gate-length transistors, which, in principle, require the solution of the Poisson equation in its full form. However, within the scope of electrostatics analysis for compact modeling, short-channel effects are mostly important in the subthreshold region, where they degrade the transistor behavior as well as alter the value of threshold voltage itself. Thus, it is possible to restrict the analysis of short-channel effects to a solution of the Poisson equation under total carrier depletion, i.e.,

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x)}{\lambda^2} + \frac{C_{ox}(V_{gs} - V_t)}{\mathcal{E}_s t_s} = 0. \quad (15)$$

The third term of the above equation corresponds to the channel potential under subthreshold condition, as written for long-channel devices, eq. (9). Replacing this term into

eq. (15), we have a differential equation of the form:

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x) - \varphi_\ell}{\lambda^2} = 0, \quad (16)$$

where

$$\varphi_\ell = \frac{C_{ox}}{C_{ox} + C_i}(V_{gs} - V_{t\ell}). \quad (17)$$

The solution to equation (16), considering the boundary conditions, is:

$$\varphi(x) = \varphi_\ell + \frac{(V_{ds} - \varphi_\ell)\sinh\left(\frac{x}{\lambda}\right) - \varphi_\ell \sinh\left(\frac{L-x}{\lambda}\right)}{\sinh(L/\lambda)}. \quad (18)$$

Hence, expression (18) describes the electrostatic potential for short-channel devices in the subthreshold region. Fig. 8-a compares the minimum value from eq. (9) to that of eq. (18) for a 2D-FET with $L = 12$ nm, revealing an important degradation of the subthreshold characteristics.

For compact modeling purposes, it should be noted that an expression for the current will depend on the integration of the term $\exp\left[-\varphi(x)/\phi_T\right]$ over x [12]. Inspection of eq. (18) reveals that the integration must be carried out numerically. Therefore, it is imperative to obtain an approximation to allow an analytical treatment.

Keeping in mind that the subthreshold current characteristics are essentially dictated by the top of the potential energy barrier, a simple approach is to expand eq. (18) into a Taylor series around the point along the channel where the electrostatic potential is minimum, as it has been done for conventional MOSFETs [29]. Thus, the first step is to determine the expansion point, by taking the derivative of eq. (18) with respect to x and setting it to zero. The result is

$$x_{\min} = \frac{L}{2} - \frac{\lambda}{2}\ln\left[\frac{(V_{ds} - \varphi_\ell) + \varphi_\ell \exp\left(-\frac{L}{\lambda}\right)}{-\varphi_\ell - (V_{ds} - \varphi_\ell)\exp\left(-\frac{L}{\lambda}\right)}\right]. \quad (19)$$

Then, we retain only the first two non-zero terms of the series, to write:

$$\varphi_{\text{approx}}(x) \approx A_2(x - x_{\min})^2 + A_0, \quad (20)$$

where $A_i = \frac{d^i\varphi}{dx^i}(x = x_{\min})$.

For devices with very short channels ($L < 30$ nm), the lateral electric field in the oxide (i.e., the electric field component in the direction along the channel) also needs to be taken into account [12], [13]. In [13], the authors suggest a linear dependence relating the lateral electric field in the two-dimensional semiconductor $E_x(x)$ to the lateral electric field in the oxide $E_{ox}(x)$, i.e., $E_x(x) = \alpha E_{ox}(x)$, where α is an empirical value obtained from TCAD simulations (Silvaco ATLAS). This approximation allows one to rewrite the characteristic length of the 2D-FET, eq. (7), to include the effect of the lateral electric field of the oxide, as:

$$\lambda = \sqrt{\frac{\mathcal{E}_s t_s t_{ox} t_i}{\mathcal{E}_{ox} t_i + \mathcal{E}_i t_{ox}} + \frac{1}{\alpha}\left(\frac{\mathcal{E}_{ox} t_{ox}^2 t_i}{\mathcal{E}_{ox} t_i + \mathcal{E}_i t_{ox}}\right)}. \quad (21)$$

Fig 8-b depicts the minimum value of the electrostatic potential when a high-κ dielectric oxide (HfO$_2$) is considered.
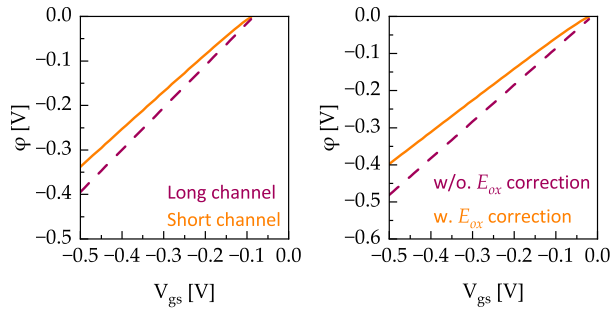
FIGURE 8. Value of the minimum electrostatic potential considering short-channel effects. Parameters: monolayer MoS$_2$ channel with $N_D = 3.5 \times 10^{11}$ cm^{-2} and $L = 12$ nm, $V_{ds} = 0.5$ V, SiO$_2$ insulator (t_i = 90 nm) nm), Al gate, and n^{++} Si substrate. a) Gate oxide: SiO$_2$ (t_{ox} =5 nm). b) Gate oxide: HfO$_2$ (t_{ox} =5 nm). A factor $\alpha = 0.96\varepsilon_{ox}/\varepsilon_{SiO_2}$ was used, as done in [13].

FIGURE 9. Analysis of the model to include interface trap effects. Parameters: monolayer MoS$_2$ channel, Al$_2$O$_3$ gate oxide, SiO$_2$ insulator, Al gate, n^{++} Si substrate, $D_{it0} = 4.15 \times 10^{12}$ eV^{-1}cm^{-2}, $D_{it1} = 2.9 \times 10^{13}$ eV^{-1}cm^{-2} and $\mathcal{E}_\sigma = 0.07$ eV. a) Validation of the expression for the interface states distribution compared against experimental data [30]. b) Comparison between the C_Q and C_{it} for $V_{gs} < V_t$.

While the oxide thickness and the other parameters are kept unchanged, it was necessary to account for the lateral electric field correction, in order to achieve a subthreshold behavior similar to the one registered with SiO$_2$ (Fig. 8-a). This indicates that the parasitic effect of the lateral field in the oxide is quite relevant for short-channel 2D-FETs, and its impact needs to be included for an accurate compact model.
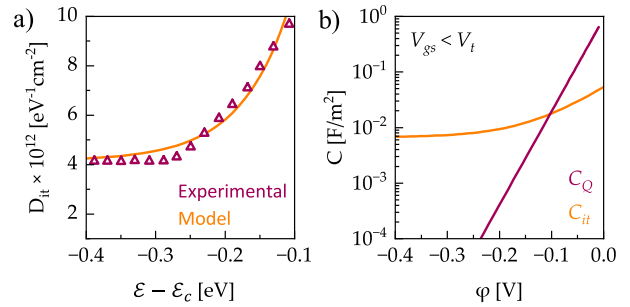
F. INTERFACE TRAPS

Although two-dimensional materials do not form chemical bonds out of the plane, interface traps can be induced by underlying materials or defects and impurities in the crystalline lattice. The problem is made worse by the present fabrication techniques for 2D-FETs, which lag far behind the state-of-the-art for silicon devices. As a consequence, today, even the best 2D-FETs will inevitably be affected by interface traps, especially considering the low density of states of these materials when compared to three-dimensional semiconductors.

In molybdenum disulfide, interface traps can arise from three main sources [30]: i) defects in the crystalline lattice, such as sulfur (S) vacancies; ii) defects in the substrate insulator or gate oxide; and iii) externally induced lattice strain.

Sulfur vacancies are relatively common when the material is grown by CVD and result in localized states near the middle of the bandgap ($\mathcal{E}_{it} = \mathcal{E}_c - 0.46$ eV) [31]. Although the interface state density is typically high (10^{12} to 10^{13} cm^{-2}), the electrostatic control is not significantly altered. On the other hand, these point defects result in unintentional doping and reduce carrier mobility by increasing Coulomb scattering.

The substrate insulator often presents very few defects, as it typically consists of thermally oxidized silicon, a very mature technique. As such, the interface state density is on the order of 10^{11} cm^{-2} or lower. In contrast, depositing a gate oxide with a high dielectric constant onto a two-dimensional material is a challenge and often results in various defects. For instance, ultraviolet (UV) and ozone treatments are often used for surface preparation, and intermediate layers are frequently

employed to improve the interface quality between the oxide and the semiconductor. Also, the use of the atomic layer deposition (ALD) technique, at a relatively low temperature (200 °C), for oxide deposition, also introduces traps into the material [32].

Finally, as pointed out in various works by Fang et al. [30], [33], [34], the main source of interface states near the conduction band in MoS$_2$ is externally induced lattice strain. This occurs because the bandgap formation in this material is mainly due to the separation of d orbitals in molybdenum, which contributes to both the conduction and valence bands. As the material is extremely thin, slight roughness or defects in adjacent insulators can locally distort the chemical bond between molybdenum and sulfur, altering the band structure. Consequently, interface traps with a U-shaped distribution appear within the bandgap.

The conjunction of all these factors can be modeled by the expression for the distribution of interface states near the conduction band, which behave as acceptors:

$$D_{it}(\mathcal{E}) = D_{it0} + D_{it1} \exp\left(-\frac{\mathcal{E}_c - \mathcal{E}}{\mathcal{E}_\sigma}\right), \qquad (22)$$

where D_{it0} is a fixed parameter, D_{it1} is the peak value, and $\mathcal{E}_\sigma$ determines the decay rate of the exponential. Fig. 9-a illustrates the validation of this model with the experimental data presented by Fang et al. [30].

The impact of interface traps can be included in the model for the channel potential by considering that a fraction of the carrier density $n_{it}(x)$ occupies these interface states, according to the position of the Fermi level [12]. However, this approach significantly complicates the process of obtaining an explicit analytical expression for $\varphi(V_{gs})$.

For compact modeling purposes, Xu et al. [35] noted that the effects of interface traps on the electrostatic potential are significant only in the subthreshold region. Under this bias condition, the Fermi level is far from the bottom of the conduction band, and D_{it0} is the dominant term in eq. (22).

Therefore, it is convenient to consider a uniform distribution with an effective value, $D_{it}(\mathcal{E}) = \overline{D_{it}}$. Then, we have a capacitance due to interface traps given as $C_{it} = q^2 \overline{D_{it}}$, and the channel potential in the subthreshold region is rewritten as

$$\varphi(x) \cong \frac{C_{ox}}{C_{ox} + C_i + C_{it}} (V_{gs} - V_t), \qquad (23)$$

This approximation is justified by contrasting C_{it} with the quantum capacitance, defined as

$$C_Q = q \frac{\partial n_{2D}}{\partial \varphi} = \frac{q^2 N_{DoS}}{k_B T} \left[\frac{\exp\left(\frac{\varphi - V}{\phi_T}\right)}{1 + \exp\left(\frac{\varphi - V}{\phi_T}\right)} \right], \qquad (24)$$

where Fermi-Dirac distribution was considered for improved accuracy. Also known as electrochemical capacitance [36], C_Q is directly associated with the two-dimensional density of states and represents the filling of discrete energy levels in the conduction band as a function of the applied voltage.

Fig. 9-b shows a comparison between the two capacitances for $V_{gs} < V_t$. The quantum capacitance grows exponentially with φ and exceeds C_{it}, which has an almost invariant behavior when $V_{gs} \ll V_t$. In [30], the authors suggest that $\overline{D_{it}} = 8 \times 10^{12}$ eV^{-1}cm^{-2} is able to reproduce the experimentally measured subthreshold slope a device fabricated with a 1 nm thick layer of yttrium oxide (Y$_2$O$_3$) used as a buffer layer to easy the deposition of the Al$_2$O$_3$ layer onto MoS$_2$ and improve the interface quality.

IV. MODELING OF I–V CHARACTERISTICS

For the modeling the I–V characteristics, the expression for the drain current can be directly written as a function of the electrostatic potential [12] or as a function of the charge in the channel [17], which is a function of the electrostatic potential. In both cases, our approach results in fully analytical expressions. However, the second option is the one that provides the best results, free from numerical errors.

A. DRIFT-DIFFUSION FORMALISM

The I–V characteristics of the 2D-FET considering carrier transport governed by the drift-diffusion formalism are obtained by solving the following integral:

$$I_{ds} = \frac{qW}{L} \int_0^{V_{ds}} \mu n_{2D} dV, \qquad (25)$$

where the carrier mobility may initially be taken as $\mu = \mu_0$, a constant value.

Considering the gradual channel approximation, an expression for the Fermi level potential as a function of the channel potential is derived from eq. (9):

$$V = \frac{\lambda^2}{\mathcal{E}_s t_s} \left[C_{ox} (V_{gs} - V_t) - q n_s \right] - \phi_T \ln\left(\frac{n_{2D}}{N_{DoS}}\right). \qquad (26)$$

It is convenient to change the variables in the integral of eq. (25):

$$I_{ds} = \frac{qW\mu_0}{L} \int_{n_S}^{n_D} n_{2D} \frac{dV}{dn_{2D}} dn_{2D}, \qquad (27)$$

where $n_S = n_{2D}(V = 0)$, $n_D = n_{2D}(V = V_{ds})$ and

$$\frac{dV}{dn_{2D}} = -\frac{q\lambda^2}{\varepsilon_s t_s} - \frac{\phi_T}{n_{2D}}. \qquad (28)$$

Solving the integral yields an expression for the I–V characteristics of a single-gate long-channel device, initially neglecting deleterious effects:

$$I_{ds} = -\frac{qW\mu_0}{L} \left[\phi_T (n_D - n_S) + \frac{q\lambda^2}{\varepsilon_s t_s} \left(n_D^2 - n_S^2 \right) \right]. \qquad (29)$$

Since the carrier concentration depends only on the electrostatic potential and that this expression for the electrostatic potential can be explicitly obtained using the technique presented in the previous section, the I–V characteristics can also be calculated without the aid of numerical routines, which is an attractive feature for integrated circuit simulators.

B. SUBTHRESHOLD CURRENT CONSIDERING SHORT-CHANNEL EFFECTS AND INTERFACE TRAPS

Analyzing only the subthreshold regime, eq. (25) can be solved with the aid of eq. (10):

$$I_{ds} = \frac{W\mu_0 q N_{DoS} \phi_T}{L} \exp\left[\frac{C_{ox}}{C_{ox} + C_i} \left(\frac{V_{gs} - V_t}{\phi_T} \right) \right] \times \left[1 - \exp\left(\frac{-V_{ds}}{\phi_T} \right) \right]. \qquad (30)$$

Considering now the electrostatic potential including short-channel effects, given by eq. (20), we have:

$$I_{ds} = \left\{ \frac{2W\mu_0 q N_{DoS} \phi_T \sqrt{\frac{A_2}{\pi\phi_T}} \exp\left(\frac{A_0}{\phi_T}\right)}{\mathrm{erf}\left[\sqrt{\frac{A_2}{\phi_T}} x_{min}\right] + \mathrm{erf}\left[\sqrt{\frac{A_2}{\phi_T}} (L - x_{min})\right]} \right\} \times \left[1 - \exp\left(-\frac{V_{ds}}{\phi_T} \right) \right]. \qquad (31)$$

where erf (a) is the error function, which can be approximated by [29]

$$\mathrm{erf}(a) \approx \frac{2}{\pi} \tan^{-1} \left[\frac{\pi}{2} \left(1.2a^4 + 0.1a^3 + 0.5a^2 + a \right) \right] \qquad (32)$$

to obtain a fully analytical expression for the subthreshold current.

Now, taking into account the degradation of subthreshold slope due to interface traps, eq. (23), we have:

$$I_{ds} = \frac{W\mu_0 q N_{DoS} \phi_T}{L} \exp\left[\frac{C_{ox}}{C_{ox} + C_i + C_{it}} \left(\frac{V_{gs} - V_t}{\phi_T} \right) \right] \times \left[1 - \exp\left(\frac{-V_{ds}}{\phi_T} \right) \right]. \qquad (33)$$

C. MOBILITY DEGRADATION AND VELOCITY SATURATION

Regarding the current behavior above threshold, high values of gate or drain voltage will lead to carrier mobility degradation and velocity saturation, respectively. Both effects can be introduced semi-empirically into our compact model by modifying the parameter $\mu(x)$. In this case, the mobility ceases to be a fixed parameter and effectively varies with the voltages biasing the transistor.

When an intense vertical electric field is present, the charge centroid in the channel shifts towards the gate oxide or the substrate insulator, depending on the bias conditions. As a result, charge carriers become more affected by dangling bonds, interface roughness, and any fixed charges present in these dielectrics, leading to more surface scattering, which degrades the effective mobility of the two-dimensional material.

Cao et al. [12] suggest that the empirical mobility model commonly used in silicon MOSFETs can be also utilized to describe this phenomenon in 2D-FETs. Then, we have

$$\mu(x) = \frac{\mu_0}{1 + \left(\frac{\varepsilon_{ox}|E_{z_1}(x)| + \varepsilon_i |E_{z_2}(x)|}{\varepsilon_s |E_{zC}|} \right)^\varsigma}, \qquad (34)$$

where $E_{z_1}(x)$ and $E_{z_2}(x)$ represent the vertical electric field at the interface with the oxide and in the insulator, E_{zC} is the critical value of the vertical electric field, and ς is a fitting parameter. It is important to note that $E_{z_1}(x)$ and $E_{z_2}(x)$ have a non-trivial dependence on $V(x)$ through $\varphi(x)$, in such way that the integral in eq. (25) would need to be solved numerically.

A possible simplification to reach an analytical solution is to take a midpoint along the channel to average out an invariant value of mobility with respect to x, in such way that, $\mu_{\deg} = \mu(x = L/2)$, where $\mu(x)$ is calculated by eq. (34). Then, $\mu(x)$ can be removed from the integral in eq. (25). To formalize an analytical expression for compact modeling of the I–V characteristics, the following definition is used:

$$\mu = \begin{cases} \mu_0, & V_{gs} \leq V_t \\ \mu_{\deg}, & V_{gs} > V_t \end{cases}. \qquad (35)$$

Also, when the longitudinal electric field along the channel reaches a critical value E_{xC} at some point near the drain contact, the carrier velocity saturates, becoming equal to a constant value v_{sat}. This effect can be included in the model via a semi-empirical function widely employed to model conventional MOSFETs [14], [37]:

$$\mu(x) = \frac{\mu_0}{1 + \left[\frac{\mu_0 E_x(x)}{v_{sat}} \right]}, \qquad (36)$$

where $E_x(x) = d\varphi(x)/dx \approx (\varphi_D - \varphi_S)/L$ within the gradual channel approximation.

As discussed in [37], besides including a field-dependent mobility term, it is also necessary to revisit the upper limit of integration in eq. (25). This is because the electrostatic potential at the drain side saturates at a value $\varphi_{d_{sat}}$. The
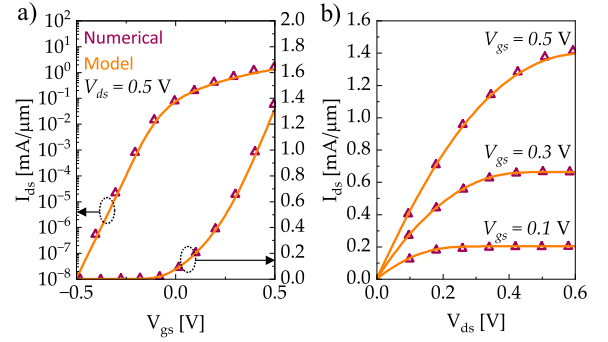
FIGURE 10. Validation of the I–V characteristics against simulation data [12]. a) $I_{ds} - V_{gs}$ in linear and logarithmic scales. b) $I_{ds} - V_{ds}$ for various V_{gs} values. Parameters: monolayer MoS_2 channel with $N_D = 3.5 \times 10^{11}$ cm^{-2}, SiO_2 gate oxide ($t_{ox} = 2$ nm), Al_2O_3 insulator ($t_i = 90$ nm), Al gate, n^{++} Si substrate, $\mu_0 = 50$ cm^{2}V^{-1}s^{-1} and $L = 10\,\mu$m.

value of the electrostatic potential for which velocity saturation occurs can be easily calculated through the condition $dI_{ds}/d\varphi_D = 0$ when $\varphi_D = \varphi_{D_{sat}}$.

With the aid of eq. (11), it is also possible to calculate the value of V_{ds} which causes current saturation:

$$V_{ds_{sat}} \cong \varphi_{D_{sat}} - \phi_T \ln \left[\frac{C_{ox}}{qN_{DoS}} \left(V_{gs} - V_t \right) \right]. \qquad (37)$$

V. RESULTS AND DISCUSSION

To demonstrate the accuracy of our expressions for the I–V characteristics, it is necessary to contrast them with simulation and experimental data available in the literature. In what follows, we seek to validate every aspect of the expressions presented in the previous sections, starting with the current-voltage relationship, obtained using our own method for the explicit calculation of the electrostatic potential.

Fig. 10 shows the validation of eq. (29) against simulation data presented in [12]. The 2D-FET employs a monolayer MoS_2 channel of length $L = 10\,\mu$m, long enough to allow short-channel effects to be neglected. Interface traps or any other non-idealities are also not included in this particular simulation. In any case, the results provide excellent agreement and correctly reproduces the $I_{ds} - V_{gs}$ characteristics (both in linear and logarithmic scales), with a maximum relative error of 13.83% near the threshold, and $I_{ds} - V_{ds}$ for various V_{gs} values, with a maximum relative error always below 2%. The use of the analytical approximation for the electrostatic potential is demonstrated to be a very accurate description, almost identical to the exact solution obtained numerically. In this particular case, we used $n = 2$ in eq. (13) to assure good accuracy.

Fig. 11-a shows the validation of eq. (31) against TCAD simulation (Silvaco ATLAS) data available in [13]. The device is based on a monolayer MoS_2 channel with $L = 5.9$ nm, in which short channel effects become significant. Since the device uses 2.6 nm of Al_2O_3 as gate oxide, the correction concerning the effect of the lateral electric field of the oxide, eq. (21), also needs to be included. For comparison
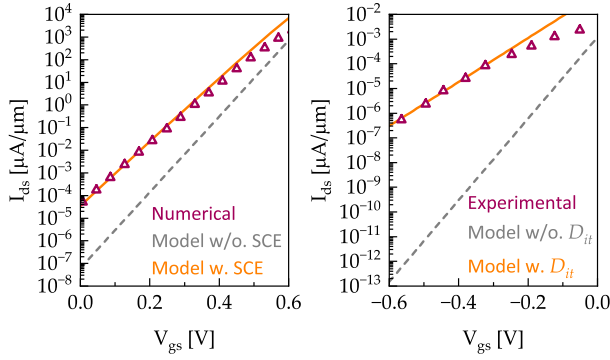
FIGURE 11. Validation of I–V characteristics considering degradation effects in the subthreshold region. a) Short-channel effects: results from our model in contrast to TCAD simulations (Silvaco ATLAS) [13]. Parameters: Monolayer MoS$_2$ channel with $N_D = 3.5 \times 10^{11}$ cm^{-2}, $\mu_0 = 320$ cm^{2}V^{-1}s^{-1} and $L = 5.9$ nm, $V_{ds} = 0.64$ V, HfO$_2$ gate oxide ($t_{ox} =$2.6 nm), SiO$_2$ insulator $t_i =$270 nm), and n^{++} Si substrate. The threshold voltage was set to $V_t = 0.7$ V to match the simulation data. A factor $\alpha = 0.96 \varepsilon_{ox}/\varepsilon_{SiO_2}$ was considered to account for the lateral field in the oxide. b) Interface-traps effects: results from our model in contrast to experimental data [6]. Parameters: Monolayer MoS$_2$ channel with com $N_D = 3.5 \times 10^{11}$ cm^{-2}, $\mu_0 = 47$ cm^{2}V^{-1}s^{-1}, $L = 0.5\mu$m, $W = 4\mu$m, $V_{ds} = 0.01$ V, HfO$_2$ gate oxide ($t_{ox} =$30 nm), SiO$_2$ insulator ($t_i = 270$ nm) nm), and n^{++} Si substrate. The threshold voltage set to $V_t = 0.23$ V and a trap density $D_{it} = 4 \times 10^{12}$ eV^{-1}cm^{-2} are employed to match the experimental data.

purposes, the subthreshold current considering a long channel (GCA approximation), eq. (30), is also presented, to illustrate the degradation of the subthreshold slope.

Fig. 11-b shows the validation of eq. (33) against experimental data presented in [6]. The MoS$_2$ layers for the experimental devices were obtained using mechanical exfoliation and transferred to a Si/SiO$_2$ substrate [6]. Next, 30 nm of HfO$_2$ were deposited using the ALD technique. Therefore, as discussed earlier, defects are expected to appear at the interfaces of the channel with adjacent layers. Here, a value of $D_{it} = 4 \times 10^{12}$ eV^{-1}cm^{-2} is employed to reproduce the experimental data. For comparison, the ideal subthreshold current, eq. (30) is also shown.

Fig. 12-a shows the validation of the current-voltage characteristics, considering now the mobility degradation, as compared to simulation data presented in [12]. The analytical approximation effectively captures the behavior of the I–V characteristics above threshold. The ideal current-characteristics, eq. (29), is also displayed for comparison. In this case, $E_{zC} = 21 \times 10^7$ V/m and $r = 1.3$ are used as fitting parameters.

Fig. 12-b shows the validation of the drain current expression, including velocity saturation, as compared to simulation data presented in [38]. The model efficiently describes the I–V characteristics in the saturation regime with $v_{sat} = 3 \times 10^6$ cm/s, a value very close to the obtained in [38] using the Monte Carlo method. For comparison purposes, the ideal I–V curve, eq. (29), is also displayed to underscore the relevance of the correction applied to the carrier mobility, eq. (36).

To further consolidate our work, the compact model is validated in comparison to experimental data from [39], as shown
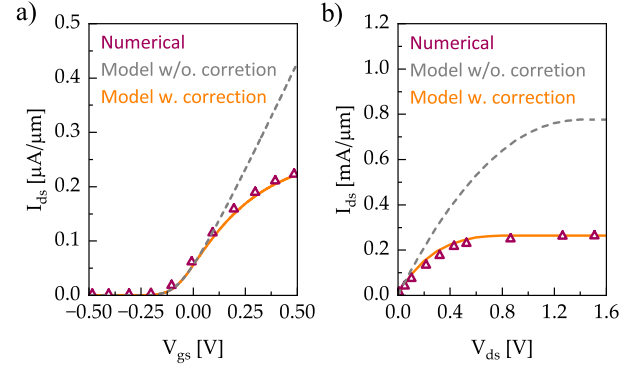
FIGURE 12. Validation of I–V characteristics considering degradation effects above the threshold voltage. a) Mobility degradation: our results in contrast to simulation data [12]. Parameters: Monolayer MoS$_2$ channel with $N_D = 3.5 \times 10^{11}$ cm^{-2}, SiO$_2$ gate oxide ($t_{ox} =$2 nm), Al$_2$O$_3$ insulator ($t_i = 90$ nm), Al gate, n^{++} Si substrate, $\mu_0 = 50$ cm^{2}V^{-1}s^{-1} and $L = 10\mu$m. $E_{zC} = 21 \times 10^7$ V/m and $\varsigma = 1.3$ are used as fitting parameters. b) Velocity saturation: our results in contrast to simulation data [38]. Parameters: Monolayer MoS$_2$ channel with $N_D = 3 \times 10^{12}$ cm^{-2}, HfO$_2$ gate oxide ($t_{ox} = 13$ nm), SiO$_2$ insulator ($t_i = 270$ nm), Al gate, n^{++} Si substrate, $\mu_0 = 50$ cm^{2}V^{-1}s^{-1}, $L = 100$ nm and $v_{sat} = 3 \times 10^6$ cm/s.

in Fig. 13. The results demonstrate excellent agreement, correctly capturing various aspects of the I–V characteristics. A fixed fitting factor was used to match the current amplitude to the experimental data. This fitting factor represents the effect of the reported access resistance of 1.3 kΩ-μm. On the other hand, the channel length modulation effect is not being considered, which explains the small discrepancies in the I_{ds}–V_{ds} curves in saturation condition (Fig. 13-b).
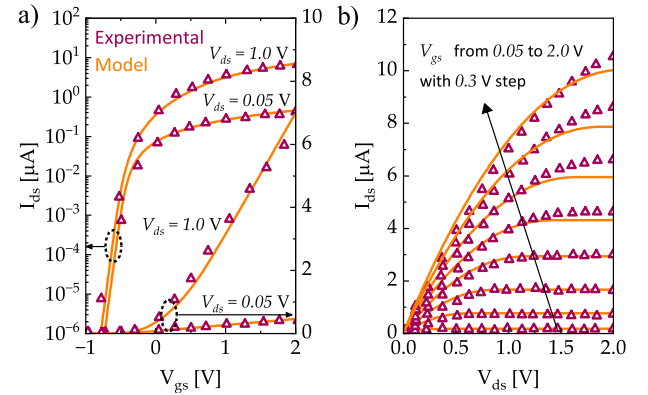
FIGURE 13. Validation of I–V characteristics in comparison to experimental data [12]. a) $I_{ds} - V_{gs}$ in linear and logarithmic scales. b) $I_{ds} - V_{ds}$ for several V_{gs} values. Parameters: MoS$_2$ channel ($t_s =$5 nm) with $N_D = 5 \times 10^{11}$ cm^{-2}, ZrO$_2$ gate oxide ($t_{ox} =$20 nm), SiO$_2$ insulator ($t_i = 260$ nm), Ni gate, n^{++} Si substrate, $\mu_0 = 38$ cm^{2}V^{-1}s^{-1}, $L = 2\mu$m and $W = 3.3\mu$m. A fixed fitting factor of 0.375 was used to match the current amplitude to the experimental data. This factor is related to the effect of an access resistance of 1.3 kΩ-μm reported by the authors.

VI. CONCLUSION

In this paper, we have developed a compact model for 2D-FETs based on molybdenum disulfide, offering a fully

analytical, explicit, and physics-based formulation of the current-voltage characteristics. By means of a systematic approach starting from the Poisson equation and the drift-diffusion transport model, we derived closed-form expressions for the electrostatic potential, channel charge, and drain current. Key non-idealities, such as interface traps, short-channel effects, carrier mobility degradation, and velocity saturation were also incorporated into a unified analytical framework, improving the predictive capability of the model.

The proposed model is particularly well suited for integration into circuit simulation environments, given its analytical simplicity and absence of special functions or iterative procedures. These features make it a promising candidate for SPICE-compatible implementation, enabling fast and reliable circuit-level design based on 2D-FET technology. Potential applications include digital logic gates, analog front-end blocks such as amplifiers and comparators, and flexible or wearable electronics, where the use of atomic thin 2D semiconductor channels provide key advantages.

This work focused on MoS_2 due to its experimental maturity, but the modeling strategy is general and can be extended to other transition metal dichalcogenides (TMDs) or even to anisotropic 2D semiconductors such as black phosphorus, by appropriately adjusting the material parameters. Likewise, the symmetrical structure of the derived current expressions allows straightforward application to p-type devices, supporting CMOS-like design.

Looking forward, we highlight some improvements and extensions that could enhance the accuracy of the proposed model and foster its widespread adoption. For instance, the empirical mobility expression employed here, which is adapted from conventional silicon-based FET models, could be replaced by a more rigorous mobility model derived from the unique scattering mechanisms in 2D materials. This requires dedicated studies, possibly involving first-principles calculations, detailed transport simulations and experimental investigations.

Another important issue concerns the modeling of source and drain contacts. Although Schottky barrier FETs (SB-FETs) fall outside the scope of our work, contact resistance and barrier formation play a crucial role in the performance of top-gated 2D transistors. Incorporating these effects into physics-based models remains a key challenge and a necessary step towards a more complete model.

From a broader perspective, advancing compact modeling for 2D-FETs also requires bridging the gap between academic formulations and commercial-grade simulation tools. While academic models such as ours often prioritize physical insight, commercial SPICE models demand continuity, charge conservation, and numerical stability. Notable efforts, such as the S2DS model [15], have begun to address these challenges by combining physical modeling with data calibration and Verilog-A implementation. Our model contributes to this landscape by offering a more compact yet rigorous analytical formulation, which can also serve

as a basis for future developments aiming at commercial deployment.

As a final remark, the excellent electrostatic control provided by using two-dimensional materials allows a reduction of the transistor length until the ballistic limit of the current is eventually reached, as recently demonstrated for MoS_2 transistors [40]. In this case, carriers are able to travel through the channel without significant scattering, and the drift-diffusion (DD) formalism used in this work will be no longer valid. For this reason, we have also developed models for ballistic 2D-FETs based on the Landauer transport formalism [26], [27], [28].

In practice, the choice of drift-diffusion (DD) or Landauer ballistic transport formalisms to describe a particular device will depend on the level of maturity in each specific fabrication process. Currently, the suppression of scattering mechanisms below the level needed to assure ballistic transport is beyond the reach of most research groups, in such way that DD-based models will stay strongly relevant in the near to mid future and even in the long term, for quite a few of the more challenging materials.

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