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Failure Mechanism and Sampling Frequency Dependency on TID Response of SAR ADCs

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Abstract
This paper describes the main failure mechanism of charge redistribution Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) under radiation. Results of two different radiation experiments (gamma and X-ray) each considering two identical 130nm, 8-bit SAR ADCs, operating with distinct sampling rates, showed that lower sampling frequencies cause the converters to fail at lower accumulated dose, while increasing the sampling frequency increases the converters robustness to radiation. A SPICE model of a SAR ADC is used to simulate radiation induced leakage effects, considering the same technology node and operating conditions of the tested converters. A very good agreement between simulation results and gamma irradiation experimental data allows us to explain the main failure mechanism, which is related to leakage in switches connected to the programmable capacitor array of the internal DAC of the converter.

Keywords Analog-to-Digital Converters · Leakage · Reliability · Radiation · Gamma · X-ray

1 Introduction

Ionizing radiation effects in integrated circuits (ICs) significantly affects the reliability of electronic systems exposed to such environmental condition. An important class of effect in MOS transistors is the Total Ionizing Dose (TID), which causes electrical degradation due to the accumulation of trapped charges in the insulation oxides, affecting the threshold voltage (V_{th}) of transistors, the leakage current and the carrier mobility, among other parameters [30–32]. These effects usually depend on biasing, switching frequencies, and size of the transistors [3, 14, 21, 34, 37] and may even lead to complete system failure.

Electronic systems applied to control, instrumentation and communication tasks comprise mixed-signal interfaces that include Analog-to-Digital Converters (ADCs). These circuits are crucial in satellites, spacecrafts and data acquisition systems of nuclear facilities and particle accelerators, for instance. Therefore, as important as the correct functioning of computing units and digital system parts, is the reliability of analog-to-digital (AD) and digital-to-analog (DA) system interfaces. Examples of works in which reliability to radiation effects and mitigation techniques were evaluated in such blocks can be found in [4, 5, 9, 12, 20, 24, 36].

In a previous work of our research group a fault-tolerant data acquisition system (DAS) was proposed to cope with radiation effects and other environmental degradation sources [9, 13, 22, 23]. The system was designed and programmed in a Commercial Programmable System-on-Chip (PSoC) from Cypress Semiconductor [11] fabricated in a 130 nm CMOS

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process. The adopted fault tolerance strategy is based on diversity redundancy, with hardware and time redundancy, in a way that the DAS is composed of three ADCs operating in parallel and two voters.

Two of the three converters of this system are identical Successive Approximation Register (SAR) converters based on charge redistribution, a popular architecture which benefits of low power, relatively small area and good achievable resolutions and sampling rates. Due to these features, SAR converters are present on several commercially available programmable mixed-signal platforms, such as PSoC5 [11], SmartFusion [2] and MSP430F6638 [35].

The low power feature of this kind of converter may be suitable for remote applications such as satellite control and instrumentation systems, and wireless sensor networks, for example. These applications may be subjected to environmental interactions, such as radiation effects and electromagnetic interference, and, despite that, these embedded converters should perform correctly in such conditions.

The current work focuses on the distinct radiation response of the SAR ADCs related to the individual sampling frequency, as well as on the elucidation of the main failure mechanism of the converters. In addition to the gamma irradiation results, presented in [10], this work presents new data of an X-ray experiment, which corroborates the observed effects related to the sampling frequency dependency on TID effects.

The irradiated SAR converters in each experiment belong to the same die and were set with different sampling frequencies (74 ksps and 740 ksps, where *sps* stands for samples per second). Results revealed that the radiation effects in the converter functionality is more severe for the converter which operates with lower sampling frequency.

Therefore, in the present work, a study comparing the results of SPICE simulations with experimental results of radiation tests is carried out. The obtained results allow us to understand the functional degradation mechanism, as well as the dependency of such degradation with the converter sampling frequency. Considering the findings of this study, we propose simple but effective strategies to enhance the robustness of such kind of converter when deployed in environments subjected to ionizing radiation.

2 The Studied Converters

2.1 Basics of Charge Redistribution SAR ADCs

SAR ADCs are sequential converters that uses the binary search principle to convert an analog input sample to an N-bit quantized representation. The main building block of a charge redistribution SAR converter is a capacitor array controlled by a set of switches. The charge redistribution technique was proposed by McCreary and Gray [27] in 1975 and soon became one of the most popular AD conversion alternatives when low area and low power are required. These features are achieved because the capacitor array plays the role of the Digital-to-Analog (DAC) converter required to generate the reference voltage levels on traditional SAR converters, at the same time that provides an intrinsic sample-and-hold operation. A simplified schematic of an 8-bit, single-ended, charge redistribution SAR is depicted in Fig. 1.

The binary search principle in a SAR converter consists in find the closest analog estimate of the input signal, using a voltage comparator that compares the input value (V_{IN}) with the output of the internal capacitive DAC [29]. In a charge redistribution SAR the DAC works by setting capacitive dividers (by means of programmable switches and binary weighted capacitors) that, in each redistribution step,

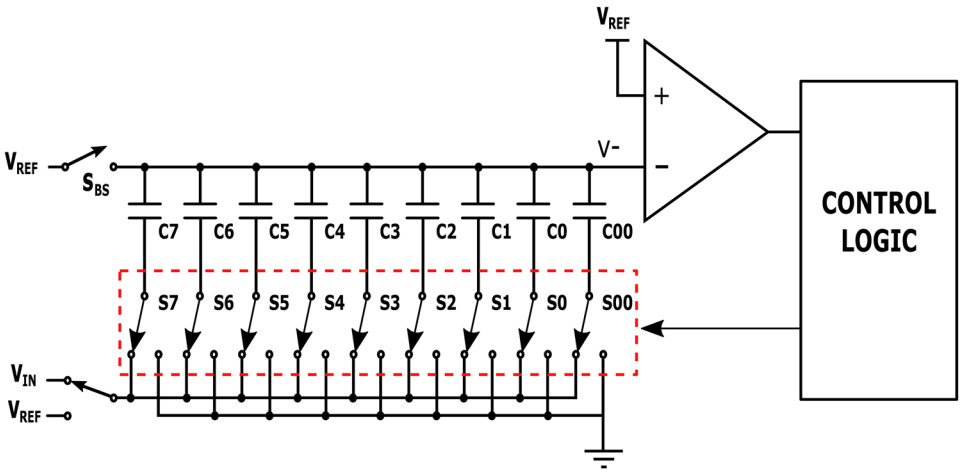


Fig. 1 8-bit Single ended SAR ADC simplified schematic

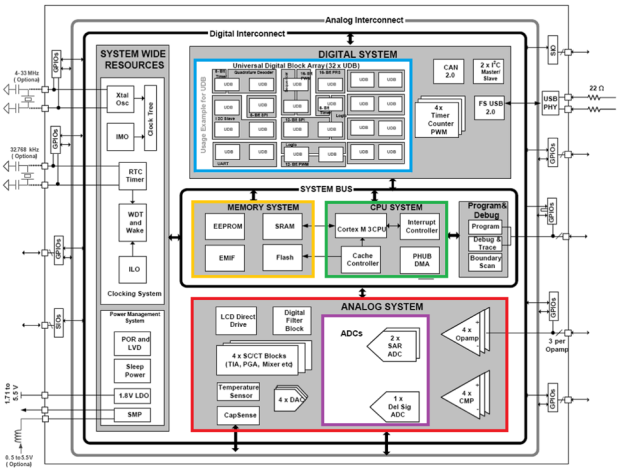


Fig. 2 PSoC 5LP block diagram

generate a voltage to be compared with the input sample. This way, the converted word converges to an N-bit digital representation of the input sample at the N_{th} redistribution step.

2.2 The Converters Under Test

The converters under test are part of a fault tolerant data acquisition system (DAS), proposed by our research group in [9]. The system was fully implemented in a commercial Programmable SoC (PSoC 5 from Cypress Semiconductor) manufactured in a 130 nm CMOS technology. Such device has a 32-bit ARM Cortex-M3 processor, several memory resources, digital peripherals, such as communication interfaces and programmable logic devices. The device also comprises analog peripherals, such as ADCs, DACs, comparators, operational amplifiers, and configurable analog blocks. The general architecture of the PSoC is presented in Fig. 2.

The available converters of PSoC are a Sigma-Delta (ΣΔ) AD converter and two Successive Approximation Register (SAR) converters. In this implementation both SAR converters were programmed to operate with different sampling rates (740 ksps and 74 ksps) and 8-bit wide output. A temporal voter and a synchronizer bock are used to synchronize the system [9]. The block diagram of the redundant DAS, prototyped into the PSoC device, is depicted in Fig. 3. Besides both SAR converters studied in this work the system also comprises a ΣΔ (operating at 74 ksps) converter, two voters, sample-and-hold blocks, direct memory access (DMA) blocks, a synchronizer and a status register block, which allows monitoring the converters during the experiment.

3 Radiation Experiments

This section presents the obtained results in two distinct radiation experiments over the considered DUT: a Cobalt-60 gamma irradiation and and a high dose rate X-ray experiment.

In both experiments, it was applied a 120 Hz signal at the converters input, alternating between a sinusoidal and a ramp signal, both swinging among the full scale limits of the converters (0 to 2V).

To allow monitoring the system during the experiment, the output of the converters are stored in internal buffers. The buffers content is sent to an external computer every 3 minutes (gamma experiment) and 2 minutes (X-ray experiment) by means of an UART/RS232 interface. The collected data is then used to calculate important parameters, such as Total Harmonic Distortion (THD), Effective Number of Bits (ENOB) and Integral Non-Linearity (INL). Figure 4 shows the experimental setup applied in the experiments, whose details are given in the following subsections.

3.1 Cobalt-60 Gamma Irradiation

In this experiment the system was exposed to ionizing radiation using a Cobalt-60 gamma radiation source from Atomic Energy of Canadian Limited (model Eldorado 78)

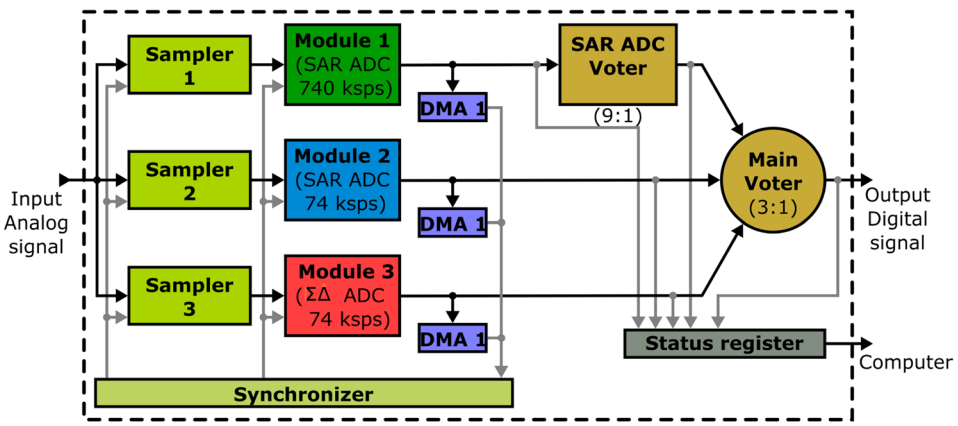


Fig. 3 Block diagram of the DAS programmed into the PSoC device

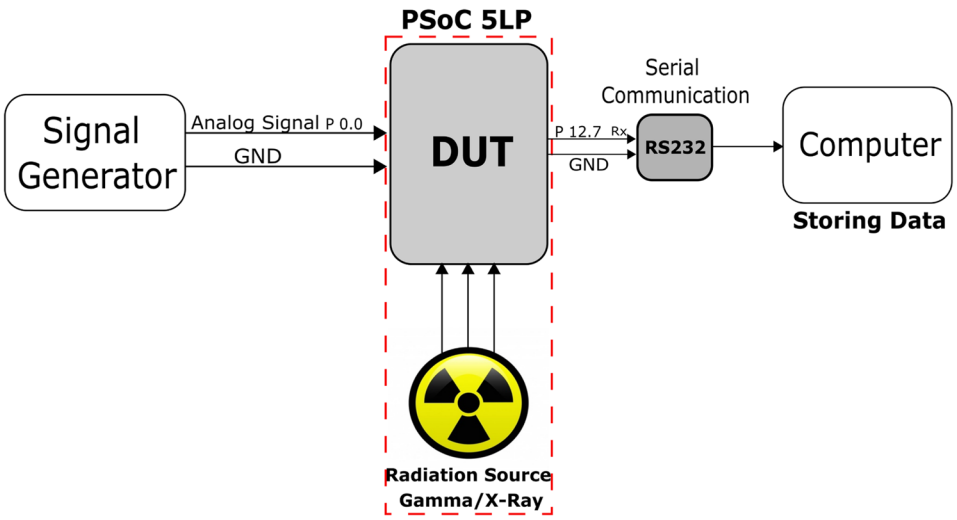


Fig. 4 Experimental setup for Gamma and X-Ray irradiation

with a dose rate of 0.28 rad(Si)/s (1 krad(Si)/h), following the European Space Agency (ESA) Basic Specification 22900 [15].

It is important to mention that both converters are submitted to the same radiation dose and biasing regimes. Due to facility schedule constraints the total dose accumulated by the devices was 242 krad(Si).

Concerning the behavior of the converters under study, results showed no significant degradation to the SAR ADC operating at 740 ksps (from here on referred to as SAR@740). For this converter, the THD at the end of experiment (accumulated dose of 242 krad(Si)) was approximately the same of the pre-rad situation (near 1%).

On the other hand, the THD of SAR@74 reached near 10% after irradiation. In practice, this means that the summed power of the spurious harmonics is equivalent to 10% of the power of the fundamental frequency of the signal, considering the sinusoidal stimulus. In this case, 10 harmonics were taken into account, as recommended by IEEE Standard for Terminology and Test Methods for ADCs [1]. This linearity degradation can be observed by visual inspection in Fig. 5a, which shows the converted signals for three values of accumulated dose, considering the ramp input stimulus. Conversely, negligible degradations is observed on SAR@740 block for the same dose values (Fig. 5b).

Besides degradation on linearity, it can be observed from Fig. 5 that the radiation caused the SAR@74 to present gain and offset errors. This behavior is due to the appearance of entire ranges of missing codes and changing in the code occurrence probability, as detailed in [22]. Figure 6 compares the INL (calculated using measured data) of the converter, before and after irradiation.

3.2 X-Ray Experiment

In order to confirm the sampling frequency dependency of the converters degradation due to TID, a second radiation experiment was performed using an XRD-6100 (Shimadzu) X-ray diffraction setup.

X-ray sources are very versatile for studying radiation effects in electronic devices since it is possible to modify the X-ray tube current, bias and the source-device distance, in order to choose an adequate dose rate. The radiation dose was determined using an ionization chamber considering the exposure measure and transformed into an absorbed dose in silicon [28]. The effective energy was measured using aluminum foils of different thickness and calculating the half-attenuation Al layer [26, 33].

A voltage of 20 kV was applied on a cooper X-ray source, generating a 10-keV effective energy X-ray beam. A current of 10 mA was applied on the X-ray tube terminals with a distance of 7 cm from the DUT. In this condition, the radiation dose rate was 30.3 rad(Si)/s (109 krad(Si)/h). For this experiment (different from the gamma irradiation) the DUT board was prepared by removing the top package of the PSoC 5 IC.

In this X-ray test, the experiment was ended when the PSoC system failed completely, with an accumulated dose of 30.6 krad(Si). Details on the adopted X-ray dosimetry methodology can be found in reference [6].

Although the effects caused by 10-keV X-ray photons and 1.25 MeV of ^{60}Co gamma-ray source are comparable, they are generated predominantly by different radiation mechanisms of interactions with matter: photoelectric effect (X-rays) and Compton scattering (gamma rays) [16, 18, 25]. Thus, the different mechanisms may generate charges that occupy different levels of energy in the trapping process.

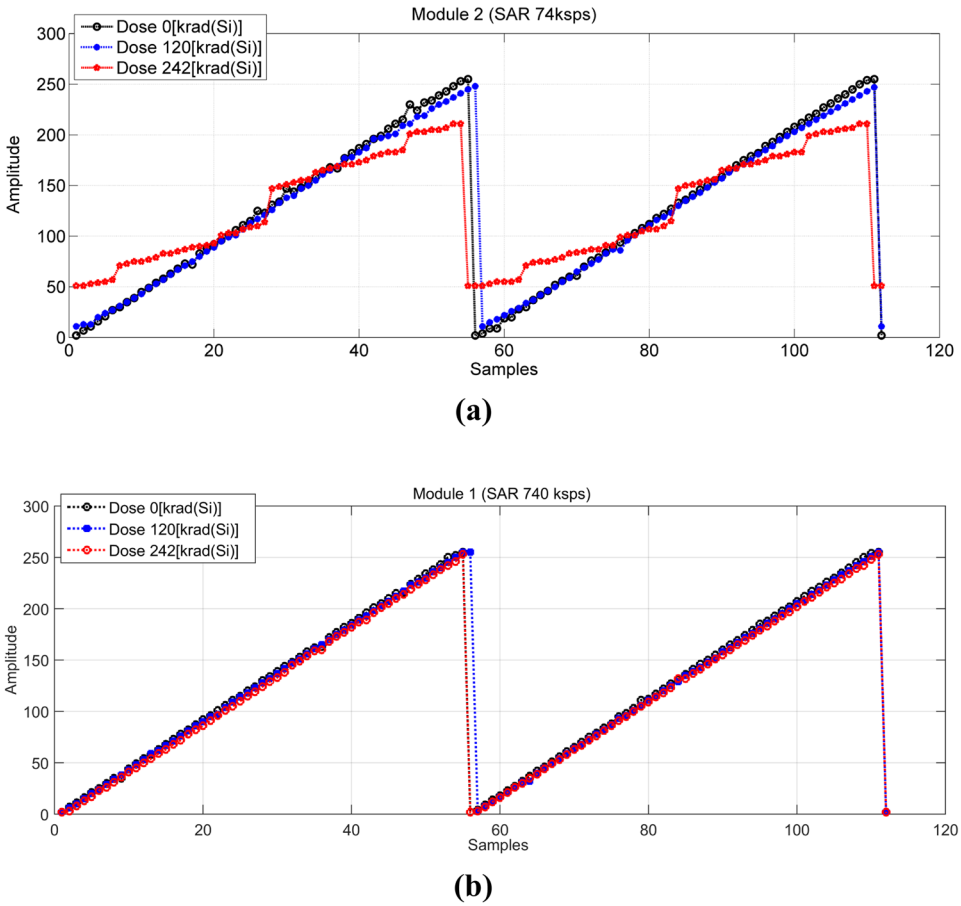


Fig. 5 Output of SAR@74 **(a)** and SAR@740 **(b)** for different accumulated doses during gamma irradiation

An important factor to be considered in the performed experiments is the different dose rates applied. High dose rates may lead to saturation of short half-life charge traps, because, at high dose rates, the charge trapping rate is much higher than the trap decay rate. At low dose rates, the escaping of charges from these traps is faster than the velocity of charge trapping. Therefore, in low dose rate irradiations, it can be expected the buildup of trapped charges being dominated by long-life traps. Thus, different charge buildup, and the consequent electrical degradation, may be observed for different dose rates. This process is also known as self-annealing. It is worth mentioning that lower dose rates are suitable to better reproduce the radiation of the space environment.

The fabrication process variability may also contribute, in some degree, to the failure behavior in both experiments, since the devices used in each experiment are not from the same fabrication batch. However, given to the high observed difference on the failure doses, and considering our previous experience in similar experiments, it is possible to affirm that variability is not the dominant effect in this case.

It is worth noticing that a second gamma experiment was performed with the studied device, in which a 13% variation in the failure dose was observed, compared with the first experiment (with the same trend observed for individual converters failure). Additionally, we have also observed, in past experiments of our group, and in literature data, variations in dose of failure that may be greater than this, tough within the same order of magnitude. The observed variation (between gamma and X-ray experiment) was near one order of magnitude (10×), indicating that another effect may be dominating this difference on results.

Uncertainties in X-ray dosimetry could also be a source of discrepancy. However, as already mentioned, a careful calibration setup was carried out, eliminating the possibility of this issue to be one of the main contributors. Future works are being considered in order to investigate the observed dose rate effects in this specific DUT.

With this in mind, one can conclude that the difference in dose rates is the main cause of the distinct values of total dose reached before failure in both experiments. Nevertheless, the trend related to the sampling frequency is the same.

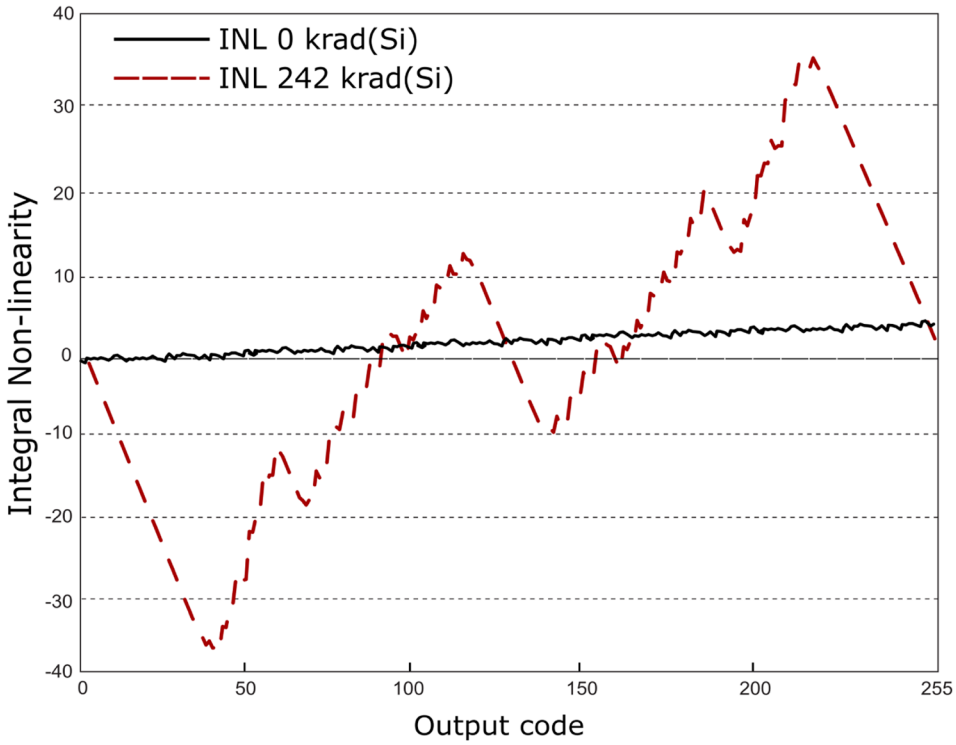


Fig. 6 Comparison of measured pre- and post- irradiation (gamma) INL for SAR@74 ADC

Table 1 shows the time of experiment and correspondent accumulated doses in which the converters and the whole system have failed. The failure of the converters, in this experiment, was considered when the signals harmonic distortion presented values higher than 20%. The whole system failure was characterized when all the communication and status signals where lost. It can be observed in Table 1 that the SAR converter operating with lower sampling frequency failed with a lower accumulated dose than the faster SAR, confirming the dependency on the sampling frequency observed in the previous gamma irradiation. The ΣΔ converter showed to be more robust to TID.

Figure 7 shows the waveform of the sawtooth signal at the converters output, for different accumulated doses, evidencing the sequence of converters failure shown in Table 1. The degradation starts to become visible for the slower SAR at an accumulated dose of 14.5 krad(Si) (Fig 7a) whose failure was registered at 18.1 krad(Si) (Fig 7b), while the faster SAR failed at 21.8 krad(Si) (Fig 7c). The ΣΔ converter was able to tolerate a 25.9 krad(Si) dose.

Due to the very high dose rate employed in this experiment and given the interval time in which the logs with the signal status were sent to the computer (2 minutes), failures were observed already in an advanced degradation state. For this reason, in this experiment it was not possible to verify the intermediate linearity degradation as in the gamma irradiation experiment. On the other hand, it was possible to witness the failure of all ADC modules and the complete system failure, differently from the previous experiment.

4 Failure Mechanism Investigation

4.1 Explaining the Observed Results

It can be observed from Fig. 5a stepped pattern of the output signal (after gamma irradiation) when the output code passes by codes which represents the voltage values generated by the capacitive DAC during binary search. This is evident in the figure at the following quantization values:

$$Q = 64 = 2^6 = 0.25V_{FS},$$
$$Q = 128 = 2^7 = 0.5V_{FS},$$
$$Q = 192 = (2^6 + 2^7) = (2^8 - 2^6) = 0.75V_{FS},$$

where V_{FS} is the full-scale voltage of the converter (2 V in this experiment).

Table 1 Accumulated dose and experiment time until the failure of the tested converters and PSoC system

Module	Time in minutes	Accumulated dose (krad/(Si))
SAR 74 ksps	10.0	18.1
SAR 740 ksps	12.0	21.8
Sigma-Delta	14.3	25.9
PSoC device	17.0	30.6

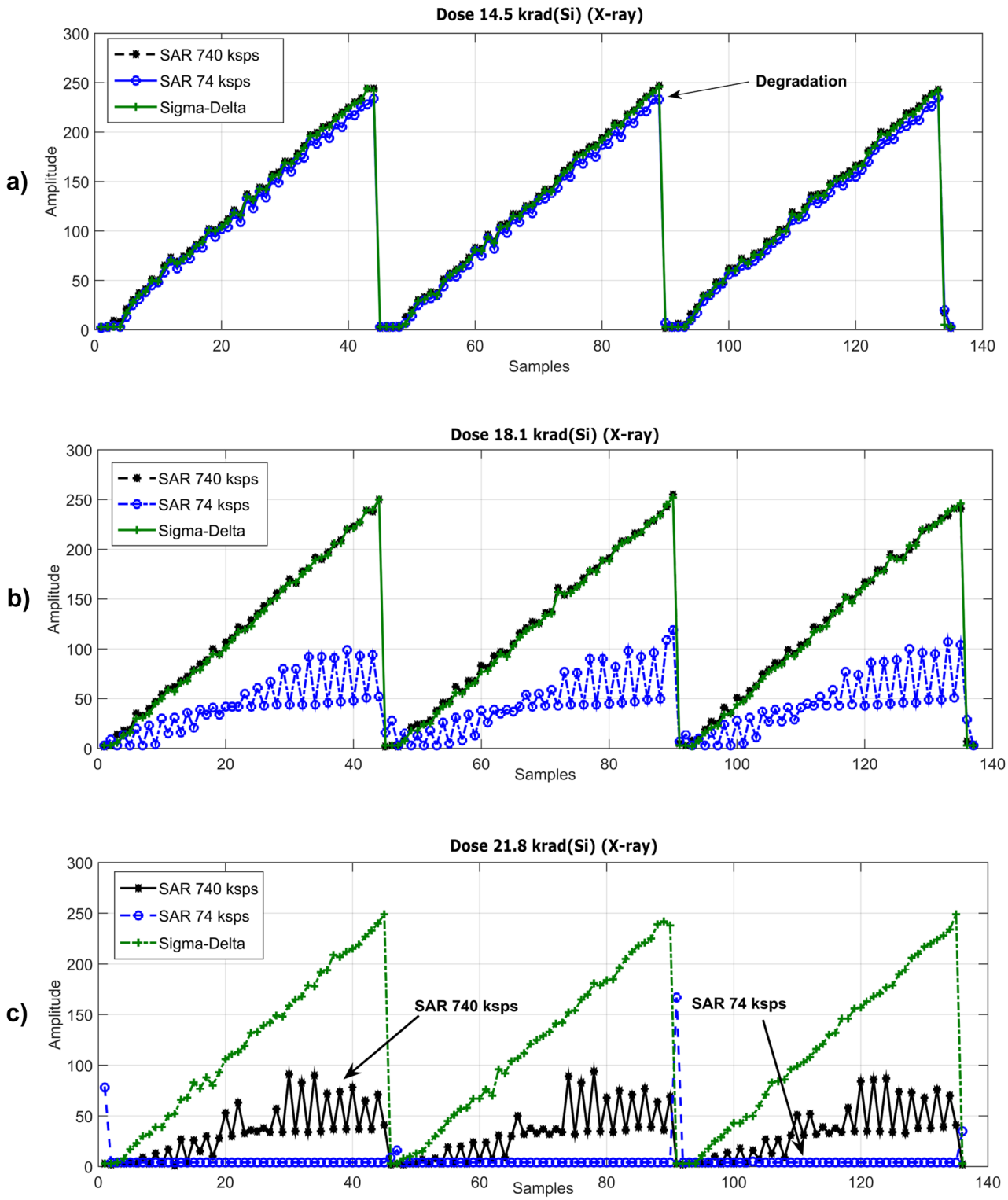


Fig. 7 Output of the tested converters, with the ramp signal as input, for different doses, during X-ray irradiation. **a)** The degradation starts to become visible for the SAR@74 ksps with an accumulated dose of 14.5 krad(Si); **b)** The SAR@74 ksps failure was registered at 18.1 krad(Si) dose; and **c)** The SAR@740 ksps failed at 21.8 krad(Si) dose

Because the capacitors of the internal DAC are binary weighted, this suggest that the main failure mechanism is originated at the capacitor array (rather than at the comparator or voltage reference blocks, for example). Considering also that the codes at both extremities are not being generated, it can be concluded that voltages generated by the

equivalent capacitive dividers at each redistribution step are not accurately being formed.

Firstly, the possible influence of the different switching activity on the observed results was analyzed. Though the faster SAR experiences 10 cycles of sampling and charge redistribution, while the slower converter process a single sample, they are converting the same signal. This means that the voltages on the capacitors, and, consequently, the electric field across the capacitors insulator are kept equal in both converters most of time, despite the higher switching activity of SAR@740. It is known from literature, that the electric field on the oxide, besides biasing levels and duty cycles (impacting the value of integral of electric field across the oxides during the irradiation) are the key factors to self-annealing effects [17, 31, 34], presenting a higher influence than the switching activity itself. This agrees with previous experiments we made in mixed-signal programmable arrays in the past [3].

Finally, the ΣΔ converter tested in the experiment reported in this paper also relies on internal capacitors, both switched and static ones. This converter operates with the same sampling frequency of SAR@74 (74 ksps), and did not fail on the gamma essay, being the last to completely fail in the X-ray experiment.

With this in mind, we can assume that the main contribution to the observed conversion errors f SAR@74 is the leakage paths induced by radiation in the switching matrix of the programmable capacitor array. This will cause the stored charge, during the conversion steps, to leak from/to the capacitors, introducing an error to the generated voltage which is compared to decide the value of each converted bit.

By inspection analysis of a typical charge redistribution SAR circuit it was identified that this behavior can be attributed to leakage current from top plates of the capacitors, as suggested in [8], while leakage on other switches of the capacitor array have less impact to the conversion, as explained in next section. Additionally, the total charge leakage in a given redistribution step will be proportional to the time the voltage under comparison is hold by the equivalent capacitive divider, which explains the sample frequency dependent behavior observed in both radiation experiments. These observations are confirmed by the simulations detailed in Sects. 4.2 and 5.

4.2 Simulation Setup

Since the irradiated ADCs belong to a commercial device, no detailed information about the internal architecture of the converters is available. This way, in our simulations we used a single-ended model of an 8-bit SAR converter, considering the same technology node of the tested converters (130 nm). The circuit is the one depicted in Fig. 1. The total capacitance of the array of the modeled converter is 3.072 pF. The unit capacitance (C_0 and C_{00}) is 12 fF, with the other being binary weighted in relation to the unit. The reference voltage, as well the supply voltage, considered in simulations is 1.2 V.

In this circuit, leakage of the top plates of capacitors may occur through the switch that connects V_{REF} to the top plates of the capacitors. In the simulated circuit, this is a bootstrapped switch (named S_{BS}), because the voltage of the top plates ($V\_$) may achieve a voltage of up to 1.8 V (higher than the supply voltage) during the redistribution phase. The schematic of the bootstrapped switch is depicted in Fig. 8, while its location in the circuit is highlighted in Fig. 9. During the sampling phase (S_{BS} is closed), the capacitor C_{hold} is charged. This voltage is then added to 1.2 V (when $\overline{SampleControl} = 1$), during the redistribution phase, in order to allow a voltage larger than 1.2 V at M_1 gate, avoiding current flow in this transistor when $V\_$ is larger than 1.2 V.

Though the transistor connecting V_{REF} to the top plates in the simulated converter (M_1 of the bootstrapped switch) is a PMOS device (in which radiation induced leakage is negligible), leakage between these nodes may be due to malfunction of the bootstrap circuitry. In this specific switch, leakage at M_3, may reduce the voltage at M_1 gate, allowing current flow between nodes V_{REF} and $V\_$, depending on the voltage under comparison. Other bootstrapped switch architectures may have distinct devices being responsible for the leakage. Finally, a simple Transmission Gate (TG) may also be used if V_{REF} is kept lower than 2/3 of V_{DD}, which guarantees $V\_$ will be limited at V_{DD}. In this case, leakage will directly affect the NMOS transistor of the TG. In all cases, the designer must analyze the circuit to identify the weak points of each design (related to radiation-induced leakage), in order to employ some mitigation strategy, as discussed afterwards in this paper.

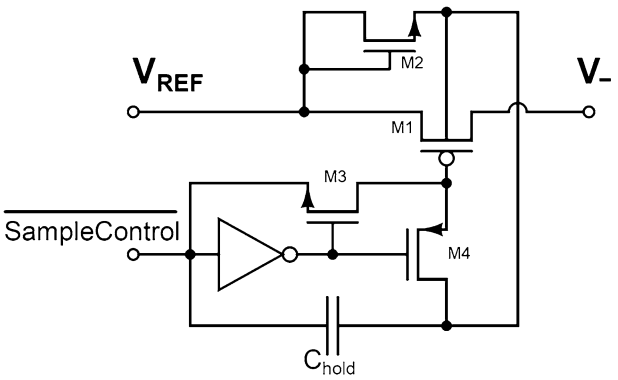


Fig. 8 Bootstrapped switch of the simulated converter

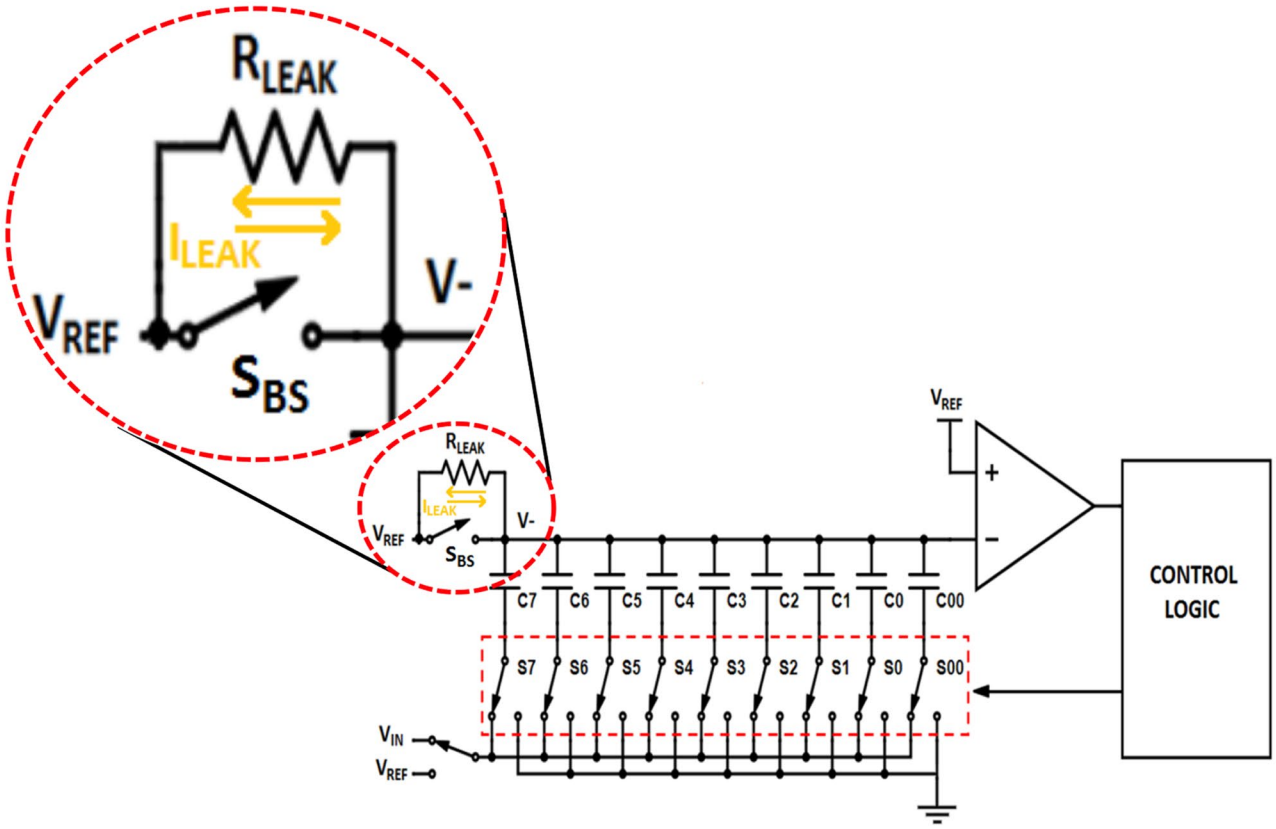


Fig. 9 Simulated SAR ADC with a leakage path between nodes $V\_$ and V_{REF}

Radiation-induced leakage may be simulated at circuit level by adding a current source, a parasitic transistor or a resistor between the nodes which form the leakage path. The first technique becomes inaccurate when the node voltages are variant, as is the case of this circuit.

We choose, for sake of simplicity, a resistor to model the leakage, since the observed pattern of signal degradation is symmetric (which is more evident in the results of gamma irradiation), suggesting the leakage current may occur from or to the capacitors, depending on the voltage ($V\_$).

In some related works [7, 21], radiation response of MOS transistors in 130 nm technologies is reported, associating the measured leakage with correspondent radiation dose. The exact behavior of a given transistor under radiation highly depends on its size and biasing condition. In this work the exact sizes of transistors of the irradiated circuit are unknown (though usual values are adopted in the simulated ADC) and the biasing is variable. Therefore, an exact reproduction of the radiation induced leakage, by simulation, is not possible, being the adopted values suitable to reproduce the approximate radiation response of the simulated devices.

In this simulation, the resistance value of R_{LEAK} (Fig. 9) was set to 1.5 MΩ, resulting in currents with order of magnitude of 10^{-8}A, which is compatible with the leakage values observed in the literature [7, 21], for transistors of 130 nm technologies under similar doses (with Cobalt-60 irradiation).

The circuit was simulated using *HSpice*^{TM}, considering a ramp from 0 to 1.2 V and 743 μs period as input stimulus.

As already mentioned, the actual circuit of the converter is probably different from the simulated one. Probably, the SARs of PSoC are fully-differential (rather than single-ended). Additionally, the bootstrapped switch may have a distinct architecture. However, this does not modify the sampling scheme of this type of converter, in which a special switch, connecting the voltage reference to one of the capacitor array terminals, is required. Nevertheless, the main elements of a charge redistribution SAR ADC were simulated in our setup. Finally, the way we simulated the leakage path on the top plates is sufficiently generic, so that it can model both direct leakage and malfunction of either a bootstrapped switch or a simple transmission gate.

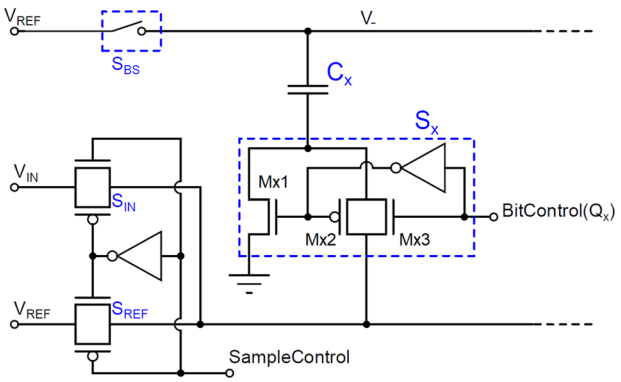


Fig. 10 Transistor level representation of a switch belonging to a branch of the capacitor array

Though the leakage may affect several NMOS transistors of the simulated circuit, leakage on NMOS transistors of switches S_{00} to S_7 will not significantly modify the voltage under comparison (though contributing to the power consumption increase) as explained below.

Figure 10 depicts one capacitor branch (C_x) with the corresponding switch (S_x). If considering the redistribution phase, the bottom plates of the capacitors must be connected either to ground (through M_{x1}) or to V_{REF} (through the TGs S_{REF} and the one formed by M_{x2} and M_{x3}). Assuming the second case, leakage in M_{x1} (which should be open) will create a conduction path from V_{REF} to ground. However, the voltage on the bottom plate of C_x will still be V_{REF}, unless this current is high enough so that the V_{REF} source cannot appropriate drive it, which will happen only in extreme situations (which may be the case of the observed results at the end of X-ray experiments). Considering now the opposite configuration to S_x (M_{x1} closed and the internal TG open), current due to leakage in M_{x3} will be deviated to ground via M_{x1}. The same applies in the sampling phase, when V_{IN} must be connected to the bottom plates.

Therefore, assuming values of dose in which the voltages V_{REF} and V_{IN} present sufficient drive strength to provide the radiation-induced extra leakage current, there will be no significant change in the voltage of the array, if compared with the voltage error caused by leakage in the top plate switch (S_{BS}).

Leakage simulations were also performed in switches S_{00} to S_7 with no observable voltage error to the considered leakage current value.

Additionally, simulation of leakage in the transistors of the comparator also showed to have no significant effect. The same order of leakage current value was simulated in the NMOS devices of a latched comparator (architecture described in [4]), corresponding to doses of up to 1 Mrad(Si), according to the transistors dimensions. Negligible offset and settling time degradation were observed in the obtained results.

In fact, the effects of ionizing radiation on the comparator of SAR ADCs will depend on its power consumption (which reflects the biasing of the transistors). The mean power consumption of the simulated comparator is 12 μW, which can be considered a low-power consumption for an analog building block. Ultra-low power analog circuits, with consumption of the order of nW, may present distinct behavior [19], being more sensitive to TID, if considered the tested dose values.

This way, the next section focuses on the results of leakage simulation on the switch S_{BS}, since it was the only element of the circuit whose malfunction due to the simulated leakage lead to functional deviations in the considered converter model.

It is important to remark that the correspondence of simulated leakage current values with total dose is made considering data from Cobalt-60 gamma irradiation results presented on literature, with similar dose rates, on transistors of the same technology node of the DUT. Considering the X-ray results, there is no available literature data which can be used to try to simulate the same conditions of the

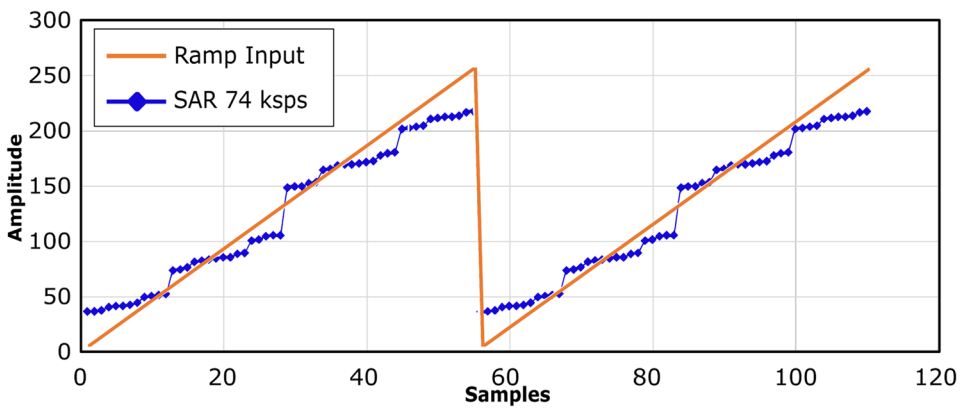


Fig. 11 Simulated output vs. input plot for the 74 ksps SAR ADC, considering leakage in the S_{BS} switch

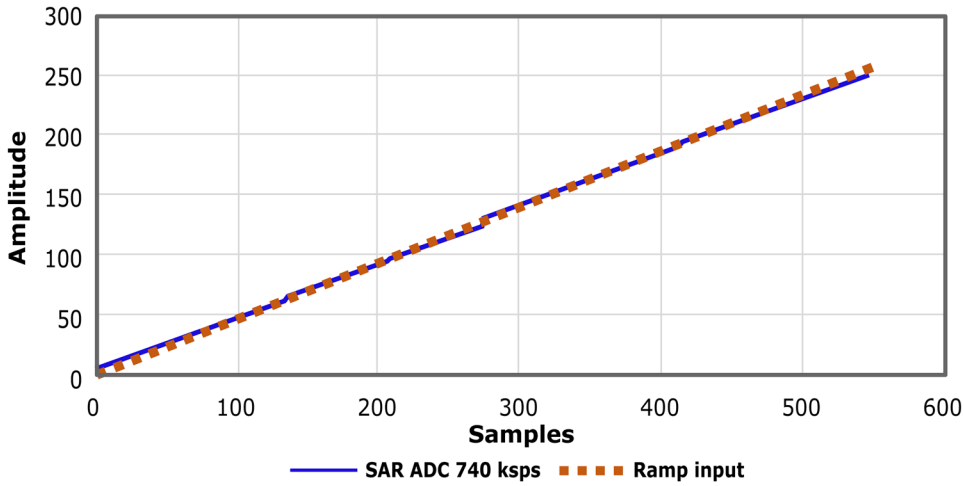


Fig. 12 Simulated output vs. input plot for the SAR ADC operating at 740 ksps, considering the adopted leakage model

performed experiment. Additionally, as stated before, the lower dose rate used in the Cobalt-60 experiment emulates, in a more realistic way, what can happen in a space mission. Therefore, the simulations performed in the current work are focused on the results observed for the Cobalt-60 gamma radiation experiment.

5 Simulation Results and Discussion

Figure 11 shows the simulation results for the conversion of the input ramp stimulus by the slower converter (SAR@74) considering the radiation-induced leakage model in the bootstrapped switch. It can be seen that the converted signal degradation is very similar to the experimental data showed in Fig. 5a. The amplitude drop of the output signal, the decrease on the conversion slope and the values of the missing codes, are very similar validating the adopted dual-direction (voltage dependent) leakage model between $V\_$ and V_{REF} nodes for this simulation.

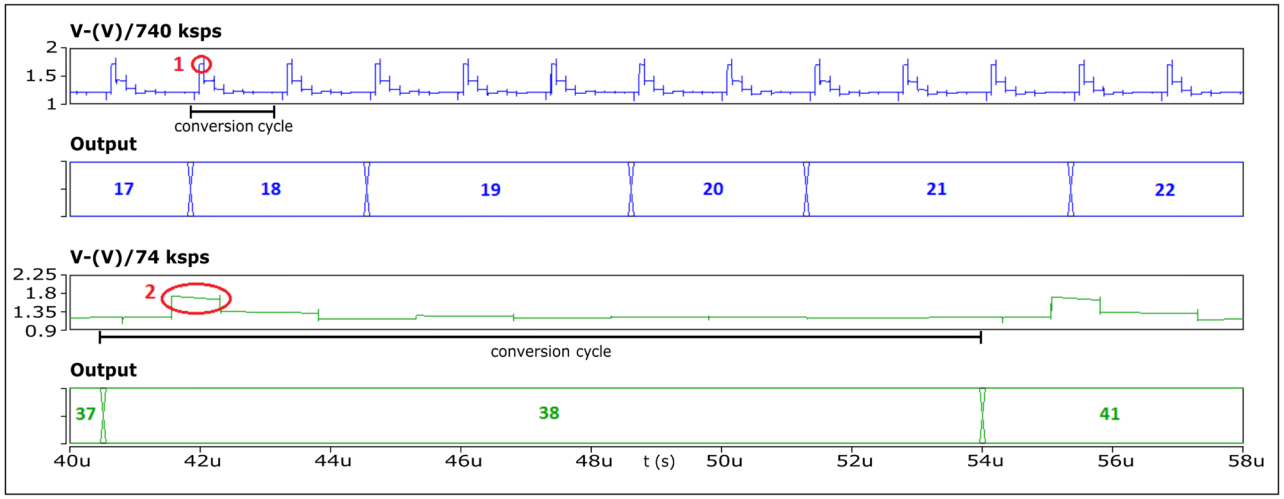
The converter operating with higher sampling rate (SAR@740) was simulated with the same leakage model and input signal. Similarly to which was observed in the gamma radiation experiment, the functional degradation is not significant, if compared with the errors observed for the slower converter, as can be seen by inspection in Fig. 12.

Simulation results allow us to explain why the slower converter showed a higher degradation in the gamma radiation experiment, despite both were submitted to the same conditions and total dose. The same explanation applies to justify the high lifetime of the SAR@740 converter if compared with the slower counterpart under X-ray irradiation. With lower sampling frequency, more time is spent between the decision of each bit value during the charge redistribution phase. Therefore, more charge is allowed to leak from/to the capacitors, increasing the error at the voltage delivered to the comparator at the decision instant of each bit.

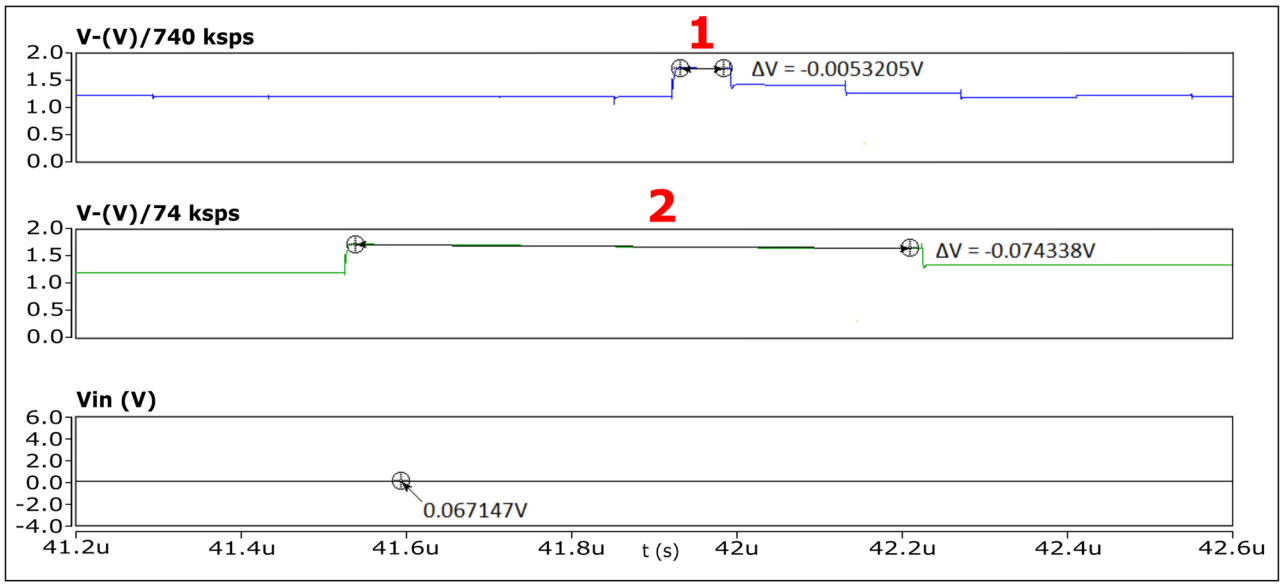
The voltage at the comparator non-inverting input ($V\_$) of both converters, as well as the converter output values, are shown in Fig. 13a. At the instant represented in the figure, the value of the ramp input is 67.1 mV, when simulation time is near 42 μs. This voltage should be converted to a decimal value of 14 in an ideal 8-bit ADC (with $V_{REF} = 1.2$ V). The converted values are 18 and 41 (SAR@740 and SAR@74, respectively), showing a higher and severe degradation in the slower converter.

Figure 13b highlights the conversion of the most significant bit (MSB) (first step of redistribution phase) to the same samples shown in Fig. 13a. It can be seen, in Fig. 13b, that the total voltage drop at the capacitors ($V\_$ node) is significantly lower (5 mV) in the faster converter than the drop observed for the slower SAR (74 mV). Such effects continue to happen until the least significant bit is obtained, contributing to the overall error of the converted sample.

The observed results allow to point out mitigation strategies to enhance lifetime of SAR ADCs in radiation environments. If a commercial device is considered, the system designer may chose to use the higher possible sampling frequency, in order to reduce the leakage impact on the voltage under comparison. Of course this will increase the power consumption and generate a higher amount of data (a decimation strategy may be adopted in the signal processing unit). Therefore, the system designer must evaluate the benefits and drawbacks of using oversampling. For the designers of SAR ADCs, replacing some specific transistor of the switching array by Enclosed Layout Transistors (ELT) may be a suitable alternative to enhance TID robustness of SAR ADCs.



(a)



(b)

Fig. 13 **(a)** Simulation of internal voltages of capacitor top plates($V\_$) of SAR@74 and SAR@740 converters and output converted values (decimal); and **(b)** Voltage drop at $V\_$ node caused by leakage in both converters during decision of MSB, for V_{IN} = 67.1 mV and V_{REF} = 1.2 V

6 Conclusion

In this work, the radiation response of two identical charge redistribution SAR ADCs operating at distinct sample frequencies is investigated. Results of a gamma radiation experiment showed a significant linearity degradation in the converter operating at lower sampling frequency (74 ksps), while the faster converter (740 ksps) showed an almost imperceptible degradation. Another experiment, with a high dose rate X-ray source, also showed that the linearity degradation starts to occur for a lower dose value in the slower SAR converter. In addition, the lifetime under X-ray radiation of the slower converter was lower, if compared with the converter operating at higher sampling rate.

By means of SPICE simulation of a SAR converter designed in the same technology node than the irradiated devices, the main failure mechanism observed in practical experiments is elucidated. The observed behavior in the gamma radiation experiments was reproduced quite similarly in simulations.

Results allowed us to conclude that the degradation is due to current leakage in a switch connecting the capacitor array (top plates) to the reference voltage V_{REF}. This causes charge to leak from/to the capacitors of the internal capacitive DAC of the SAR converters, generating a voltage error, which, in turn, causes decision errors on the binary search process.

This finding can help designers to select the transistors to be protected in radiation hardened converters, by applying layout techniques (Enclosed Layout Transistor, for example) only to the critical devices. It is possible that different designs present other critical switches that may be connected to the capacitor array. Therefore, the identification of such switches may be done by simple simulations, as proposed in this paper.

Another contribution of this work is to explain the dependency of the degradation severity with the used sample frequency. Smaller sample frequencies increase the total amount of charge flowing through the leakage paths (due to increase in conversion time). This way, when allowed by the power consumption budget, system designers may consider to adopt the highest possible sampling frequency when using charge redistribution SAR ADCs in radiation susceptible applications, even when the adoption of smaller frequencies is allowed by the signal bandwidth. Of course, in this case, the acquisition system must be adapted to deal with an oversampled signal.

Finally, this study also points that different sources of radiation and, mainly, different dose rates, may produce very distinct results regarding the total tolerated dose of the same system. This is attributed to self-annealing effects in low dose rate irradiation, and will be subject of further investigation in future works.

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Data Availability The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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