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An ATM Switch Model in a Hardware-Software Co-Design Environment

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An ATM Switch Model in a Hardware-Software Co-Design Environment

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Abstract

This paper presents a design methodology that allows to generate a C/VHDL system model using the Ptolemy environment. The first step is to generate a model for the whole system using the SDF/DDF domains. This model is easy to obtain, fast to simulate and replaces the C model that many system designers usually develop to describe the system's behavior. Next, the system is partitioned into a hardware implementation part and a software implementation part. Each part is described in the VHDL and CGC code generation domains respectively which allow the corresponding VHDL and C descriptions to be automatically derived. Each description may be separately inserted in the whole model, replacing its corresponding SDF/DDF original one. This permits the whole system to be co-simulated. At the end of this process a full C/VHDL model is obtained which may be co-simulated using the gcc compiler/Synopsys simulation tool environment. This C/VHDL description also serves as input to a hardware/software co-design tool. An important aspect of this gradual transformation of a SDF/DDF model into a C/VHDL model is that different partitions may be tried in a short time. An ATM switching system was used as a benchmark of this methodology.

Keywords: *ATM switch, RCube router, Ptolemy environment, system description, system simulation.*

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1. INTRODUCTION

In recent years, there has been a trend in microelectronics towards complete integrated systems on Silicon, composed of millions of transistors. However, designing such complex circuits has been increasingly difficult. The existing layout, logic and high level synthesis CAD tools, although helping to increase the designers' productivity, are not sufficient to produce high performance devices.

A new set of system level CAD tools [KA93], [KÇÜ95] are being investigated in order to help designers to obtain either hardware or hardware/software implementations of complex systems. These CAD tools allow designers to describe the system at the "system abstraction level", in contrast to the "RTL abstraction level" required for high level synthesis [GAJ92]. Such a representation may be simulated to prove its correctness at a very high level. A few CAD environments also contain tools that are able to partition the system into a mixed hardware/software solution [KA93]. These CAD tools may become the front end of future "integrated system synthesis environments". Ptolemy [BER96] is one such environment consisting of a large set of CAD tools and libraries that allow a designer to describe and simulate complex digital systems.

In [ARU97] we presented a system level model of an ATM switch using the Ptolemy environment. In that model we described the data flow behavior of ATM cells, representing their static flow across the switch, from an input to an output port. The model was entirely described using the synchronous data flow (SDF) Ptolemy domain.

In this paper we present an extension of this model, incorporating the dynamic behavioral features of the cell flow. The full ATM switch description required the interaction between two Ptolemy domains: SDF and dynamic data flow (DDF). A large set of simulations validated this complete model. Two other Ptolemy domains, CGC (a C code generation domain) and VHDL (a VHDL code generation domain), were also tested for their code generation and co-simulation properties.

Based on this study case, we propose a system design methodology in which a mixed SDF/DDF system model is gradually converted into a C/VHDL model that may be co-simulated (gcc/Synopsys environment) and used as input of a hardware/software co-design environment. This methodology has the following advantages: 1) both C and VHDL codes are automatically generated by Ptolemy and, 2) different system partitions may be tested in a short time.

In section 2 we review the ATM switch specification. In section 3 we briefly explain the several ATM cells flow paths across the ATM switch, which corresponds to the system's behavior that was captured using Ptolemy. In section 4 we give a brief overview of some relevant characteristics of the Ptolemy CAD system. In section 5 we present the co-simulation results of the full SDF/DDF model as well as of three other pairs of domains: C/SDF, VHDL/SDF and C/VHDL. In section 6 we propose a system design methodology based on Ptolemy and in section 7 we present our conclusions.

2. ATM SWITCH SPECIFICATION

A block diagram of a four ports ATM switch is shown in Figure 1. The physical line interface (ILF) is based on the UTOPIA standard. The ILF decouples the line rate from the ABSE's clock rate. The ATM basic switching element ABSE may interface to the ILF either by 8 bits data transfers (suitable for line rates up to 155 Mbps) or by 16 bits data transfers (suitable for line rates 622 Mbps or higher). The PCI and RCube interfaces manage the communication between the ATM switch and the host computer and the RCube router respectively. The RCube interface also provides the initialization of the RCube router. The RCube router is a fast switching engine developed in France [MASI96]. The VRAM memories store traffic control data, routing data and management data. Each ABSE module performs all the other ATM switch functions. An ATM switching system is composed of one or more ATM switch modules plugged into the standard PCI slots and interconnected by high-speed serial links. This system will be used in high-speed local area networks.

An ATM switch transfers ATM cells from an input port to one or several output ports at very high speed (155 Mbps or higher). An ATM cell consists of 53 bytes divided in two parts: a payload of 48 bytes (384 bits) and a header of 5 bytes (40 bits). The header consists of 6 fields: Generic Flow Control GFC (4 bits), Virtual Path Identifier VPI (8 bits), Cell Loss Priority CLP (1 bit), Payload Type PT (3 bits), Virtual Channel Identifier VCI (16 bits) and Header Error Control HEC (8 bits). At the physical layer, ATM cells are transmitted as a stream of bits. Our ATM switch is capable of performing the following functions: conversion of the incoming (high speed) bit stream into bytes; splitting the sequence of bytes into payload and header bytes; separation of ATM cell header fields, namely: VPI, VCI, CLP, PT, GFC and HEC; identification of user signaling cells and management cells; traffic control by means of the leaky-bucket algorithm [ETN96], monitoring both peak and average cell rate violations; generation of cell destination header and insertion of its time stamp, management of physical multicast operations (8 ports maximum); insertion of routing data required by the RCube router and adaptation of the cell flow to the RCube format (*flit* encoding) [MASI96]; multi-class quality of service management; statistical data generation (cell loss rate and others). More information about the ATM switch may be found in [HSS96].

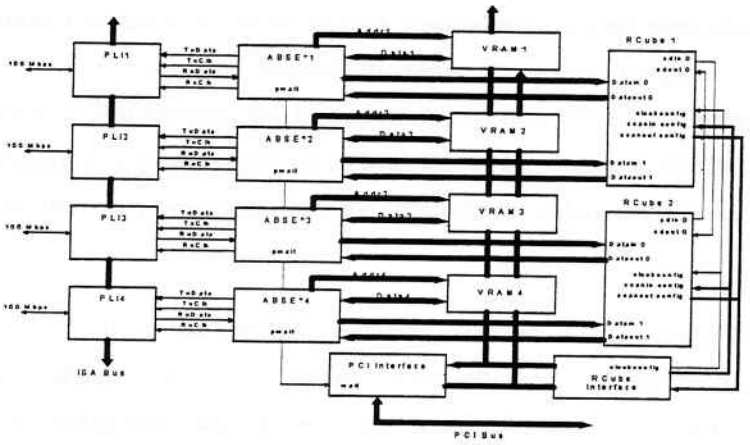

Figure 1 - A simplified block diagram of a 4 ports ATM Switching Module using the parallel RCube's inputs

3. ATM CELLS FLOW ACROSS THE ATM SWITCH

In [ARU97] we presented a model that described the flow of non-terminal ATM cells from an input to an output port. We will designate such flow as fundamental behavior of the ATM switch. Analyzing the flow of ATM cells across the switch, shown in figure 1, we identified 37 possible paths, depending on the cells' header information. The fundamental behavior accounts for 10 of these paths.

The model presented in this paper incorporates the following new features: the management of the physical multicast operation (8 ports maximum); the VRAM memories management; the terminal cells control (changing the header's VCI parameter). The incorporation of these features accounted for the 27 remaining cells' paths. A detailed description of the ATM cells' flow behavior can be found in [HSS96].

3.1 ATM Cells Fundamental Behavioral Description

The fundamental behavior refers to the flow of ATM non-terminal cells, i.e., cells whose final destination is not directly connected to the switch. Such cells arrive at the ILF, go through the ICF, pass the traffic control, get a new header with a new VPI, are routed just once through the RCube (unicast cell) and are placed in the multi-class output buffer waiting to be sent over the physical line. A detailed description of this behavior, using the SDF Ptolemy domain, was presented in [ARU97]. This behavior accounted for 10 possible cells' paths.

3.2 The Multicast Operation Control

An ATM cell will be sent to more than one destination in the network (multicast cell) when a flag (F_MC) is on. In this case the 3 bits signal "QPM" indicates how many ATM cells will be send to the RCube router. All these signals come from the routing memory. This behavior creates different cell headers for the same payload. The multicast operation can only be executed for a maximum of 8 different destinations. This behavior adds 9 ATM cell new possible paths.

3.3 Management Memory Control

The management memory implemented in the ATM switch, stores the statistical data generated in the system. There are 10 types of data as the number of discarded excessive cells, the number of routed cells, the number of discarded invalid VPI cells, etc. Each type of management data is stored in a specific memory address. When a statistical information is generated by the system, its type is identified, its previous count is retrieved, incremented and stored back in the same address. This behavior accounts for 10 ATM cells paths.

3.4 Terminal Cells Control

If the VPT flag, stored in the routing memory, indicates that a cell is terminal, the ATM switch will insert a new header composed of new VPI and VCI fields. In order to create these header two different data, stored in different parts of the routing memory, have to be retrieved. Furthermore the new VCI value must be validated by checking a flag stored in the routing memory. If it is not valid, the cell has to be discarded. This behavior adds 8 ATM cell paths.

4. THE PTOLEMY SYSTEM

Ptolemy is a compact software infrastructure upon which specialized design environments, called domains, can be built [BER96]. The software infrastructure, called Ptolemy kernel, is made up of a family of C++ class definitions. Domains are defined by creating new C++ classes derived from the base classes in the kernel. Ptolemy allows to build complex systems using a hierarchical composition (nested tree structure) of simpler subsystems. The whole system is called the universe. A domain models each subsystem. A subsystem, also called a galaxy, can internally use a different domain than that of its parents or children. In this case we use targets to define the parents domain. In order to mix domains it is necessary to ensure that the interface, called a wormhole, is compatible, so the child galaxy obeys the semantics of the parent domain. The Ptolemy system uses the usual data flow terminology where, actors are called stars, tokens are called particles and the invocation of the go() method of a star is called a firing. The connection between two different stars or galaxies is called arc. When a star fires, it consumes a number of particles from its input arcs, and produces a different number of output particles.

4.1 PTOLEMY DOMAINS

Domains can operate in any (or all) of three modes. *Simulation,* where a scheduler invokes code segments in an appropriate sequence; *code generation*, where code segments in an arbitrary language are stitched together to produce one or more programs that implement the specified function and; *compilation*, where the specification is analyzed and translated into optimized code in any target language.

The computations can be performed using one or more implementation languages, such as C++, C, MATLAB, and VHDL. A target coordinates the scheduling and implementation of algorithms described in a particular domain. As part of the coordination, a target may provide an interface to software (compiler, assembler, simulator, etc.) or hardware. Wormholes and targets must be used in order to define the relationship between the child and the parent of mixed domains.

4.2 THE SDF, DDF, CGC AND VHDL DOMAINS

The synchronous data flow (SDF) domain (data flow semantics) is used for signal processing and communications algorithm development. The predictable control flow of SDF allows for efficient scheduling, but limits the range of applications. A dynamic data flow (DDF) domain extends SDF by allowing data-dependent control flow. To support broader applications, the DDF domain uses dynamic (run-time) scheduling. For long runs, involving many interactions, this is more expensive than the static scheduling that is possible with SDF. It supports conditionals, data-dependent iteration, and true recursion.

The CGC domain is a code generation domain. The simulation in this domain uses commercial C compilers like GNU or "gcc" in Sun stations. This domain translates a simpler code, written in the "Ptolemy Language" into a more complete C code.

The VHDL domain generates code in the VHDL programming language. This domain supports the synchronous data flow model of computation. Ptolemy provides several VHDL targets as SimVSS-VHDL for simulation using the Synopsys VSS VHDL simulator.

5. EXPERIMENTAL RESULTS

5.1 Complete Model of the ATM Switch

The fundamental ATM switch behavior, fully described in the SDF domain, consists of a large amount of sequential operations. The ATM switch model (universe) is composed of the several galaxies. A source of ATM cells provided a model for the physical line, generating the 40 bits of the header. This source accepts the GFC, VPI, VCI (minimum and maximum), PT and CLP as decimal parameters and generates these fields as a bit stream (from MSB to LSB) [JAL95]. This model was presented in [ARU97].

A - Multicast operation control

The multicast behavior, described in section 3.2, required the description of a recursive procedure. There is a variable number of control signals (represented as particles) during each interaction. The DDF domain is well fit to describe such behavior [BER96]. The "REPEATER" control star from the Ptolemy library was combined with other library stars as well with a few customized stars in order to model this behavior as shown in figure 2a. This new DDF galaxy was joined with the existing SDF galaxy that describes the fundamental behavior, shown in figure 2b, through a customized wormhole (figure 2). The target of the DDF galaxy points to the parent domain, which is SDF.

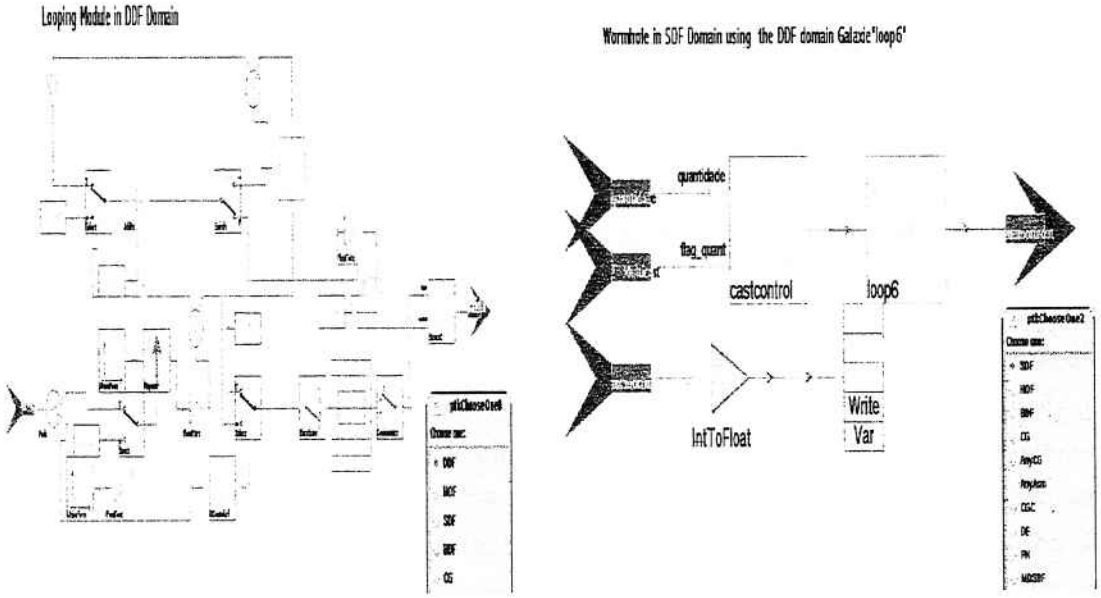

Figure 2 – Wormhole DDF/SDF a) DDF galaxy inside the wormhole, b) SDF galaxy outside the wormhole

B - Management Memory Control

The management data are stored in a 16-address memory, built from a pair of 8 address modules, as explained in [ARU97]. In order to implement the behavior described in section 3.3, we described a SDF galaxy composed of both customized and library stars. Figure 3 shows some simulation results of the management memory control.

C - Control of Terminal Cells

In order to implement the behavior described in section 3.4, we built decision forks using some DDF *IF-THEN-ELSE* stars. This type of dynamic control is best suited to describe this type of command. The control of terminal cells was finally described as a set of DDF galaxies, all of them containing the *IF-THEN-ELSE* stars. SDF-DDF wormholes, like the one shown in figure 2, were used to build the complete model shown in figure 4.

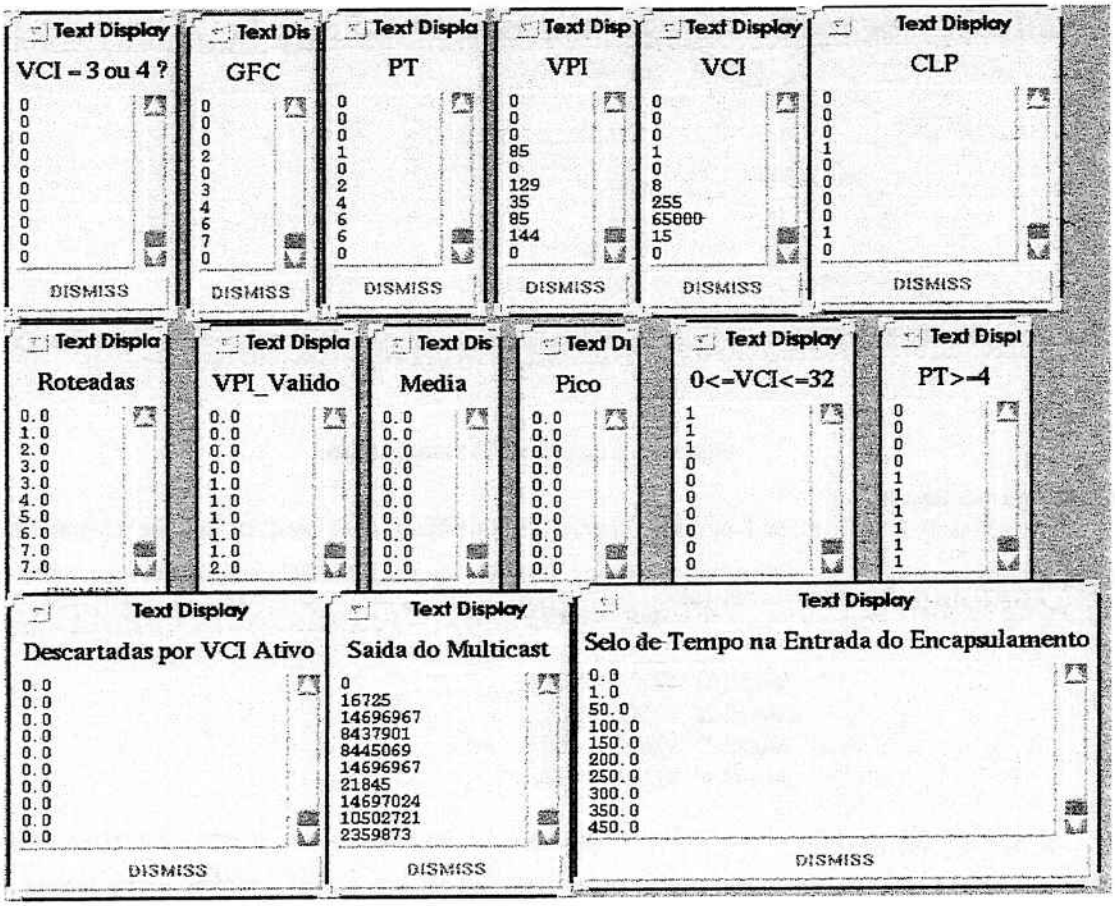

Figure 3 - Output of the management memory

D - Simulations of the complete model

The simulations were performed hierarchically. We first validated individual stars, both primitive and customized. Then each galaxy, either SDF or DDF were tested and validated. Finally, the whole model was simulated, verifying destination cell headers and counting the routed and the discarded cells. We also simulated the reasons why some cells were discarded, by retrieving the corresponding data from the management memories.

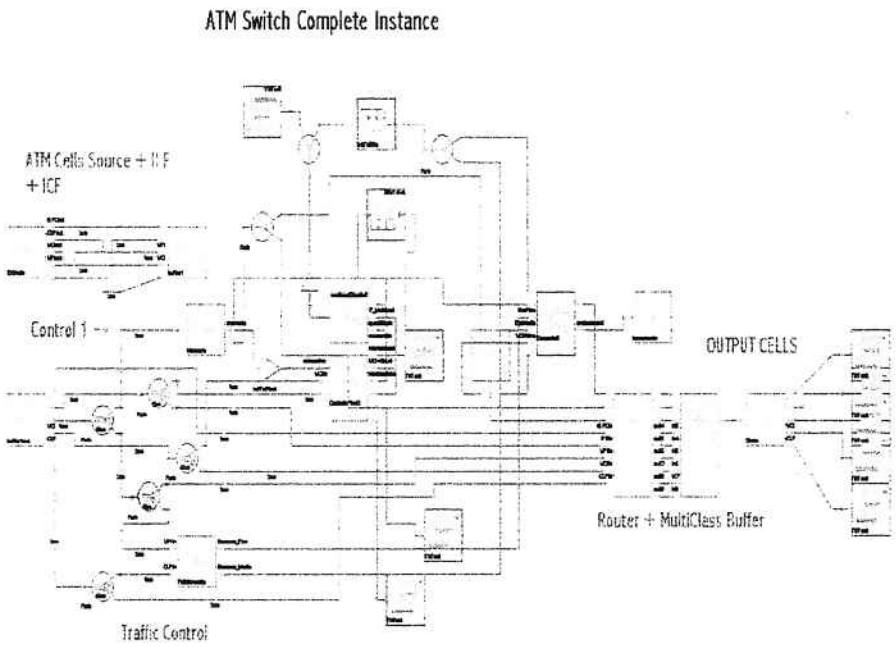

Figure 4 - Complete ATM switch model

5.2 Co-Simulation Results

The physical line (ILF) and physical layer (ICF) interfaces were used to test the co-simulation characteristics of several Ptolemy domain combinations. The following four ILF/ICF models were generated:

ILF - ICF

Model 1: SDF - SDF
Model 2: CGC - SDF
Model 3: VHDL - SDF
Model 4: VHDL - CGC.

All models were described in the Ptolemy language. All descriptions were composed of primitive and customized stars and galaxies. The number of primitive stars and galaxies varied according to the domain due to the differences among their libraries.

Simulations were performed using the Ptolemy software for the SDF model, the "gcc" compiler for the C code and the Synopsys simulation tool for the VHDL code. The simulation of model 1 and the co-simulations of models 2 and 4 were fast and efficient. The co-simulation of model 3 was very slow due to incompatibilities that exist between the VHDL and the SDF domains. The latest Ptolemy version (Version 0.7) eliminated this co-simulation capability from the system. Models 2,3 and 4 made use of the two code generation domains, CGC and VHDL. Both the C code as well as the VHDL code was simulated as they were, meaning that the generated codes are compatible with the simulation tools. Part of the generated code, for both C and VHDL, was specified by the designer as a *pragma*, meaning that the code generation process does not changed them. This feature allows the designer to introduce code constraints. However the VHDL code was not ready for an architectural synthesis based on the Synopsys tool.

6. System Design Methodology

A system design environment should assist a designer to quickly generate a system model that may be validated and used as an input description to a hardware/software co-design environment. Such an environment present two problems that have been addressed in many recent publications: 1) how to partition the system into a hardware and a software part, and 2) how to co-simulate these parts which are described in different languages. It is our opinion that it is very difficult to automatically find an optimal partition of a system. Therefore we believe that an environment that allows a designer to quickly describe, and simulate different partitions is the best solution to assist system designers.

Based on the study case described in this paper, we devised such a design methodology using Ptolemy.

The methodology starts by creating a system model using the SDF and DDF domains. These are the most mature domains in Ptolemy and are well suited to describe both the data and the control flow features of digital systems. This step replaces the C model that many system designers produce in the beginning of any project. Next, a set of behavioral test vectors are derived and used to validate the model. This model may be partitioned into hardware and software implementation parts. The CGC domain is used to model the C part. The automatically generated C code may be co-simulated with the original SDF/DDF code of the other part of the system, using the same test vectors. The VHDL domain is next used to model the hardware implementation part. The automatically generated VHDL code is combined with the previously generated C code, resulting in a full C/VHDL system description. This model may be once again co-simulated using the same test vectors. The partition between hardware and software of the entire model may be manual or automatic. The incremental nature of this methodology allows for a fast and correct development of the C/VHDL system model. Consequently different partitions may be generated and tested in a short time. The resulting C and VHDL codes are well suited to be used in conjunction with commercial synthesis tools like the Synopsys Behavioral Compiler and the C compiler for the Motorola DSP56X [BER96].

7. CONCLUSIONS AND FUTURE WORKS

7.1 ATM Switch Complete Model

In this paper we described a complete model of an ATM switching system. The model required the combination of two Ptolemy domains: SDF and DDF. The SDF domain described the static characteristic of the ATM cells behavior while DDF was used to describe the dynamic behavior of these cells. The model made use of some primitive stars from the Ptolemy library, combined with some customized stars developed for this model. The "IF-THEN-ELSE" and "LOOP" behavior were described as DDF galaxies, also composed of primitive and customized DDF stars. A DDF/SDF wormhole was developed in order to joint the DDF galaxy with the SDF model. The complete ATM switch model was easy to build and to simulate, due to the large number of primitive stars in both the SDF and the DDF domains. The biggest effort was spent to build and test the SDF/DDF wormholes. We simulated the whole model for all 37 possible paths followed by ATM cells across the switch. By changing the ATM cells headers we were able to simulate terminal and non-terminal cells

routed to the output ports, discarded ATM cells due to traffic control violations and other features of the whole system [JAL95].

7.2 System Design Methodology within the Ptolemy Environment

Based on the ATM switch system study case, we proposed a digital system design methodology well fit for a hardware/software design environment, taking advantage of four Ptolemy domains: SDF, DDF, CGC and VHDL. The methodology has the following characteristics: 1) Both the C and the VHDL codes required by the hardware/software co-design synthesis tools are automatically generated, and 2) a designer may quickly evaluate different system partitions.

The methodology consists of first creating a complete system model using the SDF/DDF domains. These domains are the most mature and well documented among all Ptolemy domains. After validating this model, the system is partitioned into hardware and software parts. The software part is described in the CGC domain and the hardware part in the VHDL domain. Both are code generation domains that automatically generate C and VHDL. In both cases *pragmas* may be introduced by the designer in order to specify part of the final code. First, the resulting C code is mixed with the original SDF/DDF model and validated by co-simulations. Finally the resulting VHDL code is combined with the C code and once again validated by co-simulations, using the gcc compiler/Synopsys simulation tool. This C/VHDL code may also be used as input to the synthesis tools present in the Hardware/Software co-design environment.

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