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RESEARCH ARTICLE

Enhancing Microgrid Protection With Impedance-Based Blocking: An Embedded Validation on a Dual-Layer Architecture

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ABSTRACT Integrating microgrids has posed many challenges for distribution systems. Due to bidirectional power flow and intermittence of some renewable sources in microgrids, conventional protection methods are prone to failure. Aiming at improving them, this paper proposes a new blocking strategy to enhance dual-layer protection of the microgrid. The first layer contains the conventional overcurrent protection and the internal protection of the distributed energy resources (DERs). The second layer uses undervoltage logic and operates in the event of a possible failure or delayed operation of first-layer devices. As the undervoltage used in the second layer may present problems with selectivity losses, an impedance-based blocking strategy was proposed to mitigate it. Intelligent electronic devices close to the DERs receive voltage and current phasors, allowing the estimation of the impedance value used in the blocking strategy. The proposed protection scheme was firstly validated in a simulation environment using more than 10,000 simulated fault cases. Subsequently, an analysis was carried out on conventional and dual-layer protection with and without impedance blocking in a real-time hardware-in-the-loop test, where the proposed protection was embedded in hardware. The proposed approach not only outperformed conventional strategies in both analysis but also enhanced microgrid protection. Overall, the proposed dual-layer protection with impedance blocking reduced both the maximum clearing time and the occurrences of selectivity losses, while increasing the accuracy.

INDEX TERMS Hardware-in-the-loop, impedance blocking, microgrid protection, overcurrent protection, real-time simulation, undervoltage protection.

I. INTRODUCTION

Distribution systems have undergone notable changes due to microgrid incorporation in recent years. These microgrids facilitate the integration of local loads and Distributed Energy Resources (DERs) such as wind, solar, and energy storage systems. However, the intermittent nature of some of these DERs and fluctuations in short-circuit current levels, caused by whether the microgrid is connected or islanded, poses new challenges for conventional protection systems.

Many microgrid protection propositions have emerged based on facilities provided by smart grids, utilizing network monitoring with phasor measurement devices (PMDs). Therefore, some papers proposed more conservative techniques based on state estimation using synchrophasors [1], [2], [3]. Nonetheless, other researchers endorse fault detection through different routes, such as voltage and frequency analysis [4], voltage phase angle rate changes [5], active power differential estimation using voltage synchrophasors [6], integrated impedance angles [7], magnitude and angle analysis in the impedance plane [8], and a multi-agent system based on current phase angle variations [9]. Despite their originality, these approaches have a common drawback of requiring multiple measurement devices, which must be installed in all buses for some of these strategies. Except for [9], the mentioned proposed microgrid protection

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strategies used few fault scenarios to evaluate their effectiveness, leading to a lack of quantitative and statistical analysis of their operation. Furthermore, their centralized nature might lead to additional infrastructure costs and a failure in communication that could leave the system unprotected.

Decentralized protection schemes are proposed as an alternative to overcome some of the challenges of the centralized approaches aforementioned. Liu et al. [10] presented a protection scheme based on the Park Transform for inverter-dominated microgrids. By using the Discrete Wavelet Transform (DWT), the signals were downsampled, and noise introduced by inverter switching was removed. The decision logic utilized the energy of the DWT spectrum and a fixed threshold. Despite the methodology yielding good results, only four fault cases were evaluated.

Mohanty et al. [11] presented a current-restrained undervoltage protection for inverter-dominated microgrids. Additionally, the inverter control was modeled to reduce its current injection during undervoltages. The protection schemes utilized the positive sequence voltage and current for the tripping logic. Although the proposal proved to be effective in both connected and islanded modes, the validation was once again performed for only a few fault cases.

A microgrid protection based on the rate of change of voltage was proposed by Dawoud et al. [12]. This proposal aims to coordinate primary and backup protection by adjusting the time dial, pickup values, and parameters of the inverse time curve. Two adjustment sets were created for islanded and connected modes, optimizing their values for each condition. The methodology demonstrated adequate performance for microgrid protection in the analyzed scenarios. Nonetheless, only three-phase faults with 0 Ω and 30 Ω fault resistances were considered in the tests.

Finally, a dual-layer microgrid protection was proposed by Menezes et al. [13], combining conventional overcurrent (OC) devices and undervoltage protection. The proposed approach used only three PMDs to monitor the microgrid and perform its protection. Even though the proposal achieved high accuracy, it presented some selectivity problems due to the non-directional nature of the undervoltage protection. Moreover, no hardware-in-the-loop implementation was presented in the paper.

Several decentralized schemes for microgrid protection have been proposed in the literature. Review studies can help identify additional approaches, including machine learning-based strategies [14], adaptive protection schemes [15], [16], and multi-agent systems [17].

The decentralized structure presents a lower implementation cost in comparison with the centralized one and requires a low bandwidth communication infrastructure. Moreover, the parameterization of decentralized protection was faster and more straightforward. Finally, as all measurements and processing were carried out locally, there was no need for measurement synchronization. Additionally, these proposals are based on voltage measurements, which are less prone to fail than the conventional OC protection during the drastic changes of short-circuit levels in the microgrid between grid-connected and islanded mode. Nevertheless, as the protection algorithm was running locally, the device processing capacity could be a limiting factor when using this protection strategy. Therefore, the protection schemes need to be compatible with the hardware used for their implementation.

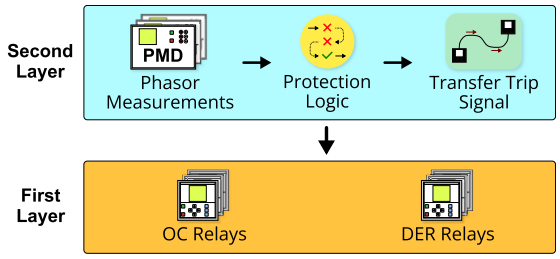


FIGURE 1. Structure of the dual-layer microgrid protection.

Following the above-mentioned context, this paper proposes an impedance-based blocking strategy to improve the dual-layer protection proposed in [13]. In addition, the impedance blocking scheme enhances the selectivity of the protection while keeping the clearing time relatively unaffected. Thus, the main contributions of the present paper are:

- A refined protection scheme, based on impedance blocking, characterized by high accuracy and reliability across both operating modes of the microgrid;
- Local computation of all decisions, eliminating the need for synchronized measurements;
- A streamlined requirement for measurement devices within the microgrid;
- A hardware-in-the-loop analysis proved the effectiveness and applicability of the proposed protection scheme.

Next, Section II describes the proposed protection strategy. The results are presented in Section III. Finally, Section IV summarizes the conclusions.

II. DUAL-LAYER MICROGRID PROTECTION

The dual-layer microgrid protection was put forward by the authors in [13]. This proposition relies on undervoltage, which is less influenced by the significant variations in short-circuit levels within the microgrid, particularly during transitions from grid-connected to islanded mode.

Regardless, this paper proposes the addition of an impedance-based blocking strategy to enhance the microgrid protection performance. The dual-layer design takes advantage of the conventional devices that would be already installed in the system. The structure of the dual-layer approach is shown in Fig. 1. Each layer will be explained in the following subsections.

A. FIRST LAYER

This layer comprised conventional protective devices, including the OC relays with inverse time characteristic and internal protection of the DERs. To ensure that the OC protection would not operate during reverse power flow,

its operation used directional blocking to operate only for faults inside its protection zone. The overcurrent inverse time characteristics are established by international standards [18], [19]. Considering a pickup current I_p and the measured current I, the tripping time can be calculated as:

$$t = \frac{DT \cdot \beta}{\left(\frac{I}{I_p}\right)^{\alpha} - 1}, \tag{1}$$

where the values of DT, β and α are all defined by the standards.

Regarding the internal protection of the DERs, the protection functions were modeled based on the recommendations in [20]. Additionally, the primary and backup protection were coordinated using a minimum time of 0.3 s.

B. SECOND LAYER AND IMPEDANCE BLOCKING

The second layer was configured to have a delayed operation in comparison to the first layer. It allowed the primary and backup protection inside the first layer to operate, using a minimum time delay of 0.6 s. Therefore, in case a device in the first layer failed or took longer than 0.6 s to operate, a device in the second layer would operate. Each device in the second layer sent a remote trip signal to an associated circuit breaker to isolate the fault, if necessary.

The decision process in the second layer was based on the inverse time undervoltage, which operated faster for severe undervoltages. Each intelligent electronic device (IED) in the second layer received voltage and current phasors from PMDs strategically installed in the microgrid. As these phasors were used locally and did not have to be compared to phasors from another bus in the system, they did not need to be synchronized to a fixed reference.

The undervoltage strategy requires a threshold (V_{pickup}) that is compared with the voltage synchrophasors (V_{ph}), considering the nominal system voltage as a reference (V_{ref}). Then, using a standard inverse-time curve [18], [19], the trip time (t_{trip}) is calculated as shown in (2) and (3):

$$M = \frac{V_{pickup}}{\left(\frac{V_{ph}}{V_{ref}}\right)}, \tag{2}$$

$$t_{trip} = \frac{DT\,\beta}{(M^{\alpha} - 1)} + L, \tag{3}$$

where, the values of α, β, and DT are defined by the inverse-time curve, and L can be adjusted to specify the minimum trip time of the curves.

To ensure the correct selectivity of the IEDs close to DERs, an impedance-based blocking was proposed. The proposed blocking region was based on where the impedance from the DER would be for normal operating conditions, thus preventing/delaying the operation of the protection close to DER. The impedance plane of the blocking strategy is shown in Fig. 2.

It can be observed that the non-tripping zone is a well determined area, and it is defined by three parameters, that are:

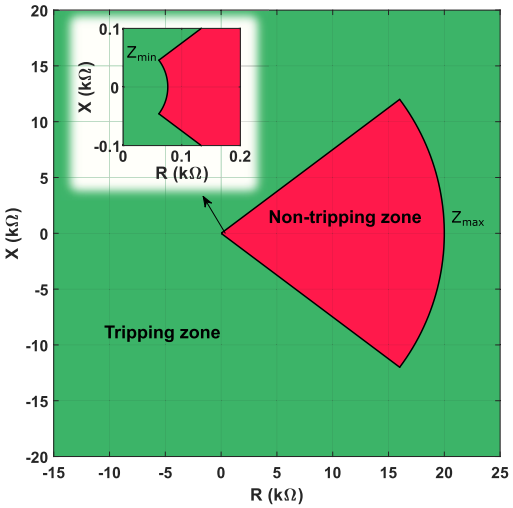


FIGURE 2. Impedance-based blocking strategy.

- Z_{min} – the minimum impedance considered as a normal operating condition;
- Z_{max} – the maximum impedance, which allows the tripping for low power injection or disconnection of the DER;
- PF_{min} – the minimum power factor expected for a DER, which defines the angle of the non-tripping zone.

Changes in power injection can also cause significant changes in the measured impedance. Therefore, the Z_{min} value was adaptively updated regarding the injected power. As the voltage and current phasors were available, the injected power S was calculated. Thus, the value of Z_{min} can be computed as:

$$Z_{min} = \frac{{V_{nominal}}^2}{OL_{max} \cdot S}, \tag{4}$$

where OL_{max} defines a maximum overload to be considered as a normal operating condition, while $V_{nominal}$ represents the nominal line voltage.

Regarding the impedance estimation, the apparent impedance Z_a can be approximately calculated by:

$$Z_a \approx \frac{V_1}{I_1} - \delta \cdot R_p. \tag{5}$$

where V_1 and I_1 are the positive sequence of voltage and current phasors, respectively; the phase resistance (R_p) is the real part of the phase impedance that can be obtained from V_p/I_p, which are the phase voltage and current; and δ is a free parameter used to adjust the phase resistance. Thus, δ is experimentally adjusted based on high resistance values for single-phase faults at the end of the protection zone. This is to enhance the performance of the protection during unbalanced faults, assisting the impedance in migrating to the tripping zone within a desired time. From Z_a calculation, the proposed approach provided an approximation for the apparent impedance that did not require fault classification, as it is usually needed for estimation.

Disturbances in the measured signals, such as noise, harmonics, and exponentially decaying DC components,

can cause errors in the impedance estimation process. Therefore, the PMD must have a filter capable of mitigating these disturbances to ensure the phasor estimation accuracy. In this paper, the PMD used a moving average-based filter to mitigate the DC component, which was proposed and validated in software and hardware by the authors, as demonstrated in [21].

III. RESULTS

The European Medium Voltage Benchmark from CIGRÉ [22] was used as the test system to validate the current proposition. The base system was modeled with some modifications. First of all, the frequency was modified from 50 to 60 Hz. Then, a synchronous generator (SG) with 5 MVA was connected to bus 5. A photovoltaic generator (PV) and a battery energy storage system (BESS) were connected to bus 8, with a rated power equal to 1 MVA each. In addition, the second feeder was removed, but a load was connected to bus 0 with its equivalent power. This load was modeled to ensure the voltage level was close to the complete system. The SG operated with constant power injection when the microgrid was connected, and it changed to voltage and frequency control when the microgrid operated in the islanded mode. In contrast, PV always operated with constant power injection while the BESS operated with a droop control to provide voltage and frequency support. The test system is shown in Fig. 3 with all the protection devices and DERs. All the parameters from the system can be found in [22].

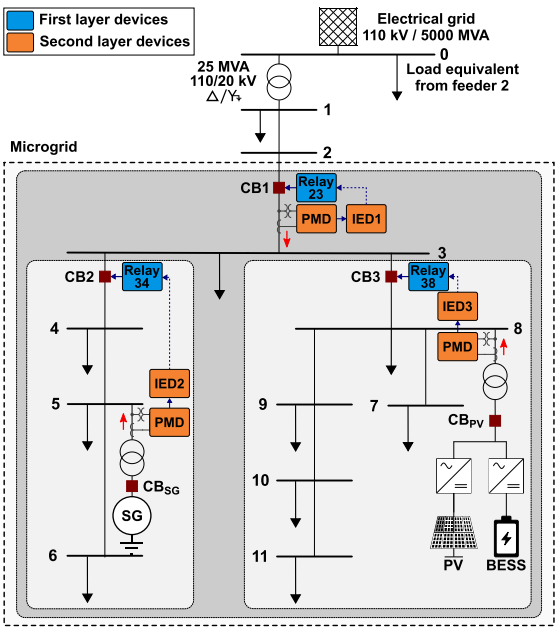


FIGURE 3. Test system with all DERs and protection devices.

The proposed protection scheme was thoroughly evaluated in a simulation environment to demonstrate its effectiveness. To validate its practical applicability, the scheme was also tested using a low-cost microcontroller in a hardware-in-the-loop (HIL) real-time evaluation. The results from both analyses are presented in the following subsections.

A. SIMULATION RESULTS

The test system was modeled in the software ATP/ATPDraw for all the analyses in the simulation environment. Three scenarios were designed to analyze the behavior of the proposed scheme under varying conditions, including fault location, type, resistance, microgrid connection status, and DER connection and output power. This resulted in a total of 10,395 fault cases. The parameters for these scenarios are summarized in Table 1.

TABLE 1. All the parameters for the simulated scenarios.

	Scenario 1	Scenario 2	Scenario 3
Fault types	All 11 fault types		
Fault resistance	0 Ω, 10 Ω, 20 Ω, 30 Ω and 40 Ω		
Fault locations	Buses from 3 to 11		
BESS status	Disconnected	Connected	Connected
Microgrid status	Connected	Connected	Islanded
DERs power output	100%, 75%, 50%, 25%, and 10%		
DERs disconnection	All DERs disconnected, SG disconnected and PV 100%, PV disconnected and SG 100%		–
Total cases	3,960	3,960	2,475

Out of the 2,475 simulated fault cases in Scenario 3, the internal protection of the DERs tripped in 2,417 cases within 0.6 seconds, which was faster than the second-layer devices could respond. Consequently, as the microgrid was islanded, the proposed dual-layer approach could not be analyzed for these cases, reducing the total number of evaluable cases to 58 (limited to three-phase faults with a fault resistance of 40 Ω). All fault simulations were conducted after the system had stabilized, with faults applied at 12 seconds. For clarity, clearing times presented in figures and tables were computed relative to the fault initiation time. A trip was considered successful if it isolated the smallest possible area and achieved a clearing time of less than 2 seconds.

Due to the difference in fault cases for each scenario, the average accuracy was used to measure the overall performance. Its value was computed considering the performance index for Scenarios 1, 2 and 3 (PI_{S1}, PI_{S2}, and PI_{S3}, respectively), as shown in (6):

$$Average = \frac{PI_{S1} + PI_{S2} + PI_{S3}}{3}. \tag{6}$$

The relays and IEDs were all configured considering the system in a radial configuration and without DERs. Relay 23 and IED1 were the backup protection for the first and second layers. IED2 and IED3 was able to send a remote trip for relays 34 and 38, respectively. Additionally, if the IED2 and IED3 tripped, they would also send a remote trip signal to the internal protection of the DERs within their protection zone. Regarding the position of the PMDs, they were strategically installed at the connection point of the microgrid and the DERs, as in [13], resulting in the installation of three PMDs. Table 2 presents the parameters for the OC relays, and Table 3 illustrates the parameters used for the second-layer devices.

All IED used extremely inverse time curves for their undervoltage logic. The pickup voltage (V_{pickup}) was defined by applying a 40 Ω three-phase fault at the end of the

TABLE 2. Parameters for the conventional OC relays.

Relay	I_{p51}	Curve	α	β	DT	I_{p50}/I_{p51}
Relay R23	181 A	Very inverse	1.0	13.5	0.125	5.7 pu
Relay R34	71 A	Very inverse	1.0	13.5	0.05	14.2 pu
Relay R38	89 A	Very inverse	1.0	13.5	0.05	11.4 pu

TABLE 3. Parameters for the IEDs in the second layer.

IED	V_{pickup}	DT	L	PF_{min}	OL_{max}
IED1	0.949523 pu	0.0035	0.850	–*	–*
IED2	0.928304 pu	0.0023	0.600	0.7	2.20
IED3	0.924904 pu	0.0023	0.625	0.7	1.25

* Not applicable to IED1, as the impedance blocking was used only for IED2 and IED3.

protected branch of each IED and using the residual voltage multiplied by a factor of 1.115, which increased the pickup voltage while maintaining it below 0.95 pu. This increased the protection sensibility for high resistance faults and avoided trips in undervoltage scenarios not caused by faults. Moreover, the δ and Z_{max} used for IED2 and IED3 were equal to 0.10 and 20 kΩ, respectively.

To illustrate how the proposed microgrid protection operates, two three-phase fault cases from Scenario 1 with 100% power injection were selected. The selection of these cases was merely visual, allowing the reader to see all phases changing during fault. The first case is a 10 Ω three-phase fault at bus 3, shown in Fig. 4. In this case, only conventional protection (first layer) was enabled to clear the fault. The currents and voltages were normalized using the pickup current from relay 23 and the nominal voltage from bus 3.

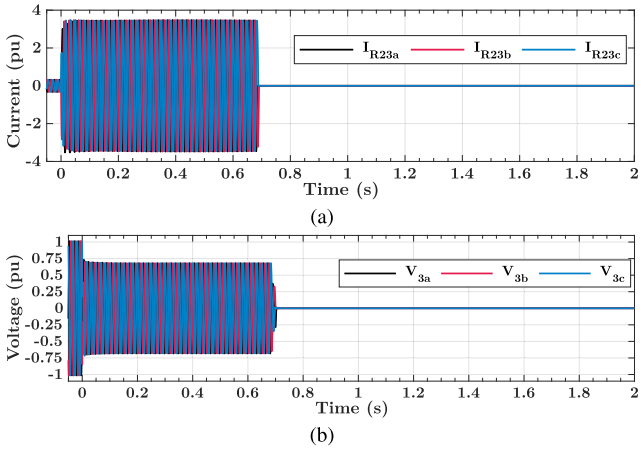


FIGURE 4. Current measured by relay 23 (a) and voltage measured at bus 3 for a 10 Ω three-phase fault applied at bus 3 (b).

In this case, due to the current level over three times the pickup current, the relay R23 successfully isolated the fault as the internal protection from the DERs also tripped. Fig. 5 presents the trip signal for the conventional protection and the proposed approach with impedance blocking.

With the dual-layer protection, the circuit breakers CB_2 and CB_3 would also operate to isolate the fault. CB_2 and CB_3 are not required to isolate the fault if all other circuit breakers can operate properly. Nonetheless, if some of them present, for example, a mechanical problem and cannot operate,

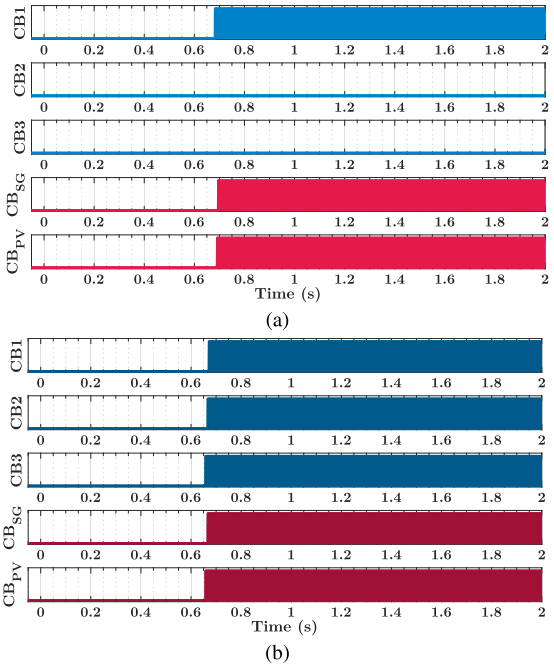


FIGURE 5. Trip signal for the (a) conventional protection, and (b) proposed dual-layer protection for a 10 Ω three-phase fault at bus 3.

the proposed protection would lead to better performance by sending a trip signal to open CB_2 and CB_3. This situation clearly demonstrates the additional reliability that the proposed protection scheme provides, ensuring fault isolation. Furthermore, the clearing time for this fault case would be similar to that for conventional protection.

In the sequence, the same fault case was analysed, but with a fault resistance of 30 Ω. Fig. 6 presents the current and voltage signals for this fault case. The trips for the conventional and proposed protection are illustrated in Fig. 7.

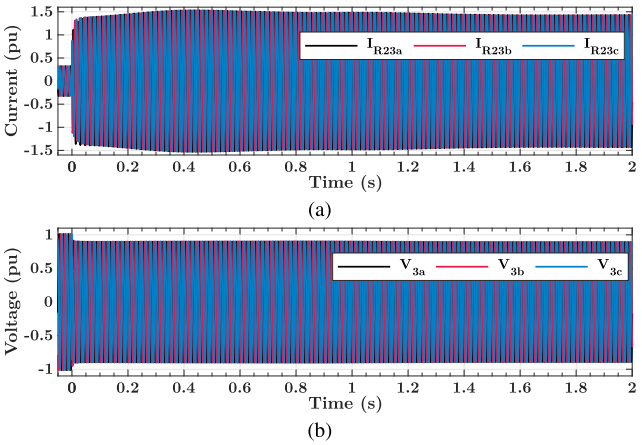


FIGURE 6. Current measured by relay 23 (a) and voltage measured at bus 3 for a 30 Ω three-phase fault applied at bus 3 (b).

As it can be seen in Fig. 7a, the conventional protection was drastically affected by the increase in fault resistance. All relays did not operate to isolate the fault within the maximum window of 2 seconds. In contrast, the microgrid would be correctly protected by the proposed dual-layer

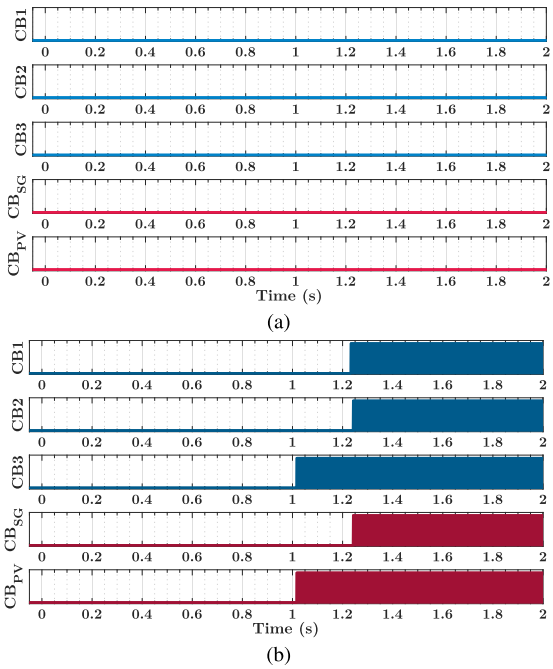


FIGURE 7. Trip signal for the (a) conventional protection, and (b) proposed dual-layer protection for a 30 Ω three-phase fault at bus 3.

strategy with impedance blocking. Fig. 7b shows that IED3 was the first to trip close to 1 s after the fault started, sending a remote trip signal to open the PV circuit breaker. Due to the SG contribution to the fault current, the undervoltage on bus 5 was less severe, which led to delayed IED2 operation. Therefore, the fault was completely isolated after IED1 operated in approximately 1.2 s, when it sent a remote trip signal to open CB2 and, consequently, disconnect the SG.

A subsequent analysis of all fault cases simulated was conducted, evaluating the accuracy for the conventional protection and the proposed dual-layer with and without impedance blocking. Table 4 shows the performance of the method in each scenario in the simulation environment.

TABLE 4. Correct trips for all the evaluated scenarios in simulation.

Scenarios	OC Relays	Dual-Layer	
		Without blocking	Impedance blocking
Scenario 1	98.54% (3902/3960)	99.95% (3958/3960)	100.0% (3960/3960)
Scenario 2	98.46% (3899/3960)	99.95% (3958/3960)	100.0% (3960/3960)
Scenario 3	58.62% (34/58)	62.07% (36/58)	79.31% (46/58)
Average	85.21%	87.32%	93.10%

First, an analysis of the results for all methods in Scenarios 1 and 2 showed that the connection of the BESS had no significant effect on any of them. Regarding conventional protection, it had reasonable results for Scenarios 1 and 2. However, on Scenario 3 the performance drastically reduced to below 59%. Therefore, the average performance for the conventional protection was equal to 85.21%. The dual-layer protection achieved a superior performance than the conventional protection. Without the impedance blocking, the

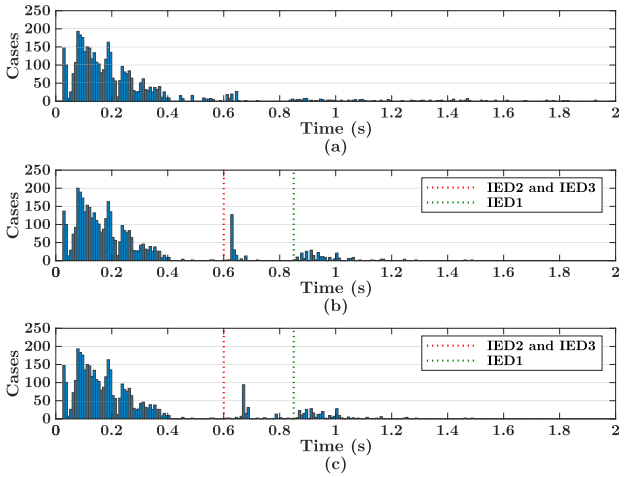


FIGURE 8. Clearing time histograms for Scenario 1 in simulation for (a) conventional protection, and dual-layer protection (b) without and (c) with impedance blocking.

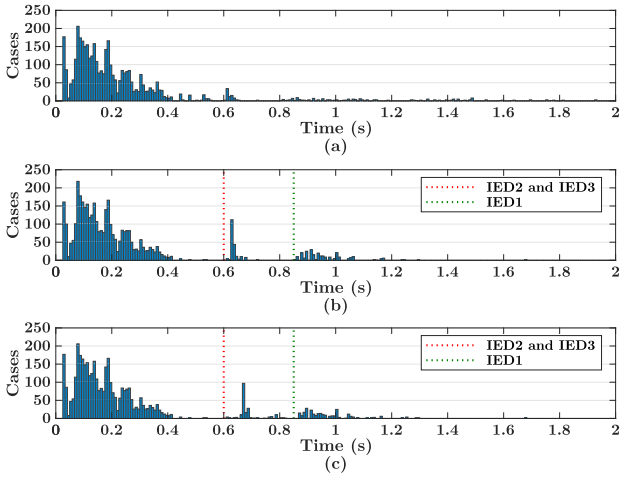


FIGURE 9. Clearing time histograms for Scenario 2 in simulation for (a) conventional protection, and dual-layer protection (b) without and (c) with impedance blocking.

protection had an elevated performance in Scenarios 1 and 2, but it only increased the performance in Scenario 3 by two cases in comparison to the conventional protection. When using the impedance blocking, the proposed protection had an accuracy of 100% for Scenarios 1 and 2, and it also increased the performance in Scenario 3 to over 79%. Overall, the dual-layer protection without and with impedance blocking had average performances equal to 87.32% and 93.10%, respectively.

Additionally, the clearing time for each protection was evaluated. Figs. 8 to 10 illustrate the clearing time histograms for each protection approach in simulation. In the histograms for the dual-layer protection, the dashed lines represent the minimum time for the primary (red) and backup protection (green) of the second layer.

Overall, the clearing time for the conventional protection was spread out over 0.6 s, reaching multiple values close to the maximum limit of 2 s. Nonetheless, when using the

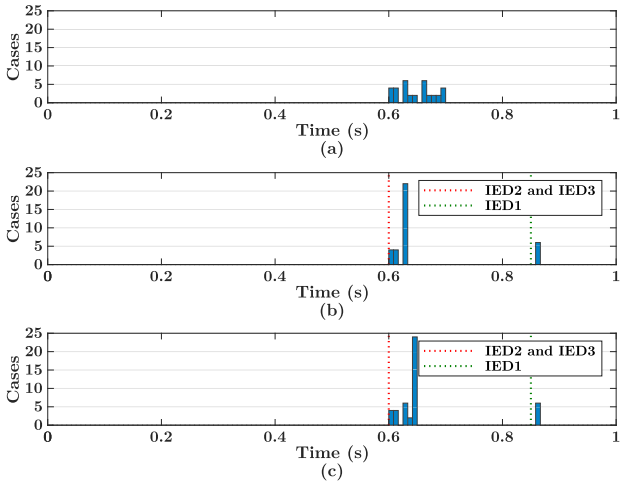


FIGURE 10. Clearing time histograms for Scenario 3 in simulation for (a) conventional protection, and dual-layer protection (b) without and (c) with impedance blocking.

dual-layer protection, these clearing times were concentrated close to 0.6 s and 1 s. Table 5 presents all the clearing time statistics for each of the scenarios.

TABLE 5. Clearing time for all the evaluated scenarios in simulation.

Scenarios	Statistics	OC Relays	Dual-Layer	
			Without blocking	Impedance blocking
Scenario 1	Maximum	1.9302 s	1.4833 s	1.4833 s
	Mean	0.2301 s	0.2389 s	0.2423 s
Scenario 2	Maximum	1.9302 s	1.6750 s	1.6750 s
	Mean	0.2272 s	0.2378 s	0.2409 s
Scenario 3	Maximum	0.6979 s	0.8583 s	0.8583 s
	Mean	0.6488 s	0.6649 s	0.6668 s
General	Maximum	1.9302 s	1.6750 s	1.6750 s
	Mean	0.2305 s	0.2403 s	0.2440 s

Although the dual-layer protection has a time delay of at least 0.6 s for the second layer, its average clearing time was close to 0.24 s for all the simulated fault cases. It can be explained by the fact that the second layer operates to complement the cases where the first layer cannot operate correctly. Thus, the average clearing time for the dual-layer protection was equivalent to that obtained by the conventional protection. Nonetheless, the maximum clearing time when using the dual-layer protection had a reduction of approximately 0.25 s. Finally, the use of impedance blocking resulted in a slight increase in the average clearing time; however, the maximum clearing time remained unchanged.

B. EMBEDDED EVALUATION

In order to evaluate the practicality of the microgrid protection, a laboratory setup was implemented for a real-time evaluation with the protection scheme embedded in hardware. The laboratory setup and the real-time results are presented in the following sections.

1) LABORATORY SETUP

The Real-Time Digital Simulator (RTDS) was used to simulate the test system and perform the hardware-in-the-loop analysis. During the simulation, electrical signals from the test system were converted to analog signals and sent to physical IEDs. Then, if a trip signal was needed, the IEDs would send it back to RTDS, which would open a circuit breaker inside the simulation. The complete laboratory setup is presented in Fig. 11.

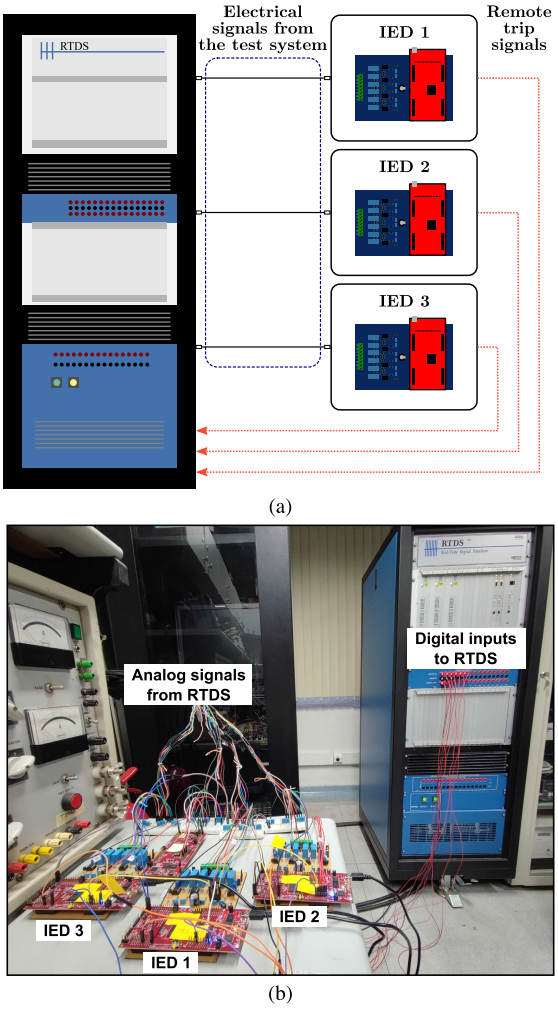


FIGURE 11. Laboratory setup for the tests with hardware-in-the-loop showing the (a) connection diagram, and (b) the actual devices.

In the laboratory setup, only the second-layer proposed strategy was embedded in each hardware that emulated the IEDs. The first-layer was modeled only in the simulation on RSCAD, which is the software used to interface with RTDS. The main component of the IEDs is the LaunchPad F28379D microcontroller from Texas Instruments, which is a dual-core 32-bit processor with a clock of 200 MHz. In addition, it has 12 channels of 16-bit Analog to Digital Converter (ADC) that were used to read the analog signals from RTDS. As this microcontroller has two cores, it allowed the execution of two independent algorithms, one on each

TABLE 6. Configurations for the analyzed scenarios.

	Scenario 1	Scenario 2
Fault types	All 11 fault types	Three-phase faults
Fault resistance	0 Ω and 40 Ω	40 Ω
Fault locations	Buses 3, 4, 6, 8, and 11	All buses from 3 to 11
Microgrid status	Connected	Islanded
DERs power output	100% and 10%	100%, 75%, and 50%
Total fault cases	80	27

core. Therefore, the first core was configured to sample and digitize the signals, followed by the digital filtering and phasor estimation. The second core executed the protection algorithm using the phasor estimated by the first core and sent trip signals if needed. Thus, it was possible to implement the PMD and IED utilizing only one microcontroller, reducing the number of devices required for the tests.

A signal conditioning board was built to utilize the full range of output voltage from the RTDS. The circuitry reduced the signal amplitude from ± 10 V peak to a range of 0 and 3 V, which the ADC supported. Additionally, the signal conditioning board had an analog filter to remove the DC component from the input signal and a 480 Hz low-pass filter to prevent aliasing during the digitization process. A sampling frequency of 1,920 Hz (32 samples/cycle) was configured to compute the phasors utilizing a quadrature oscillator technique with an FIR filter, as recommended by the IEEE Std. C37.118-1 [23]. Thus, the ADC module made the digitized signals available on the data bus of the PMD core, which estimated the phasors and sent them to the IED core using a commercial reporting rate of 120 frames per second.

2) REAL-TIME RESULTS

The test system shown in Fig. 3 was also used to validate the current proposition in real-time. The system was modeled on the software RSCAD, with the same parameters from the simulation environment.

Two distinct scenarios were investigated in the tests, which were the connected and islanded modes. The configurations of these scenarios (fault types, resistance and locations, as well as DER power outputs) are presented in Table 6. Note that, since the BESS connection/disconnection showed no noticeable impact in the simulation analysis, it was assumed to be always connected during the real-time evaluation.

In Scenario 2, only the stable cases for the islanded microgrid found in the simulation analysis were included, as for the other fault cases the internal protection of the DERs would trip under 0.6 s, powering down the microgrid. This resulted in only three-phase faults with a fault resistance of 40 Ω. In all fault cases analyzed, a trip was considered correct if it isolated the smallest area possible and with a clearing time smaller than 2 s.

To illustrate how the proposed microgrid protection operated in real-time, two three-fault cases from Scenario 1 with 100% power injection were selected to be presented in details next. The first case was a solid three-phase fault at bus 3, shown in Fig. 12. In this case, only conventional protection (first layer) was enabled to clear the fault. The currents and voltages were normalized using the pickup current from relay 23 and the nominal voltage from bus 3.

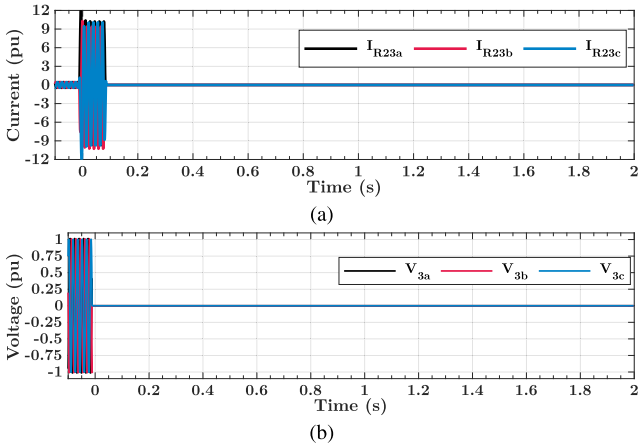


FIGURE 12. Current measured by relay 23 (a) and voltage measured at bus 3 for a solid three-phase fault applied at bus 3 (b).

Due to the high current magnitudes in this case, the conventional overcurrent protection correctly isolated the fault. The trip signals for this fault are shown in Fig. 13.

It should be noted, for this case of a solid fault, the conventional protection correctly isolated the fault under 200 ms, as the DERs were disconnected by their internal protection. The same was valid for the proposed dual-layer protection, which opened the circuit breakers CB1, CB_{SG}, and CB_{PV} under 200 ms, and it also opened CB2 and CB3 under 650 ms. It is worth mentioning that, even though the delay for the second-layer devices was 600 ms, the proposed dual-layer protection was able to trip below this time because of the conventional protection devices inside the first layer.

The second fault case was a 40 Ω three-phase fault at bus 3, shown in Fig. 14. Once again, only conventional protection (first layer) was enabled to isolate the fault.

As illustrated in Fig. 14, the conventional protection failed to protect the microgrid, as the current rose to a magnitude close to its pickup value. Relay 23 operated after 1.99 s; however, it was not enough to isolate the fault, as the DERs remained connected sustaining the fault current. The trip signals for this fault are shown in Fig. 15.

For this case, if considered the proposed dual-layer scheme, the fault would be completely isolated, with all the necessary devices operating under 1.2 seconds, thus protecting the microgrid. Although the proposed protection scheme exhibited a longer clearing time, it successfully safeguarded the microgrid, whereas the conventional protection failed under similar conditions. The analog signals (voltage and current) sent to the IEDs in the second layer are illustrated in Fig. 16. The magnitudes were reduced to be within the ± 10 V range using a transforming ratio of 1:2,300 and 1:240 for voltage and current, respectively.

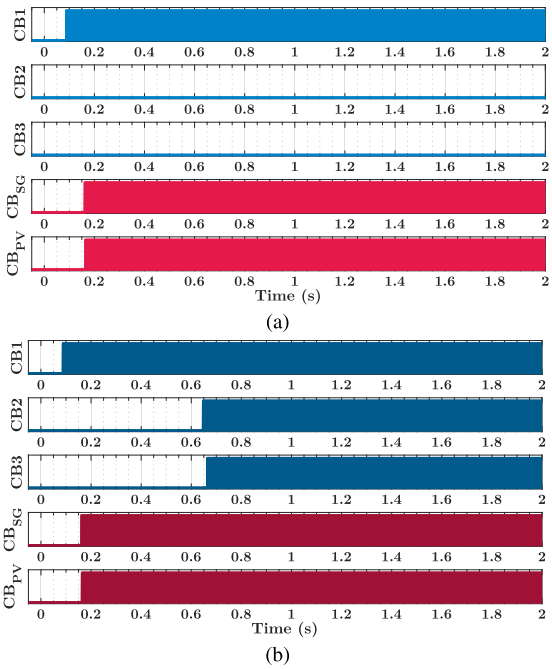


FIGURE 13. Trip signal for the (a) conventional protection, and (b) proposed dual-layer protection for a solid three-phase fault at bus 3.

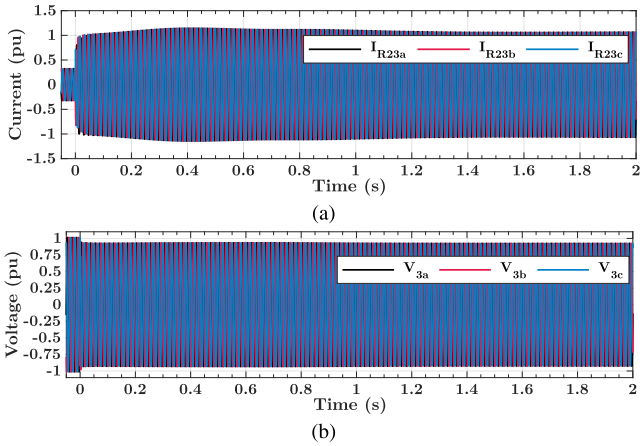


FIGURE 14. Current measured by relay 23 (a) and voltage measured at bus 3 for a three-phase fault applied at bus 3 with a resistance of 40 Ω(b).

Subsequently, all the faults of each scenario were evaluated in real-time. The results for all 107 fault cases are presented in Table 7. It is worth noting that, as mentioned before, only the devices from the second layer were embedded in the hardware, while the devices of the first layer were modeled in the simulation.

The performance for the conventional protection was reasonable for Scenario 1, while it was drastically reduced for Scenario 2 (islanded mode). The microgrid protection performance increased when using the dual-layer approach, with an additional boost when using the proposed impedance blocking, reaching an average performance of 94.44%. The proposed blocking strategy effectively reduced the number

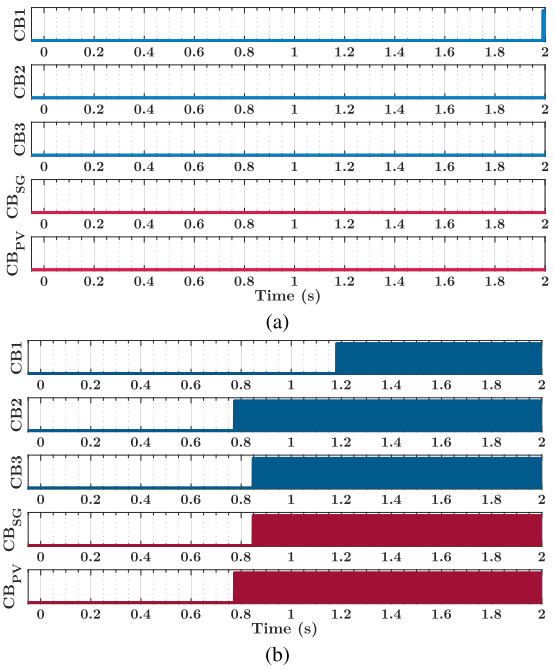


FIGURE 15. Trip signal for the (a) conventional protection, and (b) proposed dual-layer protection for a three-phase fault at bus 3 with a resistance of 40 Ω.

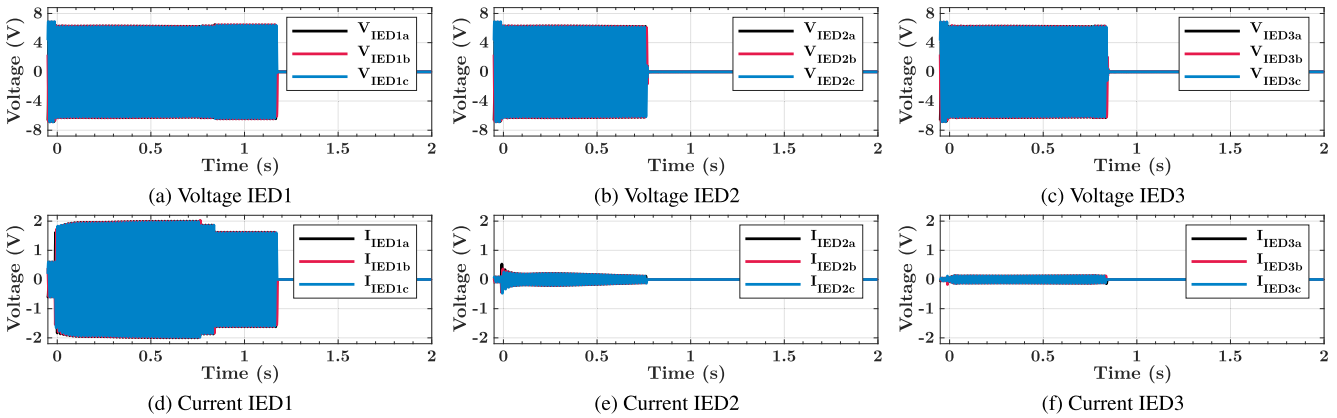
TABLE 7. Correct trips for all the evaluated scenarios.

Scenarios	OC Relays	Dual-Layer	
		Without blocking	Impedance blocking
Scenario 1	92.5% (74/80)	100.0% (80/80)	100.0% (80/80)
Scenario 2	55.56% (15/27)	66.67% (18/27)	88.89% (24/27)
Average	74.03%	83.33%	94.44%

of incorrect operations, especially in Scenario 2. The only three cases of incorrect operation of the proposed dual-layer protection with impedance blocking were related to loss of selectivity between IEDs 2 and 3. Even though these cases were considered incorrect, the proposed approach protected the microgrid, despite isolating a larger portion of the system.

One of the main advantages of a real-time evaluation is the study of the possible effects of the execution time on the clearing time. The clearing time histograms for Scenarios 1 and 2 are presented in Fig. 17 and Fig. 18, respectively.

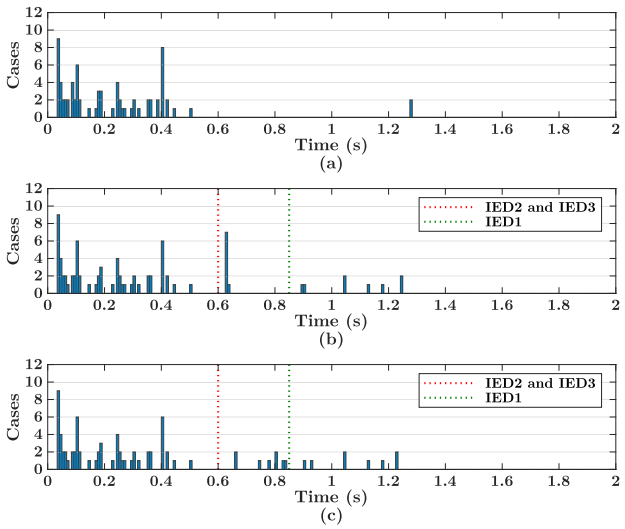
For the two scenarios, the addition of the dual-layer approach had no effect on the clearing times below 0.6 s, which is the minimum delay for the devices in the second layer. Nonetheless, the dual-layer approach operated more accurately than the conventional protection, bringing the clearing time closer to 0.6 and 0.9 seconds, which are the minimum delays for primary (IED 2 and IED 3) and secondary (IED 1) devices in the second layer. The maximum and mean clearing time for each scenario are shown in Table 8.



(a) Voltage IED1 (b) Voltage IED2 (c) Voltage IED3

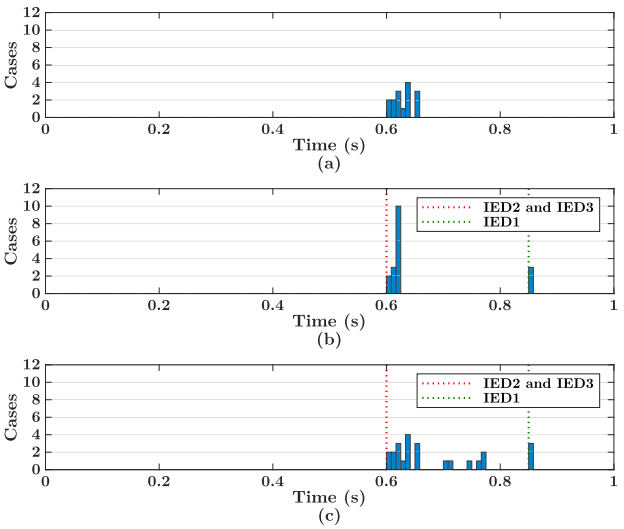
(d) Current IED1 (e) Current IED2 (f) Current IED3

FIGURE 16. Voltage and current signals sent to each IED for a three-phase fault at bus 3 with a resistance of 40 Ω.



(a) (b) (c)

FIGURE 17. Clearing time histograms for Scenario 1 in real-time for (a) conventional protection, and dual-layer protection (b) without and (c) with impedance blocking.



(a) (b) (c)

FIGURE 18. Clearing time histograms for Scenario 2 in real-time for (a) conventional protection, and dual-layer protection (b) without and (c) with impedance blocking.

TABLE 8. Clearing time for all the evaluated scenarios.

Scenarios	Statistics	OC Relays	Dual-Layer	
			Without blocking	Impedance blocking
Scenario 1	Maximum	1.2792 s	1.2469 s	1.2305 s
	Mean	0.2291 s	0.3266 s	0.3402 s
Scenario 2	Maximum	0.6544 s	0.8557 s	0.8557 s
	Mean	0.6289 s	0.6574 s	0.6866 s
General	Maximum	1.2792 s	1.2469 s	1.2305 s
	Mean	0.2965 s	0.3874 s	0.4201 s

In Scenario 1, the dual-layer protection reduced the maximum clearing time from 1.2792 s to 1.2469 s without blocking and to 1.2305 s with impedance blocking. The mean clearing time barely increased for the dual-layer protection due to the additional cases correctly isolated by the second-layer devices (after 600 ms). A similar result was obtained for Scenario 2. The increase in the clearing times was caused by cases where the conventional protection failed to operate. Overall, although the use of impedance blocking raised the mean clearing time by almost 40 ms, it was caused by the blocking strategy preventing the protection from malfunctioning, which resulted in a better general performance for the microgrid protection.

IV. CONCLUSION

This paper presented a robust dual-layer microgrid protection approach utilizing an impedance-blocking strategy to enhance its performance. The proposed protection was extensively evaluated using simulation and a hardware-in-the-loop procedure, considering changes in the operation conditions of the microgrid and different fault cases. Furthermore, the proposed protection increased the performance of the microgrid protection while reducing the maximum clearing time. Over 10,000 simulations were analyzed in the simulation environment, proving that the proposed dual-layer approach increased the reliability of the microgrid protection.

The proposed protection approach was embedded and tested in low-cost hardware, confirming that the proposition can be easily implemented in a practical application, disregarding the use of compute-intensive resources.

Further investigation into the proposed protection scheme presents several possibilities for exploration in future studies. These include: (i) examining a microgrid featuring a high penetration of DERs alongside diverse control strategies, such as grid-forming techniques; (ii) analyzing the operation of the undervoltage strategy with impedance blocking within a single-layer architecture configuration; (iii) exploring additional applications for the proposed impedance blocking method, particularly investigating its directional characteristics and potential uses.

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