Performance Perspective of Gate-All-Around Double Nanosheet CMOS Beyond High-Speed Logic Applications

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***Abstract*—In this review paper, the performance characteristics of Gate-All-Around (GAA) double nanosheet (NS) MOSFETs are described over a broad temperature range, from 78 K to 473 K (200 °C). Emphasis is on the analog operation, showing good potential. Besides the transistor length, the impact of the metal gate Effective Work Function and the vertical distance between the nanosheets has been studied. Among others, a clear Zero Temperature Coefficient (ZTC) gate voltage has been observed that can be modeled by considering the shift with temperature of the threshold voltage and the maximum transconductance. A trade-off has been noticed between the transistor efficiency and the unit gain frequency, whereby the optimal operation point occurs in strong inversion regime. The feasibility of designing simple analog circuits has also been demonstrated. Finally, a detailed investigation of the low-frequency noise behavior yields good values for the flicker noise Power Spectral Density in comparison with other technology nodes.**

***Index Terms*—GAA CMOS; analog performance; cryogenic temperatures; low-frequency noise**

I.INTRODUCTION

It has been extensively shown that Gate-All-Around (GAA) structures outperform for example tri-gate FinFETs (FFs) with respect to short-channel effect control [1] and will, therefore, be crucial for end-of-the roadmap logic devices. Depending on the aspect ratio, i.e. height (H) versus width (W) one can consider using nanowires (NWs; H~W) [2-9] or nanosheets (NSs; H<W) [6,8,10]. The effective channel width can be enhanced by implementing stacked NWs or NSs. Further footprint reduction can be achieved by combining n- and p-channel transistors in a so-called Forksheet (FS) structure [11,12].

The input and output characteristics of GAA devices have been extensively studied both by TCAD simulations and measurements and the basic static parameters – the threshold voltage V_T, the transconductance g_m, the subthreshold swing SS - have been determined over a broad temperature (T) range. While the focus is usually on temperatures from 300 K (Room Temperature - RT) to about 150 °C, there is currently strong interest in exploring also the low-T or cryogenic T side, even below 77 K [13-19]. A first reason is that lowering the temperature to 77 K results in the performance gain equivalent to one scaling step, by the increase of the device mobility upon cooling [13]. More recently, research on Si CMOS-based quantum computing has revived the interest in developing read-out electronics operating at liquid helium T [14-19].

At the same time, one might be interested in deploying GAA CMOS for applications beyond standard high-speed logic, covering the range from (high-speed) analog to RF. This requires analysis of the analog device performance, including the transistor efficiency, the Early voltage and the voltage gain.

Therefore, the goal of the present review is to summarize the characterization of GAA double NS CMOS transistors in a broad temperature range and from an analog circuit applications viewpoint. The impact of certain process parameters, regarding the Effective Work Function (EWF) metal gate and the NS separation will be discussed. On top of the standard analog parameters, also the low-frequency (LF) noise is investigated in detail. This is not only important with respect to the signal-to-noise ratio in analog circuits [20], but at the same time reveals valuable information regarding the gate stack quality [20-24].

II. DEVICES AND MEASUREMENTS

The studied nMOS transistors are vertically stacked gate-all-around (GAA) silicon nanosheets (NS) fabricated at imec, Belgium for sub 7-nm technology node [6,7].

The evaluated GAA-NS structure has double vertically stacked sheets and 22 wires or sheets in parallel. Each n-channel transistor has a gate dielectric composed by SiO_2 and HfO_2, resulting in an effective oxide thickness (EOT) of 0.9 nm, a fin width (W_{SH}) of about 15 nm and a height (H_{SH}) of about 11 nm, with an effective channel width ($W_{eff} = 22*(2 * W_{SH} + 2 * H_{SH})$) and the channel lengths ranging from 28 nm to 200 nm. Figure 1 shows the schematic structure of a GAA double NS MOSFET. The cross-sectional Transmission Electron Microscopy (TEM) image of the fabricated devices, can be found in references [7,9].

One of the process parameters investigated in this work is the metal gate stack, considering materials with different Effective Work Function (EWF). In this study, the reference devices have been fabricated with a metal gate stack composed by two layers of TiN with an aluminum-based material between them, with a total thickness of 7.5 nm (Fig. 2A). Using a different EWF metal enables to aggressively scale

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the metal gate thickness, resulting in a reduced NS separation of 4.7 nm (Fig. 2b).

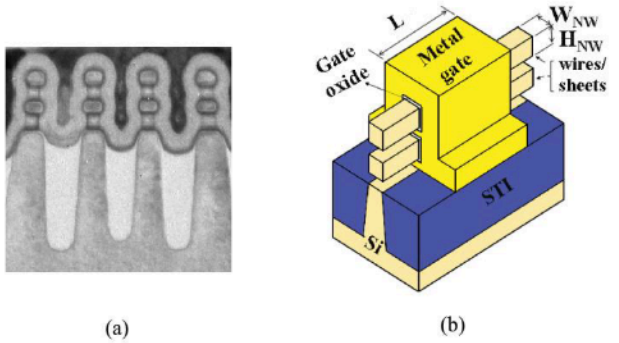

Fig. 1 TEM images of the gate stack composed by Al-based Effective Work Function metal layer (a) and the structure of the device (b) [7,9].

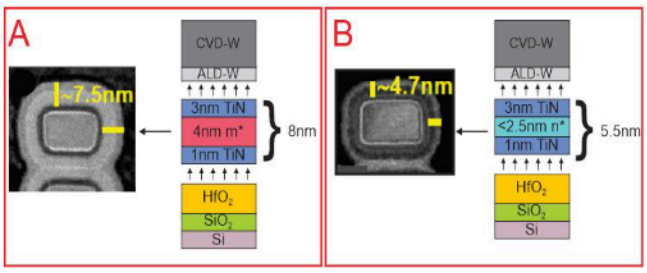

Fig. 2 TEM images of the gate stack composed by (A) Al-based layer (m*) layer and (B) layer (n*) [7].

The n-type GAA vertically stacked silicon NS MOSFETs have been measured with a gate bias (V_{GS}) from -0.5 V up to 1.0 V with a step of 10 mV, and the drain voltage (V_{DS}) in the triode region was 50 mV and 0.7 V in the saturation region. A similar bias range with opposite sign has been used to characterize the GAA NW pMOSFETs. The on-wafer measurements were performed using a B1500 Parameter Analyzer and an E4727A Advanced Low-Frequency Noise Analyzer from Keysight. For low-frequency noise analysis, at least five similar devices per wafer have been measured.

III. High and Low Temperature Performance

As can be seen from Fig. 3 obtained on a L=28 nm nMOSFET, the input characteristics at a drain voltage V_{DS}=50 mV exhibit the expected shift of V_T towards lower values for increasing T, while the drain current I_D decreases in strong inversion [25]. At the same time, a clear Zero Temperature Coefficient (ZTC) point is observed, both in ohmic regime (Fig. 3A) and in saturation (Fig. 3B), taken at V_{DS}=700 mV. This ZTC point V_{ZTC} corresponds with the gate voltage V_{GS} where I_D is independent on temperature and is an interesting design point for analog circuits. It originates from the balance between the shift of V_T with temperature on the one hand and on the other the reduction of the mobility, impacting the transconductance.

The former is illustrated in Fig. 4 for GAA double NS nMOSFETs with different gate length L and in ohmic regime (Fig. 4A) and saturation (Fig. 4B). A more or less linear reduction of V_T with T is found in Fig. 4, where the reduction becomes higher for shorter L. Moreover, a smaller V_T and a higher temperature shift is found in saturation, due to the impact of the higher lateral electric field at higher V_{DS}, inducing a drain-induced barrier lowering (DIBL). This also explains the higher $|\Delta V_T/\Delta T|$ in saturation and for shorter L in Fig. 5 [25].

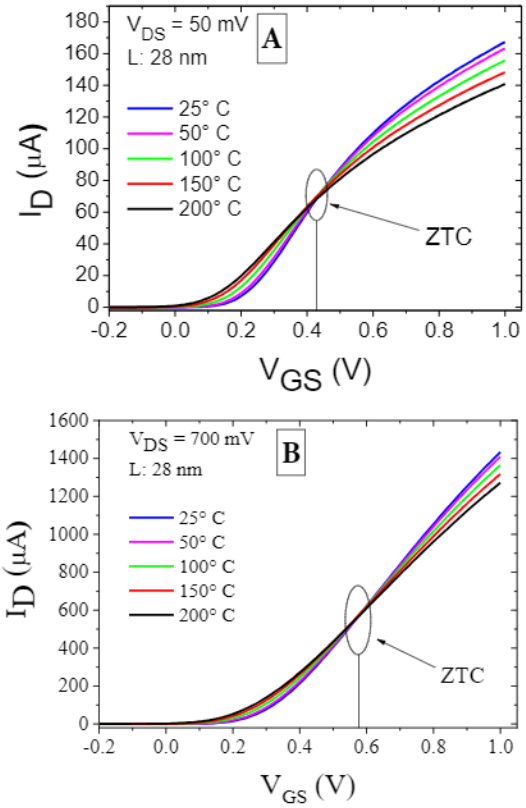

Fig. 3 ZTC point with temperature variation from 25 °C to 200 °C in triode operation region with V_{DS} = 50 mV (A) and in saturation operation region with V_{DS} = 700 mV (B) for a GAA-NS nMOSFET of L=28nm.

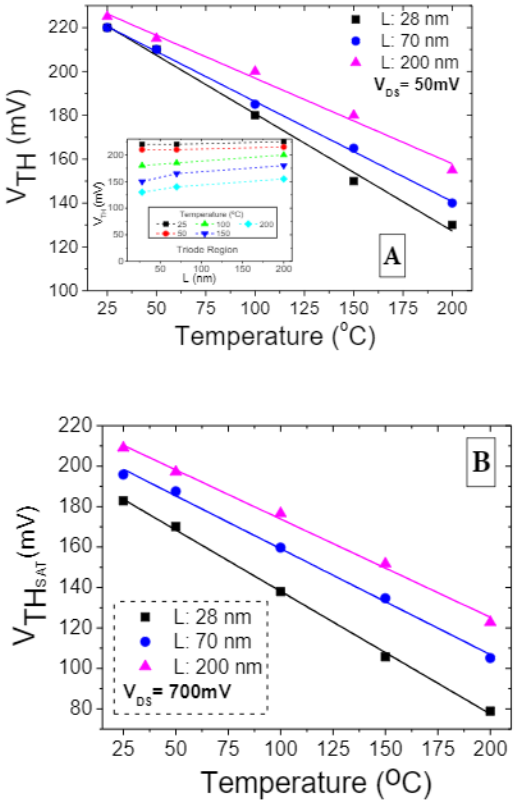

Fig. 4 Threshold voltage as a function of temperature for GAA NS nMOSFETs with different L in triode region with V_{DS} = 50 mV (A) and in saturation region with V_{DS} = 700 mV (B). The correlation coefficient of each line is higher than 0.99.

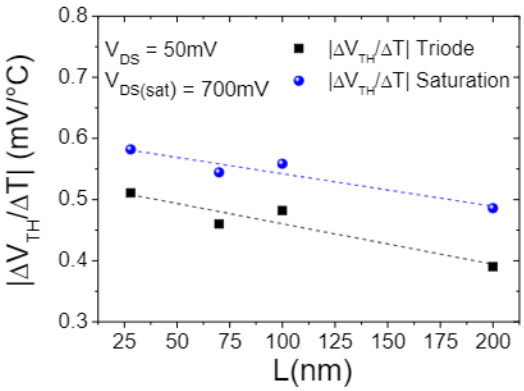

Fig. 5 Absolute value of the threshold voltage variation with temperature as a function of channel length in triode and saturation region versus channel length for GAA NS nMOSFETs.

As shown previously [25], the ZTC point can be modeled analytically, based on the equation (ohmic regime) [26,27]:

$$V_{ZTC} = V_{T1} + \frac{\left(\frac{T_1}{T_2}\right)^C \cdot \left|\frac{\Delta V_T}{\Delta T}\right| \cdot (T_2 - T_1)}{1 - \left(\frac{T_1}{T_2}\right)^C} + \frac{n.V_{DS}}{2} \quad (1)$$

In Eq. (1), V_{T1} is the threshold voltage at the reference temperature T_1 (usually RT), T_2 is a higher temperature, n is the body factor and the parameter C is derived from the temperature dependence of g_m and defined as [25-27]:

$$c = \frac{log(g_{m2}) - log(g_{m1})}{log(T_1) - log(T_2)} \quad (2)$$

with g_{m1} and g_{m2} corresponding with the maximum transconductance (g_{mmax}) at T_1 and T_2, respectively. A similar expression as Eq. (1) has been derived for the saturation regime [25-27]. Finally, as can be derived from Fig. 6, a good agreement between the analytical model and the measured data, with a maximum error less than 12% in the worst case, can be achieved. This holds both for the linear and saturation regime and for all device lengths investigated [25].

The study has also been extended to the p-type GAA double NS MOSFETs [28]; an example of the input I_D-V_{GS} characteristics for a L=200 nm device is given in Fig. 7. A clear V_{ZTC} is observed both in ohmic and saturation regime, that can be analyzed according to the analytical model of Eqs (1)-(2). Qualitatively similar conclusions can be reached with respect to the L and V_{DS} dependence [28]. Overall, it can be concluded that the GAA double NS MOSFETs continue to operate satisfactorily up to a temperature of 200 °C.

More recently, the cryogenic operation of GAA double NS nFETs has been investigated [29], showing improved SS, a higher V_T and g_{mmax} at low T. The reduction of the SS by a factor of about 4 from RT down to 78 K is as expected from its kT dependence (k is the Boltzmann constant). At the same time, it has been shown that the vertical distance between the NS, shown in Fig. 2, has some impact on the static device parameters: this leads to an increasing V_T and a reduction in low-field mobility for reduced vertical distance, as extracted from an improved Y-function methodology [29]. On the other hand, similar access resistance values have been obtained at 300 K and 78 K for both NS separations. Currently, the low-temperature characterization of the p-channel counterparts is underway.

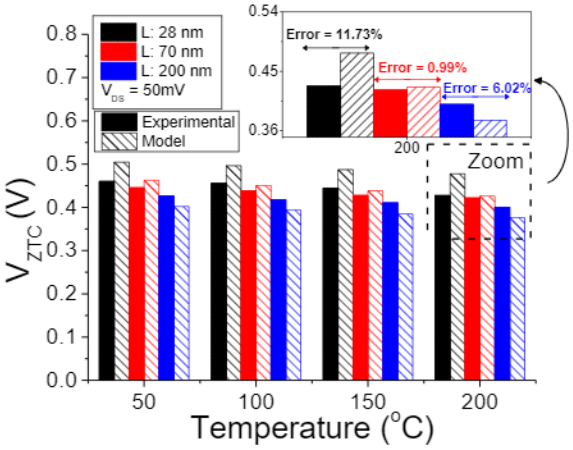

Fig. 6 Experimental and analytical model results as a function of temperature in triode region for GAA NS nMOSFETs with different channel lengths and the error demonstration for the worst case in the Zoom area.

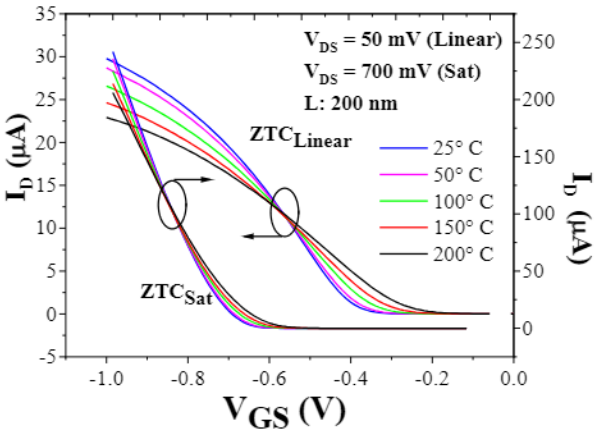

Fig. 7 Drain current in function of the gate voltage for different temperatures, corresponding with a GAA NS pMOSFET with L=200 nm.

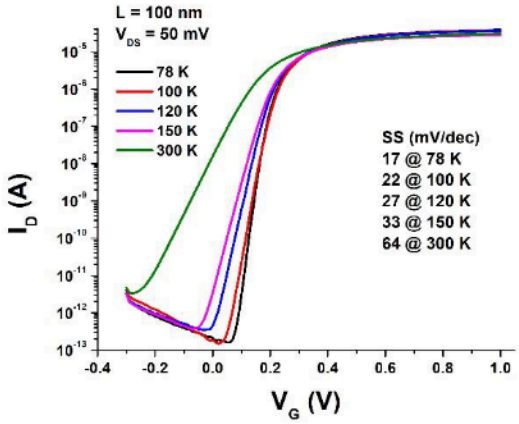

Fig. 8 Drain current in function of the gate voltage for different temperatures corresponding with a GAA NS nMOSFET with L=100 nm.

Concluding this part, it can be stated that GAA double NS transistors can be operated in a broad temperature range, with well-behaving static parameters. The presence of a clear V_{ZTC} opens up the possibility to design temperature-insensitive circuits.

IV. Analog Performance

The analog performance parameters of GAA double NS nFETs have extensively been studied in a broad temperature range [30-35], considering the impact of the NS separation shown in Fig. 2. It is evident from Fig. 9 that due to the difference in the effective work function for stack m* and n*, the V_T is affected, while at the same time, a higher g_{mmax} is obtained for the smaller vertical distance [33]. This translates into a better transistor efficiency defined as g_m/I_D in Fig. 10 for saturation. At the same time, it has been shown that this parameter degrades with T for both types of NS nFETs [33].

The Early voltage V_{EA} is an indirect measurement of the channel length modulation caused by the high lateral electric field at high V_{DS}, i.e., the higher the V_{EA} the lower the channel length modulation. Since the increase in the channel length modulation degrades V_{EA}, it also affects the intrinsic voltage gain A_V [36]. As shown in Fig. 11, gate stack n* yields higher V_{EA} for most lengths studied at a gate overdrive voltage $V_{GT}=V_{GS}-V_T$ of 200 mV and at V_{DS}=700 mV. The better Early voltage indicates a better control of the gate stack over the channel modulation by the lateral electric field. Obviously, this is the case for longer channels and for the n* devices with smaller NS separation. In addition, it has been shown that temperature has only a modest impact on V_{EA} up to 200 ºC [33].

As a result, the A_V, given by:

$$|A_V| = \frac{gm}{g_D} \cong \frac{gm}{I_D} * V_{EA} \quad (3)$$

with g_D the output conductance, increases for higher L in Fig. 12 and improves for the gate stack with the best electrostatic coupling (n*) [33]. Again, little impact of T on the intrinsic voltage gain is observed in Fig. 13.

When comparing the obtained $|A_V|$ with other technologies, the nanosheets present an improvement. For FinFETs, junctionless SOI nanowires and Ω-gate SOI nanowires the $|A_V|$ reaches values of about 34 dB [37], 37 dB [38] and 40 dB [39], respectively. On the other hand, the stacked NS can reach a gain of about 46 dB, when comparing similar dimensions and the same gate voltage overdrive V_{GT}

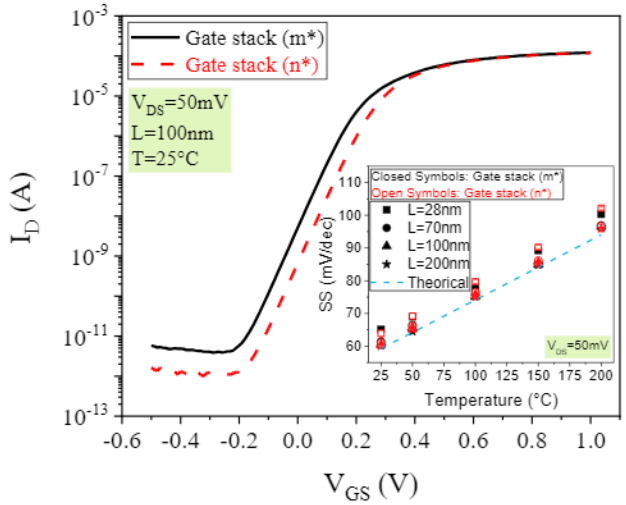

Fig. 9 Drain current as a function of gate voltage for (m*) and (n*) gate stack NS nMOSFETs and (inset) subthreshold swing as a function of temperature for (m*) and (n*) gate stack NS devices for different gate lengths.

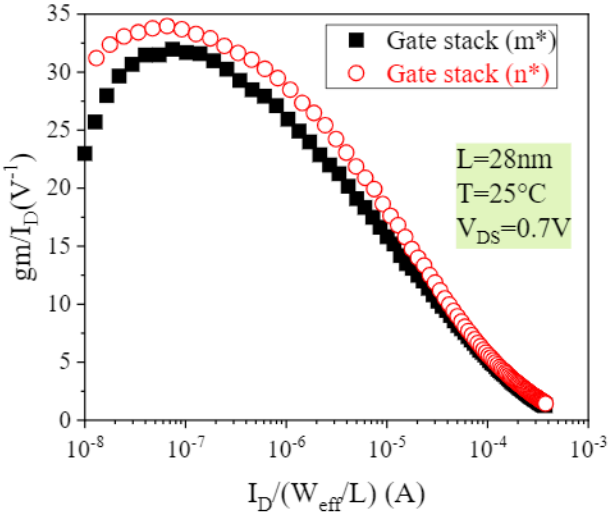

Fig. 10 Transistor efficiency (g_m/I_D) as a function of normalized drain current for (m*) and (n*) gate stack n-type devices at room temperature.

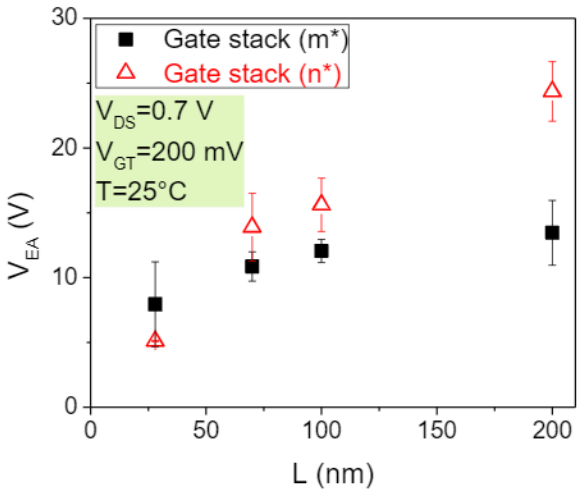

Fig. 11 Absolute Early voltage as a function of transistor channel length for (m*) and (n*) gate stack n-NS devices at room temperature.

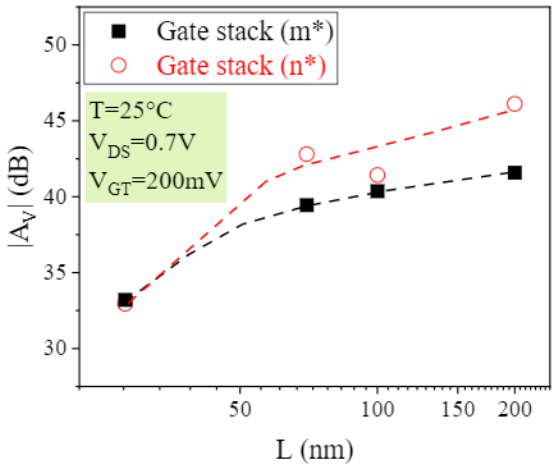

Fig. 12 Intrinsic voltage gain as a function of transistor channel length (L), for (m*) and (n*) gate stack n-type devices at room temperature.

Another important analog parameter is the unit gain frequency f_T [34,35]. The latter parameter is defined as:

$$f_T = \frac{gm_{sat}}{2\pi C_{gg}} \quad (4)$$

where g_{msat} is the transconductance when biased at saturation region (V_{DS}=700 mV) and C_{gg} is the total gate capacitance, extracted experimentally as outlined elsewhere [34,35].

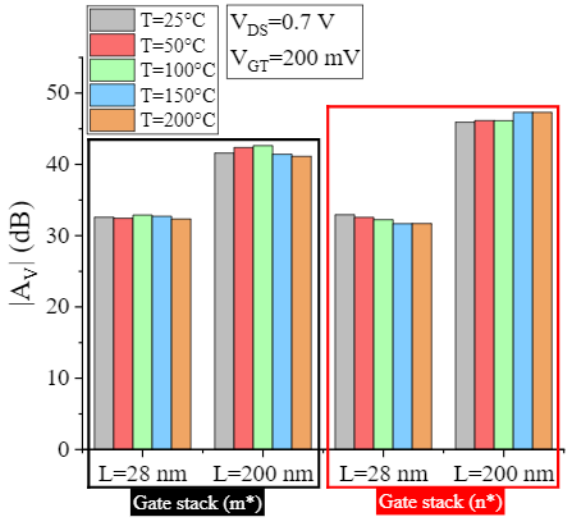

Fig. 13 Intrinsic voltage gain for the L=28 and 200 nm devices studied, in the temperature range from 25°C to 200°C.

The f_T is represented versus the inversion coefficient (IC), whereby the drain current is normalized to its value at V_T and corresponding with the transition from weak (WI) to strong inversion (SI) [41,42]. In other words, it falls in the moderate inversion (MI) regime (0.1<IC<10). It is clear from Fig. 14 that the maximum f_T for both gate stack NS nFETs occurs in SI, revealing a trade-off with the transistor efficiency in Fig. 10 that maximizes in WI. This is a challenging situation for circuit design.

In order to find the optimal operation regime, the product f_T*g_m/I_D is represented in Fig. 15 versus the IC [34,35]. The best application point is obtained at the peak of the trade-off curve, and it happens at the transition from moderate to strong inversion, with IC about 10, for transistors with L=28 nm (MG stack m* and n*) and with L=70 nm (MG stack n*); for L=70 nm (MG stack m*) and 200 nm (MG stack n* and m*) it happens at strong inversion.

The optimal operation point for both types of gate stacks is represented in Fig. 16, showing a slight reduction for increasing T, while it increases for higher L [34,35].

Finally, a comparison of the analog performance parameters between NS and NW nMOSFETs has also been performed [34,35]. The NW devices have an Ω gate structure, as described for example in Ref. [39]. The fact that it is not GAA results in slightly worse short channel effect control for the NS nFETs, as derived from the slightly degraded DIBL values. A similar efficiency versus f_T trade-off has been noted, however, for the NW transistors it occurs in the region of moderate inversion, close to the transition for the strong inversion (with IC between 5 and 11), for L from 30 nm to 200 nm. For the NS transistors the optimal point is also in the transition from moderate to strong inversion (for L=28 nm and 70 nm), and at strong inversion for L=200 nm.

The design of two simple circuits using GAA double NS FETs has been investigated, using a look-up table approach, namely, an Operational Transconductance Amplifier (OTA) [43] and a current mirror [44]. From various performance parameters, it has been demonstrated that a NS-based design offers better perspectives than for example a FinFET-based approach.

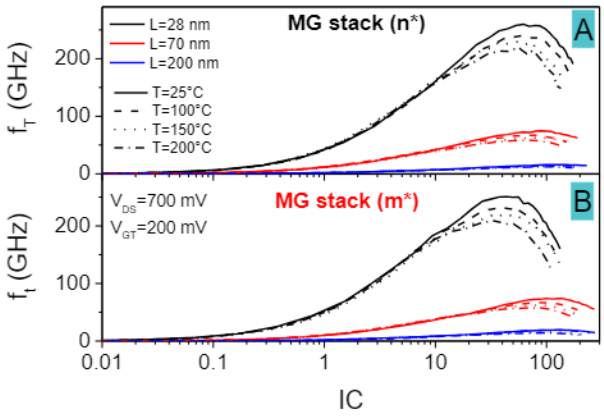

Fig. 14 Unit gain frequency as a function of inversion coefficient for nanosheet n-channel transistors with metal gate stacks n* (A) and m* (B), for different channel lengths and temperatures.

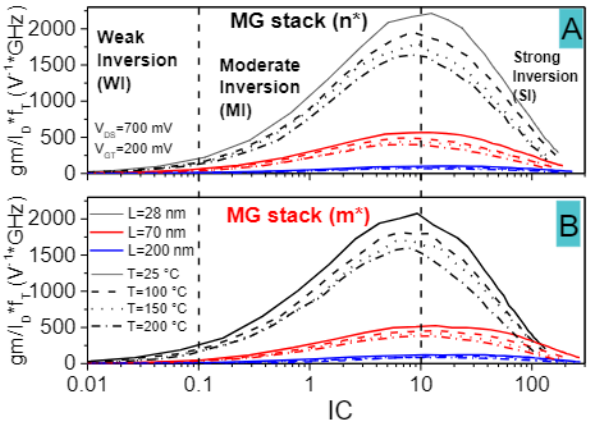

Fig. 15 Trade-off between transistor efficiency and unit gain frequency for nanosheet n-channel transistors with metal gate stacks n* (A) and m* (B), for different channel lengths and temperatures.

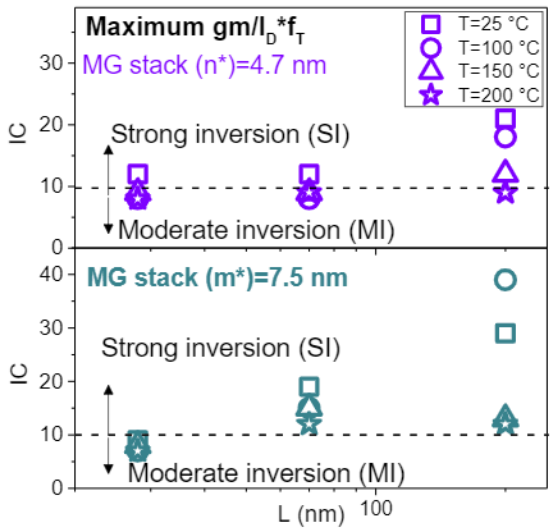

Fig. 16 Corresponding inversion coefficient values for maximum gm/I_D*f_T, for MG stacks n* and m*.

V. Low-frequency noise

The LF noise behavior of NS nMOSFETs has been studied extensively in linear operation, at low V_{DS} (50 mV) [33,45-47]. Emphasis was on the impact of the EWF metal gate. A broad range of different gate metals has been investigated, as summarized in Fig. 17 [47]. The observed noise spectra were predominantly 1/f-like (flicker noise), as shown in Fig. 18; the drain current noise Power Spectral Density (PSD) (S_{ID}) multiplied by the frequency f exhibits a horizontal trend. From a comparison of the normalized S_{ID} at f=10 Hz, i.e., S_{ID}/I_D^2 with the $(g_m/I_D)^2$ function in Fig. 19, it can be concluded that the 1/f noise is due to so-called number fluctuation or the Δn mechanism [20-24]. In other words, the 1/f noise is due to trapping by channel carriers by gate oxide traps with a density N_{OT}.

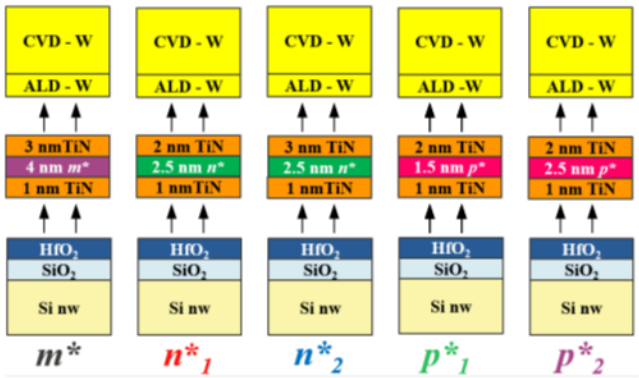

Fig. 17 Gate stack composition for five different wafers under evaluation, whereby m* is an Al-based reference process, n* is an alternative metal 1, and p* is another alternative metal 2. All thickness values correspond to the nominal ones. ALD means Atomic Layer Deposition and CVD is Chemical Vapor Deposition.

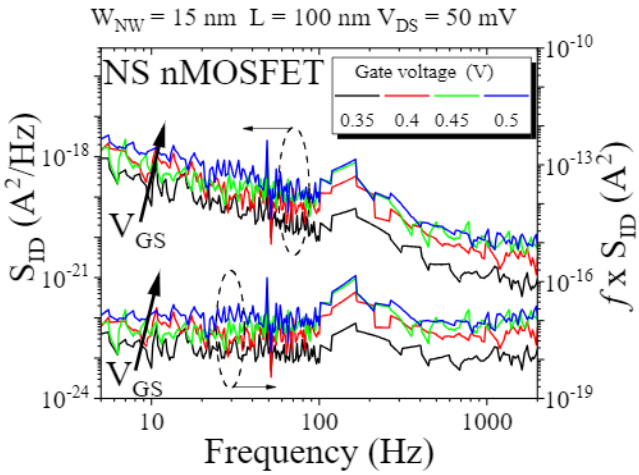

Fig. 18 Drain current noise power spectral density and normalized power spectral density as a function of frequency for a 15 nm nanosheet width n-channel device at different gate voltage.

According to the Δn correlated mobility fluctuations model, the 1/f input-referred noise PSD (S_{VG}) can be expressed as [20-24]:

$$\sqrt{S_{VG}} = \sqrt{S_{Vfb}}\left(1 + \alpha_{SC}\mu_{eff}C_{ox}\frac{I_D}{g_m}\right) \qquad (5)$$

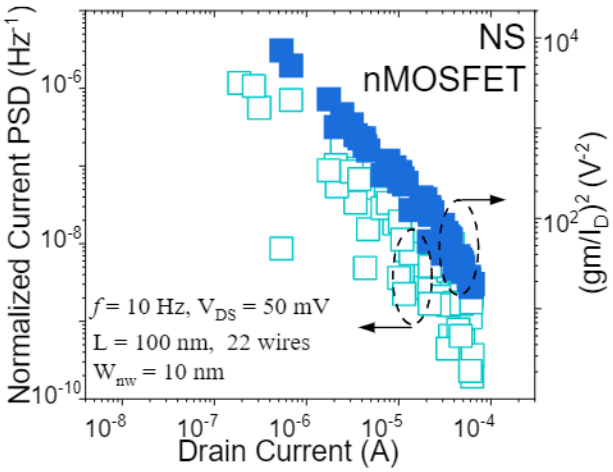

Fig. 19 Normalized drain current noise PSD at 10 Hz and g_m^2/I_D^2 versus drain current in linear operation for a GAA nNWFET with 22 wires of width W_{nw}=10 nm and a gate length of 100 nm.

with S_{Vfb} the PSD at flat-band voltage S_{Vfb}, α_{SC} the scattering coefficient, μ_{eff} the effective low-field mobility and C_{ox} the gate oxide capacitance density (pF/cm^2). In other words, representing S_{VG} versus the gate overdrive voltage V_{GT} (~I_D/g_m) should according to Eq. (5) yield a straight line with slope proportional with α_{SC} and intercept proportional with N_{OT}. This follows from the fact that the S_{Vfb} can be expressed as [20-24]:

$$S_{Vfb} = \frac{q^2 kTN_{OT}}{W_{eff}L\alpha_t C_{ox}^2 f} \qquad (6)$$

with q the elementary charge and α_t the tunneling parameter for electrons into the gate oxide. As shown by Fig. 20, a linear behavior is indeed observed, resulting in the α_{SC} and N_{OT} values of Fig. 21.

Overall, there is some impact of the EWF metal on the gate stack quality, with low N_{OT} and α_{SC} as desirable. A correlation with the μ_{eff} has also been established, which can be explained by the fact that the charged oxide traps, corresponding with N_{OT}, contribute to the Coulombic scattering and a reduction of the electron mobility [47]. According to the results of ref. [33], the vertical distance has only a marginal effect on the 1/f noise PSD. At the same time, when comparing with other types of transistor architectures, the NS devices stand out favorably [48-50]. This is in line with the general trend of the scaling roadmap for 1/f noise, where the normalized S_{VG} reduces with the EOT [51]. At the same time, increased charge sharing of the trapped charge between the different gates additionally reduces its impact on the noise PSD. Qualitatively similar results have been obtained for the GAA NS pMOSFETs.

More recently, noise characterization at cryogenic temperatures has been explored in GAA double NS nMOSFETs [29], showing the presence of 1/f and Generation-Recombination (GR) noise. In the first instance, the flicker noise can be modeled by the Δn plus correlated mobility fluctuations model down to 78 K (Fig. 23), whereby additionally, one has to consider the impact of the access resistance, according to the analysis proposed earlier [52]. Currently, the cryogenic noise performance of pMOSFETs is being evaluated and further measurements down to 10 K are foreseen in the nearby future.

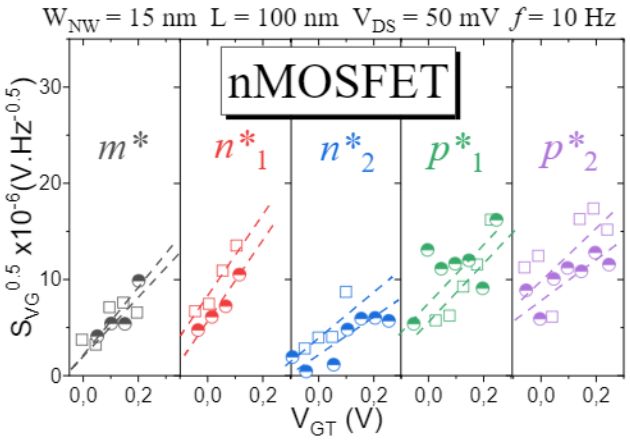

Fig. 20 Square root of the input–referred gate voltage noise power spectral density at 10 Hz as a function of drain current over transconductance ratio for the different gate stack approaches and samples.

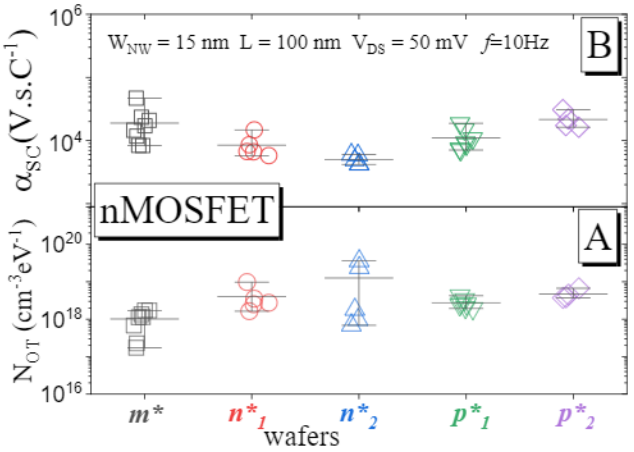

Fig. 21 A: Oxide trap density and B: Coulomb scattering coefficient for different gate stack approaches.

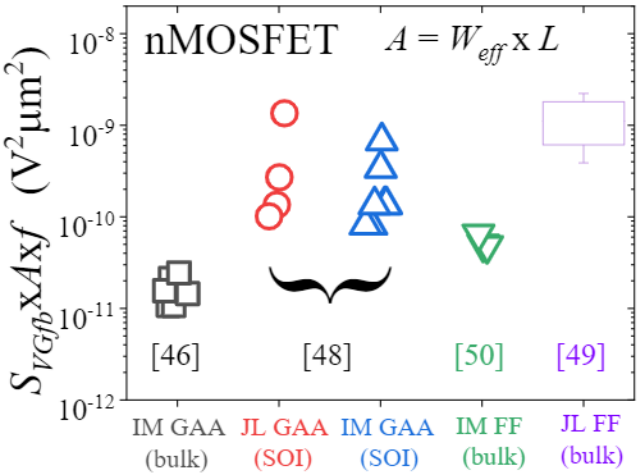

Fig. 22 Benchmark of the normalized S_{VGfb} for n–channel silicon devices on either bulk or Silicon–On–Insulator (SOI) wafers: junctionless (JL), inversion mode (IM), finFETs (FF), Gate–All–Around (GAA).

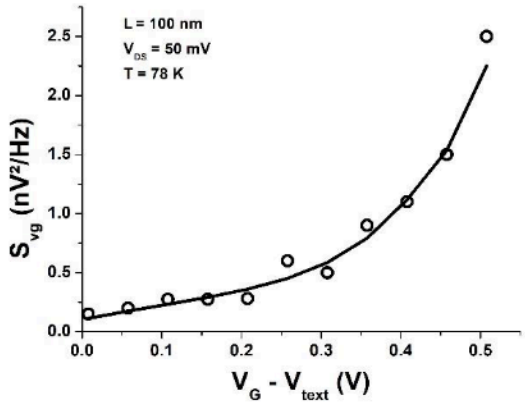

Fig. 23 Input-referred voltage noise PSD at 10 Hz for an L=100 nm GAA NW n-channel FET at 78 K.

VI. Conclusions

Overall, it can be concluded that GAA NS CMOS can be exploited beyond high-performance logic and has good potential for analog applications. Especially the low noise PSD is an asset. Moreover, the devices can operate successfully over a broad temperature range between 78 K (and as to be demonstrated also lower) and 200 °C.

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