

Received 7 November 2025, accepted 12 November 2025, date of publication 20 November 2025,
date of current version 1 December 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3635517

RESEARCH ARTICLE

Algebraic Tracking Network Topology Processor for Modern Power Systems

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This work was supported in part by the Brazilian Federal Agency for Support and Evaluation of Graduate Education (CAPES) under Grant 88887.141227/2025-00; in part by the Brazilian National Council for Scientific and Technological Development (CNPq) under Grant 408464/2023-2 and Grant 308273/2025-7; and in part by São Paulo Research Foundation (FAPESP) under Grant 2022/09203-0, Grant 2024/21574-0, and Grant 2023/17472-4.

ABSTRACT The growing deployment of Phasor Measurement Units (PMUs) in Electric Power Systems (EPSs) has led status measurements from switchable devices to be transmitted at high sampling rates, enabling rapid detection of switching events and continuous topology updates. Fast topology processing is therefore essential for reliable operation and decision-making in modern, dynamic EPSs. In this context, this paper proposes an Algebraic Tracking Network Topology Processor (AT-NTP) developed from algebraic formulations and a new islanding identification method. Using status measurements from PMUs and other sources, AT-NTP determines and updates network topologies through matrix factorization and refactorization, avoiding graph search algorithms and artificial intelligence techniques commonly used in existing topology processors. It is simple to implement, avoids combinatorial explosion, does not require training stages, and efficiently detects switching events, island formation, bus merging or splitting, and measurement configuration changes without recomputing the topology from scratch. Its formulation applies to arbitrary substation configurations requiring no adaptations, which makes it flexible and suitable for various systems. Simulation results on benchmark and large-scale real networks demonstrated its computational efficiency and confirmed its suitability for PMU-based state estimation and advanced energy management applications.

INDEX TERMS Bus-branch model, digital measurements, network topology processing, PMU, power system state estimation.

I. INTRODUCTION

A. MOTIVATION

Bus-branch model (BBM) is essential for the real-time operation of Electric Power Systems (EPSs) for, by abstracting detailed components while preserving the interconnected structure of the system, it enables the execution of Energy Management System (EMS) applications, including operational analyses, market operations, and State Estimation (SE) [1], [2], [3], [4].

The associate editor coordinating the review of this manuscript and approving it for publication was Nagesh Prabhu¹.

BBMs are generated by Network Topology Processors (NTPs) [5], which process the statuses of Switchable Devices (SDs) (e.g., switches, circuit breakers, or disconnectors located at substations) to aggregate bus-sections into equivalent buses connected by branches, representing physical links with non-null impedance such as transmission lines (TLs) or transformers (TRs). The process also excludes de-energized parts and assigns analog measurements to BBM components [5].

Traditionally, NTPs rely on SDs' status data from Supervisory Control and Data Acquisition (SCADA) systems.

However, SCADA systems, with low update rates (typically 2–5 s [6]), are inadequate for the increasingly dynamic behavior of modern EPSs. Such complexity is driven primarily by the growing integration of inverter-based resources (e.g., solar and wind generation [2]), which increase fluctuations and power generation intermittency [4], potentially leading to rapid and frequent topological changes [7]. Phasor Measurement Units (PMUs) are a promising alternative for addressing that limitation, for, unlike SCADA, they transmit both SD statuses and phasor measurements at high sampling rates, as defined by IEEE C37.118-2011 [8], [9].

PMU-based data enable a rapid detection of topology changes, supporting timely SE and EMS operations. The deployment of PMUs is therefore expected to expand in the coming years, since enhanced real-time monitoring is considered a key strategy for managing EPSs with high renewable penetration. As an example, after the 2025 Iberian Peninsula blackout, the Spanish Transmission System Operator recommended expanding PMU deployment to ensuring at least one device per substation [10].

Computationally efficient NTPs are essential for handling both complexity and dynamics of modern EPSs, and developing NTPs capable of efficiently processing high-rate PMU status measurements is crucial for maintaining correct and up-to-date topology information, provided reliable status data are available. This efficiency also allows SE tools to rely solely on PMU data, minimizing errors caused by SCADA-PMU measurement asynchrony [6], [11]. Despite their importance, existing NTPs still face several limitations, as discussed in what follows.

B. LITERATURE REVIEW

One of the earliest automatic NTPs was proposed in [12], introducing an approach based on graph search techniques for identifying bus connectivity. However, the method does not operate properly for all substation arrangements and requires a complete reinitialization after any change in SD statuses [5]. Since then, several NTPs have continued to rely on graph search algorithms, but still facing scalability issues and the risk of combinatorial explosion, which make them unsuitable for large-scale and highly dynamic EPSs [7].

The concept of Tracking NTP (T-NTP) was introduced in [13]. A T-NTP monitors changes in SD statuses and seeks to update only regions affected by topological modifications. However, it is also graph-based and entirely dependent on conventional topology processing, thus remaining subject to other fundamental limitations identified in [12].

Reference [14] introduced another graph-based T-NTP. Although improving computational performance through more efficient data structures, it still relies on sequential execution to update the network topology when multiple SDs change status simultaneously between two consecutive time steps. Despite the drawbacks, the method can process detailed Measurement Arrangements (MAs) to allocate measurements to BBM components. A detailed representation of

MAs in topology processing is important, since, depending on SD statuses, some measurements may be discarded even when the monitored equipment remains energized [14].

Reference [15] developed a T-NTP based on the method proposed in [12], addressing several of the previously identified limitations. Although designed to handle arbitrary substation arrangements and avoid complete reinitialization when SD statuses change, the method also relies on graph search algorithms, and each SD must be classified according to its location and function within substations. Fictitious SDs are introduced to represent switches connected to more than two distinct components. Complex list- and table-based rules assign indices to the buses included in or excluded from the BBM, and no detailed MAs were addressed. All such factors may limit or hamper the T-NTP adaptation to new equipment or emerging EPS characteristics.

More recently, an Artificial Intelligence (AI)-based NTP (AI-NTP) [2] has shown to efficiently leverage PMU data and detect topology errors. However, it requires training stages specific to each substation arrangement and that depend on the availability of sufficiently large datasets. MAs are not detailed and the way measurements are assigned to BBM components is not clearly described.

All aforementioned NTPs were tested only on small-scale systems, and none of the reviewed studies demonstrated the feasibility of applying them to large-scale networks within time frames compatible with the high sampling rates of PMUs.

C. PROPOSALS AND CONTRIBUTIONS

This paper introduces a simple, generic, and computationally efficient Algebraic Tracking Network Topology Processor (AT-NTP) suitable for modern EPSs where SD statuses are transmitted via PMUs. The method can also be used with legacy SCADA systems. It is based on algebraic theorems for islanding identification [16] and uses incidence matrix factorization to determine bus connectivity efficiently.

The paper also proposes a new islanding identification method based on Laplacian matrix factorization that enables the use of partial refactorization techniques that facilitate real-time matrix updates under topological changes in the network. The method overcomes the challenge of dynamically updating islanding information, a limitation faced by several standard islanding identification algorithms [17]. Furthermore, the algebraic concepts underlying it can be extended to various other problems in power systems, such as network observability analysis, network partitioning for distributed state estimation, and fault isolation.

AT-NTP, built upon the algebraic concepts of [16] and the new islanding identification method, displays the following features:

- It relies solely on matrix factorization, thereby avoiding combinatorial explosion in graph search algorithms and eliminating the need for extensive AI training;
- It is generic and applicable to arbitrary substations, requiring no adaptations for different arrangements;

TABLE 1. Comparison among the proposed AT-NTP and different NTPs from the literature according to various aspects.

Reference	A1	A2	A3	A4	A5	A6	A7
[12]	-	-	-	✓	-	✓	-
[13]	-	✓	-	✓	-	✓	-
[14]	✓	✓	✓	-	-	✓	-
[15]	✓	✓	-	✓	-	✓	-
[2]	-	-	-	✓	✓	-	-
AT-NTP	✓	✓	✓	✓	✓	✓	✓

- It employs sparse matrix and partial refactorization techniques to ensure computational efficiency;
- It requires no classification of SDs by function or location, simplifies bus inclusion/exclusion in BBM, and processes MAs straightforwardly;
- It handles multiple topological changes between consecutive PMU samples in a single execution, assuming consistent status inputs;
- It is readily applicable and adaptable to various components, features, and requirements of modern EPSs.

The concept of “Topology Processing” refers to determination of the network’s BBM from SD statuses and connectivity information without explicitly accounting for possible errors [15]. Nevertheless, even assuming error-free digital status measurements, AT-NTP overcomes several limitations of existing T-NTPs, efficiently generating BBMs for SE and other EMS applications. It can also rapidly produce topological data for topology error detection tools, since many of those methods still rely on an initial BBM [7], [18], [19], [20], [21], [22], [23].

Simulation results for IEEE 14-, 39-, 118-, and 300-bus systems and for a large-scale network with 9,241 buses and other systems from the literature showed AT-NTP achieves execution times compatible with PMU sampling rates, even under complex topological changes. Unlike other studies, the present one demonstrates the feasibility and practicality of executing AT-NTP in a large-scale system with real-world characteristics and dimensions. Table 1 shows a comparison of different aspects that highlight the advantages of AT-NTP over other NTPs from the literature:

- A1 – Applicable to arbitrary substations;
- A2 – Updates the network topology without recomputing it from scratch;
- A3 – Processes detailed MAs;
- A4 – Handles multiple topological modifications in a single execution;
- A5 – Avoids the use of graph search algorithms;
- A6 – Does not rely on training data;
- A7 – Tested on large-scale networks.

D. ORGANIZATION OF THE PAPER

The remainder of the paper is organized as follows: Section II reviews the base islanding identification method [16] and introduces the proposed approach; Section III details the AT-NTP stages; Section IV presents the test scenarios

and computational results; finally, Section V provides the conclusions.

II. ISLANDING IDENTIFICATION

The method presented in [16] efficiently identifies network electrical islands and provides direct bus connectivity through the factorization of the bus/branch incidence matrix. Building upon such a foundation, this paper incorporates the islanding identification concept from [16] into the AT-NTP design and proposes a new method that leverages the Laplacian matrix to further improve computational efficiency in the real-time operation of modern EPSs.

A. BASE METHOD

Let us consider a system with \bar{n} buses and \bar{m} branches. The pseudo-oriented bus/branch incidence matrix, \mathbf{H}' , of dimension $\bar{n} \times \bar{m}$, is defined by

$$h'_{ij} = \begin{cases} 1(-1), & \text{if branch } j \text{ is connected to bus } i \text{ at} \\ & \text{the initial (final) connection point;} \\ 0, & \text{otherwise.} \end{cases} \quad (1)$$

where h'_{ij} is the element in the i^{th} row and j^{th} column of \mathbf{H}' . Initial and final connection points of each branch are chosen arbitrarily.

As proven in [16], network electrical islands can be efficiently identified through the factorization of \mathbf{H}' . Let $\mathbf{L}_H \in \mathbb{R}^{\bar{n} \times \bar{n}}$ denote the lower triangular matrix obtained from the triangular factorization of \mathbf{H}' . A factorization graph is then defined as a graph whose nodes correspond to the rows of \mathbf{L}_H and whose edges are established whenever two non-zero elements appear in the same column of \mathbf{L}_H . Therefore, the graph structure directly reflects the connectivity encoded in \mathbf{L}_H . By associating each row of \mathbf{L}_H with a bus of BBM and each column with a branch, the factorization graph naturally maps to the electrical network. A factorization path corresponds to a tree within that graph, where all nodes are interconnected [24]. Consequently, all buses belonging to the same factorization path form an electrical island [16] and islanding cases can be detected through a simple triangular factorization of \mathbf{H}' , with no graph search algorithms or other techniques prone to combinatorial explosion.

B. PROPOSED METHOD

Despite the simplicity of the method of [16], matrix \mathbf{H}' is asymmetric and rectangular, which hinders the direct use of partial refactorization methods based on factorization paths, as discussed in [25] and [26]. Partial refactorization is desirable for updating the matrix characteristics in real time in response to topological changes.

Towards overcoming that limitation, this paper proposes an islanding identification method based on the factorization of the Laplacian matrix, \mathbf{Y}' , of dimension $\bar{n} \times \bar{n}$, defined by

$$\mathbf{Y}' = \mathbf{H}'\mathbf{H}'^T \quad (2)$$

In the context of EPSs, \mathbf{Y}' can be interpreted as the nodal admittance matrix of the network, assuming all admittances are real and unitary. Its LDU decomposition yields matrix \mathbf{L}_Y , of dimension $\bar{n} \times \bar{n}$, which stores the lower triangular factors. Analogously to matrix \mathbf{L}_H in the base method, buses belonging to the same factorization path of \mathbf{L}_Y are interconnected, forming an island. Therefore, each factorization path corresponds to a distinct island disconnected from the others.

The effective use of \mathbf{Y}' for islanding identification can be established through an analogy with the observability theory of SE. Observable islands correspond to sets of buses whose state variables can be independently estimated with the use of available measurements [1]. According to [27], observable islands can be identified through analyses of the factorization paths obtained from the Gain matrix, G_{DC} , of the linear Weighted Least Squares (WLS) estimator. Theorems and corollaries in [27] guarantee each factorization path found in the lower triangular factor of G_{DC} directly corresponds to an observable island, provided only power flow measurements are represented in G_{DC} .

The matrix \mathbf{H}' , in turn, is equivalent to the transposed Jacobian matrix of the linear WLS estimator, H_{DC} , when each branch of the system is considered a fictitious active power flow measurement:

$$\mathbf{H}' = H_{DC}^T. \quad (3)$$

Although those active power flow measurements do not need to exist physically, the analogy holds, since a branch connecting buses i and j is represented in \mathbf{H}' in the same way an active power flow measurement between i and j would appear in H_{DC}^T . By adopting an identity weighting matrix, substituting (3) into (2) yields

$$\mathbf{Y}' = H_{DC}^T H_{DC} = G_{DC}. \quad (4)$$

Therefore, \mathbf{Y}' is equivalent to the definition of G_{DC} in [27]. Because each branch of the network is represented in \mathbf{Y}' as a power flow measurement and no equivalent to power injection measurement exists, all theorems and corollaries established for G_{DC} in [27] also apply to \mathbf{Y}' .

Whereas different factorization paths identified during the factorization of G_{DC} represent distinguished observable islands of the network that have no connection between them through flow measurements, similarly, each isolated factorization path identified in \mathbf{L}_Y represents an electrical island of the network that has no branch connecting it to the others. Since only matrix \mathbf{L}_Y is required, islanding detection can be performed solely by factorizing the lower triangle of \mathbf{Y}' .

An additional advantage of \mathbf{Y}' is its symmetric structure, which enables the direct application of partial refactorization methods [25], [26] that promote real-time updates of matrix characteristics in response to switching operations, avoiding full refactorization and efficiently detecting new islanding scenarios.

Finally, the proposed method is generic and applicable beyond EPSs. The Laplacian matrix provides a well-established framework for analyses of node connectivity in any graph, supporting efficient refactorization techniques to track changes in dynamic graphs with time-varying node and edge structures.

III. PROPOSED AT-NTP

AT-NTP is structured hierarchically into three stages. The first is Substation-Level Processing (SLP), where each network substation is initially fully represented in its bus-section model. At this stage, connectivity among bus-sections through SDs is verified and a reduced equivalent model is generated. The second stage is Network-Level Processing (NLP), in which the proposed islanding identification method determines the energized islands of the system and constructs the corresponding BBM. Measurement Arrangement Processing (MAP), the final, assigns the appropriate analog measurements to the energized components already represented in the BBM. Together, the three stages fulfill all functional requirements of the proposed AT-NTP.

A. SLP STAGE

Connectivity among bus-sections through closed SDs is verified in the SLP stage. All interconnected bus-sections are merged into an equivalent bus, resulting in a reduced network model that differs from BBM, since potential deenergized islands are not yet eliminated.

A pseudo-orientation is defined for each substation k with \bar{n}_{Sk} bus-sections and \bar{m}_{Sk} SDs through an arbitrary selection of initial and final connection points for each SD. The status of n^{th} SD at time t , denoted ST_n^t , is 0 (open) or 1 (closed). According to such definitions, the pseudo-oriented bus-section/SD incidence matrix $\mathbf{H}'_{Sk} \in \mathbb{R}^{\bar{n}_{Sk} \times \bar{m}_{Sk}}$ is constructed as

$$h'_{Skij} = \begin{cases} 1(-1), & \text{if SD } j \text{ is connected to} \\ & \text{bus-section } i \text{ at the initial (final)} \\ & \text{connection point and } ST_j^t = 1; \\ 0, & \text{otherwise.} \end{cases} \quad (5)$$

where h'_{Skij} is the element of \mathbf{H}'_{Sk} in row i and column j .

Although only bus-sections and SDs are represented in \mathbf{H}'_{Sk} , it still corresponds to an incidence matrix, and the zero columns, associated with open SDs, do not affect the theoretical results in [16], ensuring all supporting theorems remain valid. Therefore, the triangular factorization of \mathbf{H}'_{Sk} results in the lower triangular factor matrix \mathbf{L}_{HSk} , of $\bar{n}_{Sk} \times \bar{n}_{Sk}$ dimension. The factorization paths in \mathbf{L}_{HSk} are determined by the algorithm described in [24].

Bus-sections belonging to the same factorization path of \mathbf{L}_{HSk} are connected by closed SDs and form a single equivalent bus in the reduced network model. Part of the reduced model of the system will be constructed from a

simple factorization of \mathbf{H}'_{Sk} and according to the following changes in the network data:

- The index of the equivalent bus in the reduced model is assigned as the lowest index of the bus-sections that comprise the respective factorization path;
- The connection points of TLs, TRs, generating units (GUs), loads, synchronous condensers (SCs), and measurement instruments, among other network components, are replaced by the equivalent buses. In other words, the network components connected to each bus-section are “transferred” to the bus-section with lowest index in their respective factorization paths;
- Equivalent buses not linked to any branch are disregarded from the reduced model.

Fig. 1 illustrates the SLP procedures. In Fig. 1(a), matrix \mathbf{H}'_S is assembled for a substation modeled at the bus-section level, where bus-sections are numbered in black and SDs are numbered in blue. The i^{th} row corresponds to bus-section i , b_i , whereas the j^{th} column corresponds to SD j , d_j . In SLP, all bus-sections must be numbered, including operational or transfer bus-sections, which will likely become equivalent buses in BBM, and intermediate bus-sections. Fig. 1 (b) highlights the process of identifying equivalent buses according to the factorization paths of \mathbf{L}_{HS} for the construction of the reduced network model.

The SLP process is summarized in the flowchart of Fig. 2. The processes illustrated in Fig. 1 will be repeated for all substations belonging to set S_{SUB} . If AT-NTP is being initialized, i.e., when there is no previous network configuration to be updated, an initialization flag is triggered: $init_flag = 1$. If $init_flag = 1$, then $S_{SUB} = \Omega_{SUB}$, where Ω_{SUB} is the set consisting of all substations in the network. If $init_flag = 0$, then statuses ST_n^t and ST_n^{t-1} of all SDs, at the current time step and the previous time step, respectively, must be compared. Therefore, set S_{SUB} will consist of all substations with at least one SD whose status has changed between t and $t - 1$ and operations in unchanged substations are avoided. If $S_{SUB} = \phi$, the AT-NTP execution is terminated, for there were no changes in the network.

If $init_flag = 1$, the reduced model of the network is ensured by the factorizations of \mathbf{H}'_{Sk} -type matrices and the necessary changes in the network data. If $init_flag = 0$, the results from the SLP stage at time t for all substations k belonging to S_{SUB} should be compared with the last result obtained by SLP at the respective substations for identification of buses belonging to the following sets:

- S_{BR} : Formed by equivalent buses that had at least one adjacent branch removed or inserted, modifying the set of adjacent branches assigned to the respective bus in the last SLP execution;
- S_{SH} : Formed by equivalent buses that had at least one shunt component removed or inserted, modifying the set of shunt components assigned to the respective bus in the last SLP execution;
- S_{NE} : Formed by buses that are (were) interconnected with those belonging to S_{BR} through branches included

in (excluded from) the set of adjacent branches to the buses in S_{BR} .

Those sets provide input to the next AT-NTP stages. In summary, the SLP stage identifies equivalent buses and directly and generically reassigns the connection points of network components. There is no feature in the structure of matrices \mathbf{H}'_{Sk} that restricts their use to specific substations. Given the SD statuses and their connection points, the factorization of \mathbf{H}'_{Sk} enables the identification of interconnected bus-sections regardless of their physical distribution. SLP operates even for substations in which bus-sections are located at different voltage levels, such as bus-sections b_1 , b_4 , and b_{10} in Fig. 1(a), which are separated from the other bus-sections by a TR. Consequently, the SLP stage applies to substations with arbitrary arrangements.

The SLP stage is therefore used to determine the equivalent buses and the new connection points of any component connected to the bus-sections of the substations. Those components may range from traditional elements, such as TRs, TLs, and measurement instruments, to more advanced ones, including Flexible AC Transmission Systems (FACTS) devices and High Voltage Direct Current (HVDC) line interconnections. Although those devices rely on power electronic switches, they are connected to the bus-sections through SDs; therefore, their connectivity can be determined by the AT-NTP.

FACTS devices can be classified as shunt elements (e.g., Static Var Compensator (SVC)), series devices (e.g., Thyristor Controlled Series Compensator (TCSC)), or combined series-shunt devices (e.g., Unified Power Flow Controller (UPFC)) [28]. Although such devices may include advanced protection schemes, they are connected to the network bus-sections through SDs, whose statuses are transmitted to the control centers. Therefore, AT-NTP can handle the devices in a similar manner to any other traditional network component. Shunt devices are treated similarly to capacitor banks, reactors, and loads, and series devices can be modeled as branches, such as TLs or TRs. Finally, components that combine both characteristics can be represented as a branch associated with a shunt element.

A similar reasoning applies to HVDC systems, which are connected to the AC network through converter stations [29], [30]. Although the specific configuration of each converter station depends on type of power electronic converter adopted, all of them are connected to bus-sections via SDs. Consequently, AT-NTP can be used to determine the connectivity of converters with the grid and to identify substations and respective buses interconnected through HVDC links. AT-NTP is flexible and can be easily applied and adapted to accommodating different components, characteristics, and requirements of modern EPSs.

B. NLP STAGE

The NLP stage aims to obtain the network BBM by identifying energized islands in the reduced model and eliminating de-energized ones. Since SDs are no longer

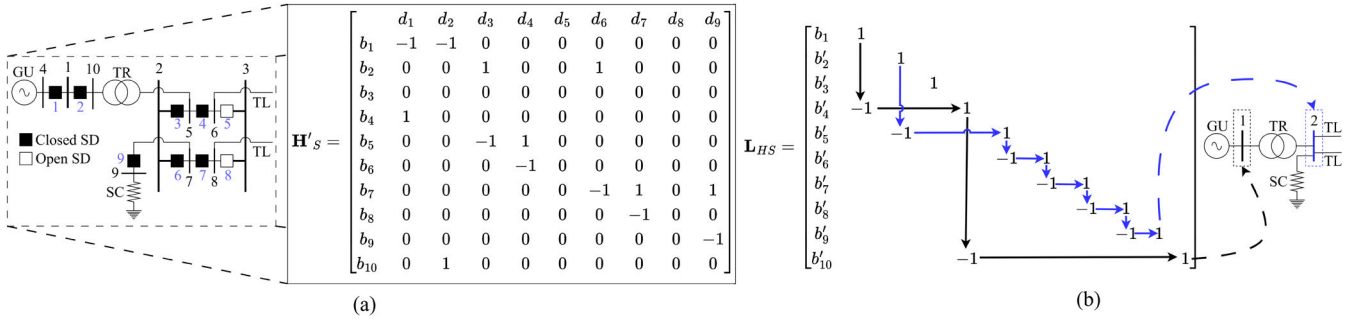


FIGURE 1. SLP stage. (a) Construction of matrix H'_S based on the bus-section model of the substation. (b) Identification of equivalent buses from the factorization paths of matrix L_{HS} .

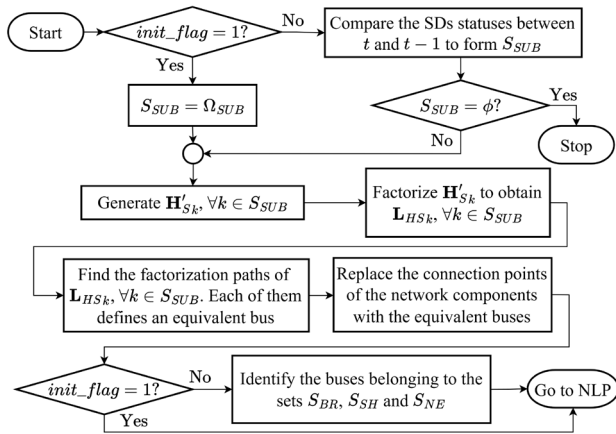


FIGURE 2. Flowchart of the SLP stage.

explicitly represented, the proposed islanding identification method is applied directly and in conjunction with partial matrix refactorization techniques.

AT-NTP initialization ($init_flag = 1$) requires no matrix refactorizing; instead, the proposed method is applied directly. Given a system with \bar{n}_S bus-sections, the Laplacian matrix at the current time step, Y'_t , of dimension $\bar{n}_S \times \bar{n}_S$, is constructed according to the definition provided in (2). The new connection points of the branches identified in SLP are used for the construction of Y'_t .

The dimension of Y'_t incorporates all bus-sections as potential network buses. Consequently, the respective rows and columns in Y'_t of all bus-sections replaced by an equivalent bus will be filled with zeros. The strategy follows an approach similar to that of [26]. All bus-sections are represented in Y'_t for preventing possible reordering and changes in the matrix dimension due to inclusion and exclusion of buses in substations, enabling AT-NTP to handle any topological modifications straightforwardly. The zero rows and columns in Y'_t do not impact the computational efficiency of the method when sparsity techniques are employed.

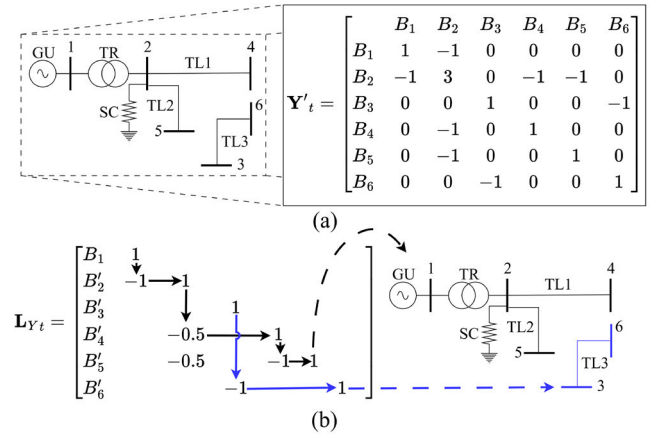


FIGURE 3. Illustration of the proposed method for islanding identification. (a) Construction of matrix Y'_t from the reduced network model. (b) Identification of electrical islands based on the factorization paths of matrix L_{Y_t} .

According to the proposed method, matrix L_{Y_t} is obtained from the lower triangular factorization of Y'_t . Each factorization path in L_{Y_t} corresponds to an electrical island in the network so that only the identification of energized islands is required. De-energized islands, along with all associated buses and equipment, are eliminated from the final BBM. An island is considered energized if it contains at least one bus connected to a GU. However, the method is flexible enough to incorporating other criteria for determining whether an island is energized, according to the modeling of a specific generation type or available measurements.

Fig. 3 illustrates the proposed method for islanding identification used in NLP when $init_flag = 1$. In Fig. 3(a), matrix Y'_t is assembled from the reduced network model, where B_i denotes the i^{th} equivalent bus. For simplicity, only the equivalent buses are represented in Y'_t in Fig. 3 – the remaining rows and columns filled with zeros have been omitted. Fig. 3 (b) shows the identification of electrical islands in the network according to the factorization paths of L_{Y_t} .

When a prior topology must be updated ($init_flag = 0$), then matrix Y'_{t-1} must be refactored to update the network

islands. Structural modifications in \mathbf{Y}'_{t-1} occur only when the connection points of branches change. The rows and columns of \mathbf{Y}'_{t-1} to be modified correspond to the buses in $S_{BR} \cup S_{NE}$. Since those modifications affect only the elements in the factorization paths of $\mathbf{L}_{Y_{t-1}}$ traced from those buses [25], the refactorization process is limited to the buses belonging to those paths. That set of buses, which are involved in the refactorization process within the NLP stage, forms set S_{RF} .

Different partial refactorization methods can refactor the rows and columns of \mathbf{Y}'_{t-1} belonging to S_{RF} . In this study, Method 1, described in [25] and which applies the triangular factors of $\mathbf{L}_{Y_{t-1}}$ associated with S_{RF} , restores the relevant portions of \mathbf{Y}'_{t-1} . The process then proceeds with structural modifications and a refactorization of the rows and columns of \mathbf{Y}'_{t-1} belonging to S_{RF} for obtaining updated matrices \mathbf{Y}'_t and \mathbf{L}_{Y_t} . Simple modifications to existing positions in the matrix can represent addition or removal of buses in BBM. The NLP stage concludes with the identification of islands based on the factorization paths in the updated \mathbf{L}_{Y_t} matrix and the elimination of de-energized islands.

Although partial refactorization can improve execution times, it involves more steps than simply assembling and factoring a new matrix, as performed during NLP initialization ($init_flag = 1$). Therefore, it is advantageous only if the portion of the matrix to be refactored is not excessively large. Conversely, several factors can lead to a large number of rows and columns requiring refactorization, including number of buses in $S_{BR} \cup S_{NE}$, their positions in the matrix, and depth of the factorization paths traced from them.

Let \bar{n}_{et-1} be the number of equivalent buses identified in the SLP stage at the previous time step and \bar{n}_{RFt} the number of buses in S_{RF} . A heuristic solution was adopted for preventing partial refactorization from becoming more time-consuming than a full factorization in complex cases. Partial refactorization is performed only if $\bar{n}_{RFt} \leq \eta \cdot \bar{n}_{et-1}$, where η is a scaling factor ranging from 0 to 1. If $\bar{n}_{RFt} > \eta \cdot \bar{n}_{et-1}$, a new \mathbf{Y}'_t matrix is assembled and factored, similarly to the process when $init_flag = 1$. In this study, η was set to 0.5, meaning the method defaults to full factorization if more than 50% of the network requires an update.

The choice of $\eta = 0.5$, however, is not a definitive solution. The value was selected because the refactorization method in this study requires a double sweep of \mathbf{Y}'_{t-1} to reconstruct, modify, and subsequently refactor the affected portions of the matrix. Therefore, if more than 50% of the matrix needs to be refactored, the refactorization process may not be significantly more efficient than simply factorizing a new \mathbf{Y}'_t matrix. Nonetheless, defining the optimal value of η depends on several factors, including system size, structure of the factorization paths, and the specific refactorization method adopted. Future studies may investigate the impact of η on AT-NTP performance and explore adaptive tuning strategies for its adjustment.

Regardless of the refactorization strategy, the NLP stage is designed to handle multiple topological changes between

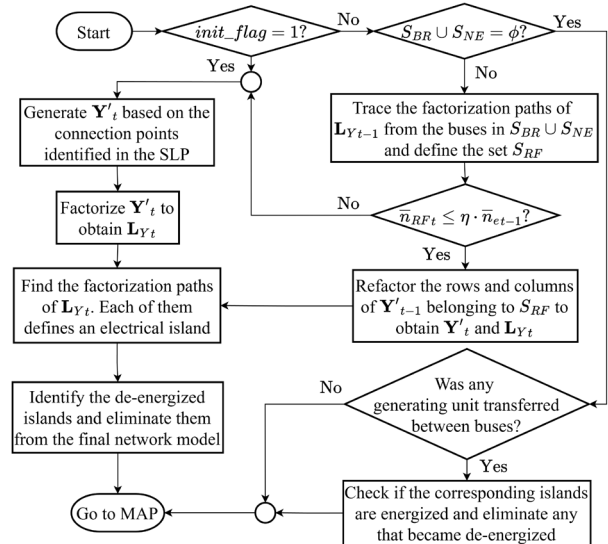


FIGURE 4. Flowchart of the NLP stage.

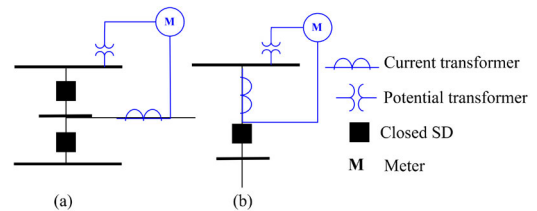


FIGURE 5. Measurement arrangements considered in this study.

two consecutive time steps within a single execution. If $S_{BR} \cup S_{NE} = \phi$, then no branch connection points have been modified, making partial refactorization unnecessary. Nevertheless, if $S_{SH} \neq \phi$ due to the transfer of a GU from one equivalent bus to another, the corresponding islands must be checked to determine if any of those islands became de-energized. The steps of the NLP stage are summarized in the flowchart in Fig. 4.

C. MAP STAGE

The MAP stage assigns appropriate measurements to BBM components. This study adopted the signal acquisition arrangements shown in Fig. 5, which are consistent with those presented in [14]. The stage processes signals from Current Transformers (CT) and Potential Transformers (PT), which are acquired by either a PMU for voltage and current phasor measurements, or an active and reactive power meter in SCADA systems. The MAP stage can be easily adapted for other MAs.

Depending on type of measurement device and acquisition system, the processing procedures differ slightly. The analysis is straightforward for PMU MAs. In the SLP stage, the connection points of CTs and PTs are replaced by their equivalent buses. If a PT is connected to an energized bus, a phasor voltage measurement is assigned to that bus.

Similarly, if a CT is linked to an energized bus and is adjacent to a branch, it is converted into a phasor current flow measurement. A CT adjacent to a shunt component can contribute to a net current injection measurement at the bus. Although uncommon in PMU-monitored systems, the proposed AT-NTP can handle scenarios that include current injection measurements.

For active and reactive power MAs, CT, PT, and the equipment whose active and reactive powers are being measured must be linked to the same bus. If any of those components are connected to different equivalent buses, at least one SD in the MA is open and the measurement must be discarded. Those MAs are then converted into a pair of active and reactive power flow measurements in a branch, provided CT, PT, and the monitored branch are connected to the same equivalent bus. If CT is adjacent to a shunt component, the arrangement may contribute to a net power injection measurement at the bus.

During AT-NTP initialization (*init_flag* = 1), all MAs located in energized islands are processed in the MAP stage for assigning measurements to BBM components. In contrast, when a prior topology is being updated (*init_flag* = 0), the process analyzes only MAs linked to energized buses in set $S_{BR} \cup S_{SH} \cup S_{NE}$, since only the measurements at those buses may have changed compared to the previous time step - measurements assigned to other network components remain unchanged.

Upon completion of the MAP stage, AT-NTP provides the network's final BBM. All de-energized buses and components are removed and the measurements are correctly assigned to the network's final configuration. The network topology is provided through output files containing lists of equivalent bus IDs, data, and parameters of other network components, with their connection points replaced by the corresponding equivalent buses and the locations of measurements within BBM. Only buses, equipment, and measurements located in energized islands are included, whereas de-energized system elements are omitted. Those lists can be readily adapted to the input file formats of state estimators, power flow analysis tools, and short-circuit calculation programs, among other EMS applications.

IV. SIMULATIONS AND RESULTS

A. TEST SYSTEMS

Simulations evaluated the computational efficiency of the proposed AT-NTP and its ability to generate network BBM within execution times compatible with PMU high sampling rates. AT-NTP was implemented in C by sparse matrix techniques for all stages and the code was executed on an Intel Core i9-14900 processor with 64 GB of RAM. AT-NTP was implemented as a fully sequential program, with no parallelization in any stage, and tests were conducted on different EPSs, including IEEE 14-, 39-, 118-, and 300-bus systems, 9,241-bus PEGASE Pan European Extra High Voltage (EHV) network [31], [32], IEEE Reliability Test

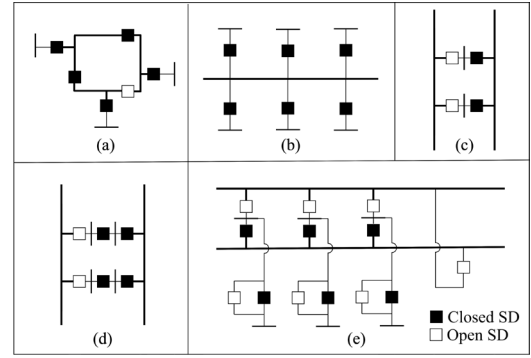


FIGURE 6. Substation bus arrangements considered in this study.

System 1996 used in [15], and the modified two-area, four-machine power system employed in [2].

IEEE systems were selected for analyses of scalability of AT-NTP in benchmark networks widely reported in the literature, whereas the 9,241-bus network assessed its performance in a real, large-scale power system. Conversely, IEEE Reliability Test System 1996 and the modified two-area, four-machine system were included specifically to enable a quantitative comparison with representative graph-search-based and AI-based NTPs reported in [15] and [2], respectively.

Since the 9,241-bus network and IEEE 14-, 39-, 118-, and 300-bus systems are represented only in BBM, they were modeled at the bus-section level using the substation arrangements shown in Fig. 6, which displays the substation bus arrangements considered, namely, (a) Ring Bus Arrangement (RBA), (b) traditional Single Bus Arrangement (SBA), (c) Double Bus Double Breaker Arrangement (DBDBA), and (d) Breaker-and-a-Half Arrangement (BHA). Those configurations are described in [2]. The arrangement shown in Fig. 6(e) is commonly adopted in the Brazilian interconnected power system, allowing the isolation of any breaker or bus without service interruption.

IEEE 14-bus system was divided into ten substations, whereas each bus in IEEE 39-, 118-, and 300-bus systems and in the 9,241-bus network was represented as a single substation. The 14-bus system and its bus-section level model (Fig. 7) are described in detail towards illustrating the proposed modeling approach.

For those test systems, MAs were distributed to monitor power or current phasor flows in branches, injections in shunt components, and voltage phasors at each bus. Table 2 provides a comparison of the sizes of the systems modeled at the bus-section level, including number of substations (N_{SUB}), bus-sections (\bar{n}_S), branches (\bar{m}), SDs (\bar{m}_S), shunt components (N_{SH}), and MAs (N_{MA}).

B. TESTS ON IEEE SYSTEMS

Three scenarios were constructed for the IEEE systems. The first involved executing AT-NTP 10,000 times for each system with *init_flag* = 1. The test evaluated the AT-NTP's initialization time, starting from a state with no prior

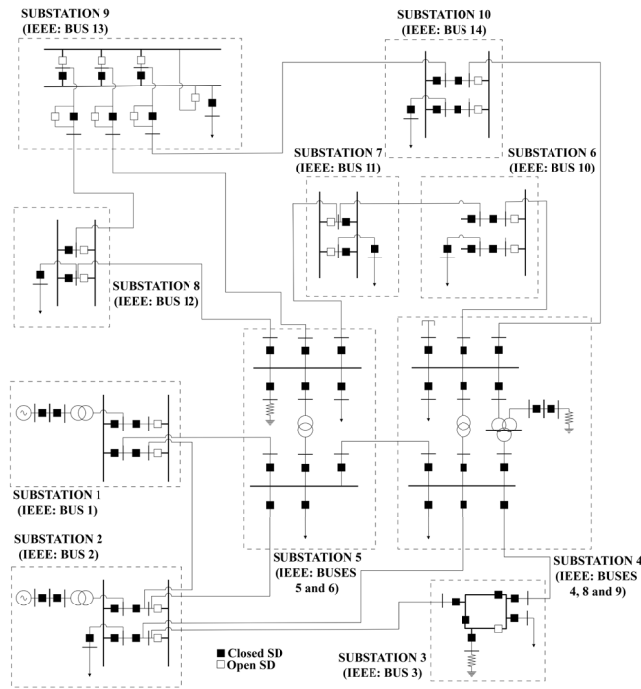


FIGURE 7. IEEE 14-bus system modeled at the bus-section level.

TABLE 2. Sizes of the systems modeled at the bus-section level in this study.

	14-bus	39-bus	118-bus	300-bus	9,241-bus
N_{SUB}	10	39	118	300	9,241
\bar{n}_S	90	206	816	1,848	70,546
\bar{m}	22	46	186	411	16,049
\bar{m}_S	87	202	839	1,900	76,272
N_{SH}	17	31	167	299	13,667
N_{MA}	56	124	539	1,121	45,765

configuration. The second scenario evaluated the time taken by AT-NTP to update the network topology in response to a single change, such as status change of a single SD. AT-NTP was executed 100 times with $init_flag = 0$, performing a single SD status change for each SD in the network for all SDs of each system considered. The third scenario analyzed the time to update the network topology in response to multiple changes. 10,000 random scenarios were generated for the 300-bus system through a random selection of 1% to 10% of its substations. The status of all SDs within the selected substations was altered from the initial AT-NTP topology for each scenario, and AT-NTP was executed 100 times with $init_flag = 0$ for each sample.

The bus-sections in Y^t matrix were ordered for all the systems, according to number of incident branches at each bus-section, with those with fewer incident branches placed first. Such a simple ordering strategy represents a low-complexity approach to matrix ordering, reducing fill-ins during factorization, hence, both memory usage and execution time. Although more advanced ordering techniques might be employed, the method was sufficient to demonstrate the AT-NTP's performance under challenging conditions.

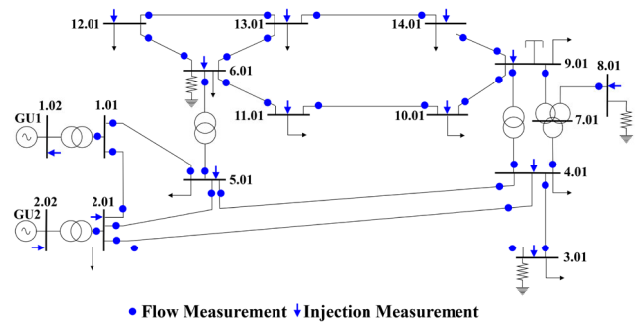


FIGURE 8. BBM of the IEEE 14-Bus system obtained from the AT-NTP output files.

TABLE 3. Initialization time of the proposed AT-NTP in the IEEE systems.

System	14-bus	39-bus	118-bus	300-bus
Min	24.08 μ s	40.93 μ s	212.74 μ s	561.82 μ s
Mean	38.94 μ s	60.74 μ s	234.96 μ s	620.17 μ s
Max	106.12 μ s	158.38 μ s	758.23 μ s	1,356.91 μ s
Std	6.63 μ s	13.32 μ s	14.80 μ s	39.33 μ s

Towards illustrating an example of the results of AT-NTP, Fig. 8 shows the BBM of the 14-bus system, constructed from AT-NTP output files during initialization with the use of the SD statuses in Fig. 7. The result in Fig. 8 corresponds to the expected standard configuration of the 14-bus system, with the connection points of system components properly replaced by the equivalent buses. Additional buses 1.02 and 2.02 represent the connection points of generators GU1 and GU2, respectively. Fig. 8 also shows the measurements properly allocated to the system components in BBM, where flow and injection measurements may represent either current phasor, or active and reactive power measurements, depending on the meter associated with MA, which can be a PMU or a typical SCADA power meter. Although voltage measurements are not explicitly shown in Fig. 8, they are embedded within flow and injection measurements, since they share the same PTs in the MAs of Fig. 5.

Table 3, on the other hand, provides minimum (Min), mean, and maximum (Max) execution times, as well as the standard deviation (Std) for the initialization of AT-NTP in each IEEE system. The mean execution time remained under 1 millisecond for all cases, even for the 300-bus system with 1,848 bus-sections and 1,900 SDs. In real-time operations, the time between two consecutive PMU samples at a rate of 60 measurements per second is approximately 16 milliseconds. Therefore, the AT-NTP's initialization time is well within the required time for PMU-based applications. The maximum values in Table 3 correspond to outliers and account for less than 1% of the recorded results.

Despite the considerably low execution times, the results in Table 3 correspond to AT-NTP initialization, a situation that requires processing the entire network. Therefore, execution times are expected to be even lower when a pre-existing topology is being updated. Fig. 9 displays the results of the second test scenario, showing AT-NTP considerably

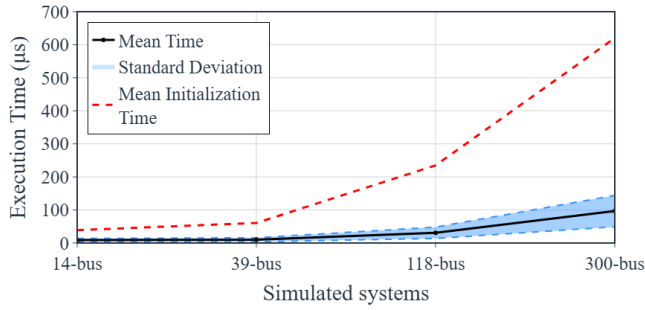


FIGURE 9. Execution time of AT-NTP for changes in a single SD in IEEE systems.

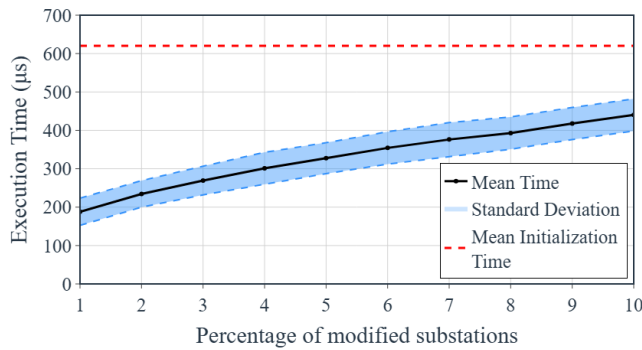


FIGURE 10. Execution time of AT-NTP according to percentage of modified substations in IEEE 300-bus system.

reduced its execution time when updating the network due to changes in a single SD at a time, staying within the order of tens of microseconds in most cases, even for larger systems. Execution times were reduced substantially even for changes involving buses located at the beginning of matrix \mathbf{Y}'_{t-1} , which may show deeper factorization paths than buses located at the final elements of the main diagonal of \mathbf{Y}'_{t-1} , imposing greater challenges to the refactorization process.

Fig. 10 displays the results of the third test scenario in the largest IEEE test system considered, namely, IEEE 300-bus system. AT-NTP execution time increased in more complex cases, in which entire substations were modified simultaneously. Concurrent changes to all SDs in multiple substations result in several simultaneous topological modifications according to the substation arrangement. In such situations, shunt elements, including GUs, loads, and capacitor banks were disconnected, substations were split into multiple buses in BBM, and number of electrical islands can vary.

Fig. 11 shows minimum, mean, and maximum number of buses in the final BBMs generated by AT-NTP for different percentages of modified substations in IEEE 300-bus system and Fig. 12 displays the corresponding number of energized electrical islands. According to the figures, the network topologies obtained in the simulated scenarios underwent significant changes compared to the standard IEEE 300-bus system configuration used during AT-NTP initialization. In some cases, the number of buses in the final BBM was lower than 300, indicating bus removals caused by de-energization after GU disconnections. In other

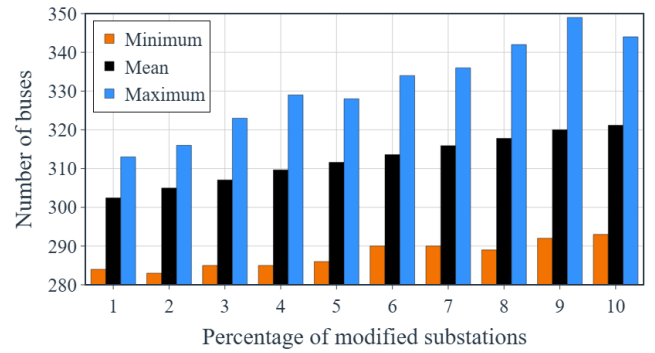


FIGURE 11. Minimum, mean, and maximum number of buses in the final BBM obtained with AT-NTP for different percentages of modified substations in IEEE 300-bus system.

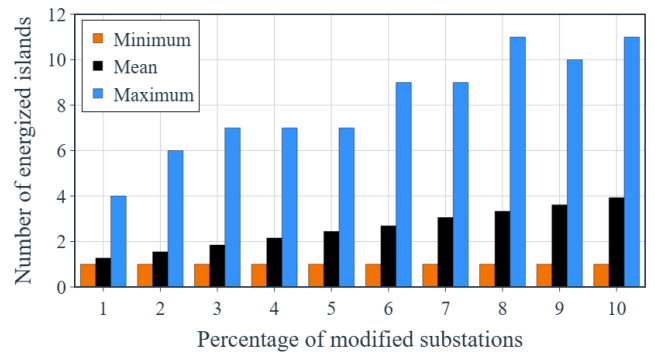


FIGURE 12. Minimum, mean, and maximum number of energized islands in the final BBM obtained with AT-NTP for different percentages of modified substations in IEEE 300-bus system.

cases, the number of buses exceeded 300, reflecting the splitting of substations into two or more buses. The results ranged from BBMs consisting of a single electrical island to multiple independently energized islands. Nevertheless, AT-NTP processed multiple modifications in a single execution, requiring less time than the initialization stage (Fig. 10).

Although simultaneous modifications across multiple substations between two consecutive PMU samples are unlikely in practice, the tests revealed AT-NTP can efficiently handle severe and highly nonlocal topological changes with low computational cost. Under typical operating conditions, when only a small number of SDs changes status within each PMU reporting interval, the execution times are expected to be even shorter than those reported for the stress-test scenarios.

C. TESTS ON THE LARGE-SCALE SYSTEM

Two scenarios were simulated on the 9,241-bus network for evaluation of the AT-NTP performance in a large-scale real system. In the first, AT-NTP was executed 100 times with *init_flag* = 1 for assessment of initialization time, whereas in the second, four substations were selected and AT-NTP was executed 100 times with *init_flag* = 0 for each of them, thus modifying the statuses of all SDs in the corresponding substation. The test evaluated the time required by AT-NTP to update the system topology in response to changes in a

TABLE 4. Execution times of AT-NTP in the 9,241-bus network during initialization (*init_flag* = 1) and for single-substation changes (*init_flag* = 0).

	<i>init_flag</i> = 1	<i>init_flag</i> = 0
Min	209.44ms	46.78ms
Mean	221.25ms	52.46ms
Max	279.82ms	62.47ms
Std	13.20ms	3.40ms

TABLE 5. Execution times of the SLP stage in substations 8 and 4 of the 14-bus system.

	Substation 8	Substation 4
Min	0.19 μ s	4.23 μ s
Mean	0.21 μ s	5.72 μ s
Max	0.24 μ s	7.19 μ s
Std	0.01 μ s	0.39 μ s

single substation. The substations in the second scenario were selected so that the changes would affect different positions along the main diagonal of matrix \mathbf{Y}'_t , including beginning, some intermediate regions, and end of the matrix.

Due to its large size, the bus-sections in the \mathbf{Y}'_t matrix of the 9,241-bus network were ordered by the Approximate Minimum Degree (AMD) algorithm, as in [33], which provides a more efficient strategy than the simple ordering used for IEEE systems. Table 4 provides minimum, mean, and maximum execution times, as well as the standard deviation for the two aforementioned scenarios. The results indicate even for a large-scale real system with 70,546 bus-sections and 76,272 SDs, the AT-NTP execution time remained within the millisecond range. Although the mean execution time required to update the network topology was 52.46 milliseconds, which exceeds the 16-millisecond sampling interval of PMUs operating at 60 samples per second, it is still within the same order of magnitude of that required by PMU-based applications. Moreover, several strategies can be adopted for further reducing the execution time of AT-NTP.

Since AT-NTP was implemented as a fully sequential program with no parallelization in any stage, greater efficiency could be achieved through parallelization. A potential approach is to parallelize the SLP stage, for the factorization of \mathbf{H}'_{Sk} matrices and the identification of equivalent buses can be performed independently for each substation. In this setup, only NLP and MAP stages remain centralized. Table 5 shows the SLP execution times for substations 8 and 4 of IEEE 14-bus system, representing smallest and largest substations, respectively, in the simulated systems. Table 6 provides the NLP and MAP execution times during AT-NTP initialization.

The results in Tables 5 and 6 indicate parallelizing the SLP stage would significantly reduce the AT-NTP initialization time compared to the values in Table 3 for IEEE systems. In this configuration, the total execution time would be dominated by (i) the SLP time of the largest substation plus (ii) the centralized NLP and MAP times. The reduction in execution time is less pronounced for the 9,241-bus

TABLE 6. Initialization times of NLP and MAP stages.

System	14-bus	39-bus	118-bus	300-bus	9,241-bus
Min	8.40 μ s	21.60 μ s	99.10 μ s	335.30 μ s	196.89ms
Mean	12.02 μ s	28.72 μ s	102.48 μ s	352.67 μ s	198.19ms
Max	22.10 μ s	36.18 μ s	132.15 μ s	381.08 μ s	201.60ms
Std	2.48 μ s	5.34 μ s	4.35 μ s	7.03 μ s	0.84ms

TABLE 7. Comparison of AT-NTP initialization times in the 9,241-bus network for different ordering strategies.

	Simple ordering	AMD
Min	2,016.98ms	209.44ms
Mean	2,025.56ms	221.25ms
Max	2,148.38ms	279.82ms
Std	19.44ms	13.20ms

network. Nevertheless, other approaches can be adopted, including implementation of decentralized architectures in which EPSs are divided into subsystems processed in parallel, as discussed in [15]. According to the results for IEEE systems, the parallel execution of AT-NTP can be significantly faster than the required processing time for subsystems with hundreds of buses.

Furthermore, the ordering strategy significantly impacts the execution time of factorization algorithms. Table 7 compares AT-NTP initialization times for the 9,241-bus network using the simple ordering applied to IEEE systems and AMD algorithm. Changing the ordering alone resulted in a substantial reduction in execution time. Therefore, employing other more efficient ordering strategies would further reduce execution times [34], [35]. The ordering of bus-sections can be performed offline and does not affect any stage of the proposed AT-NTP.

The code was executed on a personal computer; consequently, additional reductions in execution time can be achieved by enabling multithreading and by running the algorithm on machines with greater processing capabilities, such as those typically available in large control centers.

D. COMPARATIVE TESTS

Tests on IEEE Reliability Test System 1996 and the modified two-area, four-machine power system compared the performance of AT-NTP with other NTPs from the literature [2], [15]. AT-NTP follows the conventional definition of NTPs [1], which are deterministic algorithms, i.e., given a specific combination of SD statuses, they produce a unique BBM topology. Since conventional NTPs are not designed to handle topological errors, they converge to the same BBM topology for a given SD configuration, even when some statuses are erroneous. The mathematical framework and examples presented in this study ensure AT-NTP reaches the expected topology given the input status measurements. Consequently, the comparison between AT-NTP and other approaches from the literature will be limited to execution times.

IEEE Reliability Test System 1996 is the largest system that simulates the T-NTP presented in [15], which

TABLE 8. Comparison of execution times in IEEE reliability test system 1996 scenarios.

		AT-NTP	T-NTP [15]
Scenario 1	Min	39.92 μ s	-
	Mean	52.47 μ s	5,400.00 μ s
	Max	78.70 μ s	-
	Std	9.48 μ s	-
Scenario 2	Min	34.79 μ s	-
	Mean	46.81 μ s	6,600.00 μ s
	Max	76.26 μ s	-
	Std	9.88 μ s	-
Scenario 3	Min	44.82 μ s	-
	Mean	60.60 μ s	6,400.00 μ s
	Max	104.36 μ s	-
	Std	11.83 μ s	-

represents an efficient T-NTP approach based on graph search algorithms. The system comprises 24 substations, 66 branches, and 118 SDs and three scenarios were executed on it, as detailed in [15], involving simultaneous changes in multiple SDs distributed across the network. The same three scenarios were simulated by AT-NTP with a simple ordering strategy - the corresponding execution times and the mean execution times of T-NTP reported in [15] for the respective tests are provided in Table 8.

The AT-NTP results were directly compared with those from [15] for the T-NTP implemented in MATLAB and executed on a computer with an Intel Core i7-2600 processor. Although T-NTP in [15] was executed on a computer with lower processing capacity, the execution times achieved by AT-NTP were more than 100 times shorter across all simulated scenarios, underscoring its computational efficiency. In addition to its numerical performance, AT-NTP also offers important theoretical advantages.

Unlike T-NTP, AT-NTP does not rely on the classification of SDs, or the creation of fictitious ones. Moreover, both addition and removal of buses in BBM and assignment of indices are straightforward. Those features enable AT-NTP to handle diverse topological changes directly and to be easily adapted to different substation arrangements, MAs, and new equipment in EPSs. Furthermore, AT-NTP introduces a new perspective on the topology processing problem, demonstrating NTPs can be formulated using matrix factorization and refactorization routines, techniques that are already standard in most EPS analysis tools. In summary, AT-NTP is simple to implement and can be further optimized through its combination with advanced refactorization or ordering strategies.

After comparison of AT-NTP with graph-based T-NTP, additional tests evaluated its performance against AI-NTP proposed in [2]. The first three case studies presented in [2] for the modified two-area, four-machine power system were replicated. The system comprises 20 substations, 34 branches, and 85 SDs. The simulated cases, detailed in [2], involve interruption of a single TL, outage of a generating plant, and division of the network into two areas. In [2], only mean time and standard deviation for all scenarios

TABLE 9. Comparison of execution times in the modified two-area, four-machine power system.

	AT-NTP	AI-NTP [2]	
		LDM	NN
Min	7.68 μ s	-	-
Mean	15.22 μ s	11.38 μ s	27.54 μ s
Max	36.25 μ s	-	-
Std	4.49 μ s	0.66 μ s	0.27 μ s

combined were reported with the use of two different AI algorithms, logical decision-making (LDM), and an artificial neural network (NN), as classifiers. Those AI-NTP versions were implemented in MATLAB with parallel processing and executed on a system equipped with an Intel Xeon(R) Gold processor and 63.7 GB of RAM [2].

Table 9 summarizes the computational performance of AT-NTP for the selected case studies and compares its execution times with those reported in [2] for the same scenarios, considering AI-NTP implemented with both LDM and NN classifiers. According to the results, despite being implemented as a fully sequential program, AT-NTP achieves execution times comparable to those of AI-NTP, which was implemented and executed using parallel processing.

Unlike conventional NTPs, defined in [1] and [15] as deterministic processors that determine the network topology solely from SD status information, the AI-NTP proposed in [2] also processes voltage and current phasor measurements, allowing it to handle potential topological errors. However, AI-NTP depends on a specific training strategy for each substation arrangement. In other words, new training procedures must be developed and adapted for substations not included in the examples presented in [2], such as the arrangement shown in Fig. 6(e), used in previous systems. Moreover, AI-based algorithms require large volumes of data for training and the acquisition, storage, and processing of that information can become complex or even impractical in large-scale real systems.

As addressed elsewhere, unlike the data-driven nature of AI-NTPs, AT-NTP follows the conventional deterministic framework of topology processors. Although it was not specifically designed to handle topological errors, the results show it is efficient, scalable to large systems, and independent of large data volumes or adaptations for different substation configurations, and its efficiency and simplicity enable straightforward integration with other tools for topology error processing.

Given those results, both scope and limitations of the performance comparisons must be clarified. A direct comparison between AT-NTP execution times and those reported in [2], [15] for other NTPs under the same scenarios has certain limitations. The algorithms were implemented in different programming languages and executed on distinct hardware platforms. However, since the source codes of the NTPs proposed in [2] and [15] are not publicly available, it would not be fair to compare AT-NTP with independent implementations of those NTPs. Even so, the execution

times reported in [2] and [15] were sufficient to highlight the advantages of AT-NTP. Moreover, versions of AT-NTP are available in a public repository to support further more comprehensive comparative studies [36].

E. DISCUSSIONS AND PRACTICAL LIMITATIONS

Tests confirmed the efficiency of AT-NTP and its applicability to large-scale, real-world EPSs monitored by PMUs. Given a set of SD statuses, AT-NTP rapidly generates the corresponding BBM, with measurements properly allocated. Such information forms the basis for executing various EMS applications within time frames compatible with PMU sampling rates, thereby supporting real-time operation and decision-making in modern EPSs [1], [2], [3]. In addition to its computational efficiency, AT-NTP is straightforward to implement and can be easily adapted to new equipment, emerging technologies, and evolving network requirements.

Despite the advantages, AT-NTP assumes status measurements are error-free. However, in practical situations, errors in SD statuses may occur and compromise the results, since conventional NTPs are generally not designed to handle topological errors [1], [15]. Some studies monitor voltage and current phasor measurements for detecting possible errors in SD statuses and providing more reliable information to NTPs [7], [18] towards estimating the correct network topology.

Other studies rely on generalized SE, in which SD statuses are estimated jointly with other state variables. However, due to the large amount of information involved in EPSs modeled at the bus-section level, detailed substation modeling is typically restricted to regions suspected of containing topology errors, while the remainder of the network is kept represented in BBM [19], [20], [21], [22], [23]. Consequently, conventional NTPs remain necessary, even though they are not capable of processing topological errors [1], [15]. In this context, AT-NTP can be seamlessly integrated with any of those approaches, for it provides all structural and measurement information required by generalized estimators and other tools for topology error detection and correction.

Another practical concern involves the lack of synchronization among status measurements, which may arise from communication delays or from differing sampling rates, as commonly observed between PMU and SCADA data streams. Some studies have already addressed the issue in the context of SE [37]. Nevertheless, future research will extend this investigation to the context of topological errors.

Finally, although this study focused on transmission systems, nothing in the AT-NTP design restricts its applicability to them. Future work could assess its performance in distribution networks, since, in such systems, all interconnected buses without SDs can be grouped into sections to reducing the network size and facilitating island identification. Moreover, the subdivision of the grid into feeders enables the parallel execution of AT-NTP, which may further enhance its scalability in large distribution systems.

V. CONCLUSION

This paper introduced AT-NTP, a hierarchical topology processor that provides fast and reliable topology updates for modern EPSs monitored by PMUs. By combining substation-level processing, network-level islanding identification, and measurement-arrangement processing, AT-NTP incrementally updates BBM without recomputing it from scratch. The method relies entirely on algebraic formulations, avoiding graph search algorithms and artificial intelligence techniques. It is simple to implement, applicable to arbitrary substation configurations, and suitable for integration with existing EMS tools. Simulation results on several benchmarks and a large-scale real network demonstrated AT-NTP correctly identifies switching events, island formation, and bus merging/splitting with high computational efficiency, provided that status data are reliable, confirming its potential for real-time applications.

Although the study focused on transmission systems, the proposed islanding identification method is generic and broadly applicable. Since the Laplacian matrix is a fundamental construct in graph theory, the approach can be extended to other networked systems, supporting the efficient detection and tracking of connectivity changes in dynamic, time-varying graphs. Future research will explore the joint operation of AT-NTP with topology-error detection methods, address the impact of measurement asynchronism, investigate adaptive strategies for tuning the scaling factor used in NLP refactorization, and assess its applicability to distribution systems.

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