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A 2.488 Gb/s GaAs 1:4/1:16 Demultiplexer IC with Skip Circuit for Sonet STS-12/48 Systems

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A 2.488 Gb/s GaAs 1:4/1:16 DEMULTIPLEXER IC WITH SKIP CIRCUIT FOR SONET STS-12/48 SYSTEMS

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Abstract

A 1:4/1:16 demultiplexer IC with an integrated skip circuit has been successfully designed and fabricated employing SCFL standard cells based on 1 μm MESFET foundry technology. The circuit was designed to operate up to 2.5 Gb/s with low power dissipation. The demultiplexer employs a tree type architecture based on 1:2 demux blocks using Tristage flip-flops. A new skip circuit without re-timing was proposed and integrated to the demultiplexer for frame alignment purposes. The proposed skip circuit demonstrated its effectiveness and the IC operated either as a 1:4 or a 1:16 demultiplexer up to 2.5 Gb/s with power dissipation of 1.4 W. This IC is applicable for signal processing on SONET STS-12/48 optical communication systems

1. INTRODUCTION

The increase in the communication needs over all the word in the last years stimulated the development of optical communication systems with high data capacity employing ICs operating at Gb/s rates. By the other hand, the emergence of GaAs foundries gave customers the access to well established GaAs process for the prototyping of their ICs. This scenery motivated the CPqD-Telebrás, Brazilian Telecommunication Agency R&D Center, to support a research and development program on optical receivers operating up to 2.5 Gb/s. The demultiplexer circuit presented here was developed at University of São Paulo as a part of this program and received financial and technical support from the CPqD-Telebrás (contract

Telebrás-USP JDPqD 516/93). It represents the first result of Brazilian engineering on the design of Gb/s integrated circuits.

In this paper we present the design considerations and experimental results of a demultiplexer IC with an integrated skip circuit. The demultiplexer works either as a 622 Mb/s 4-bit demux or as a 2.488 Gb/s 16-bit demux, and is intended for use in both SONET STS-12 and STS-48 systems. The circuit was constructed using a 1μm MESFET foundry technology commercially available. The design emphasis was on circuit architecture for high speed operation and low power dissipation.

2. CIRCUIT ARCHITECTURE

The circuit was designed using elements from the QLSI™ standard cell library from TriQuint Semiconductor, Inc. This library is based on 1 μm FET SCFL logic gates and is specified to operate up to 2.0 Gb/s. To overcome this bit rate limitation the following procedures were adopted:

a) a tree type demultiplexer topology was used that minimizes the number of elements operating at clock rate and eases the integration to the skip circuit;

b) a bypass to the first clock divider circuit was provides, so that the IC could be driven by clock/2 instead of the clock signal at high bit rates;

c) a new skip circuit without retiming at clock rate was proposed.

As shown in figure 1, the demultiplexer employs a four level tree type circuit topology[1] using 1:2 demux blocks composed by Tristage flip-flops[2] and D flip-flops. For 1:16 demux operation mode all data outputs D1 to D16 are enabled and the clock/16 signal is present at the output clock port. When the 1:4 demux operation mode is selected, the outputs from the second demultiplexation level are driven to the data outputs D4, D8, D12 and D16 through the selectors S1 to S4. The remaining data outputs are disabled and the clock/4 signal is selected as the output clock through selector S5. A delay was introduced at the input data signal path in order to guarantee it to be sampled at the proper phase by the first 1:2 demux block. This delay was optimized envisaging the circuit operation at 2.5 Gb/s and combines the delay of logical gates and the physical delay due to the layout parasitic capacitance from metal interconnections.

Figure 2 presents the topology of the proposed skip circuit. This circuit was obtained modifying the skip circuit presented at reference [3] and was especially developed for improved performance when the demultiplexer operates at high speed. Retiming steps at clock rate were avoid and all the logic gates on the skip

circuit operate at clock/2 rate, except the clock divider circuit that is driven by the clock signal. This way, the clock divider circuit is the element that limits the high speed operation of the skip circuit. This limitation can become critical when the intrinsic delay time of the standard cells increase due to variation on the circuit fabrication process. To overcome this limitation, a bypass to the clock divider circuit was provided that allows the skip circuit to be driven by clock/2 instead of clock signal at high bit rates, increasing the circuit fabrication yield.

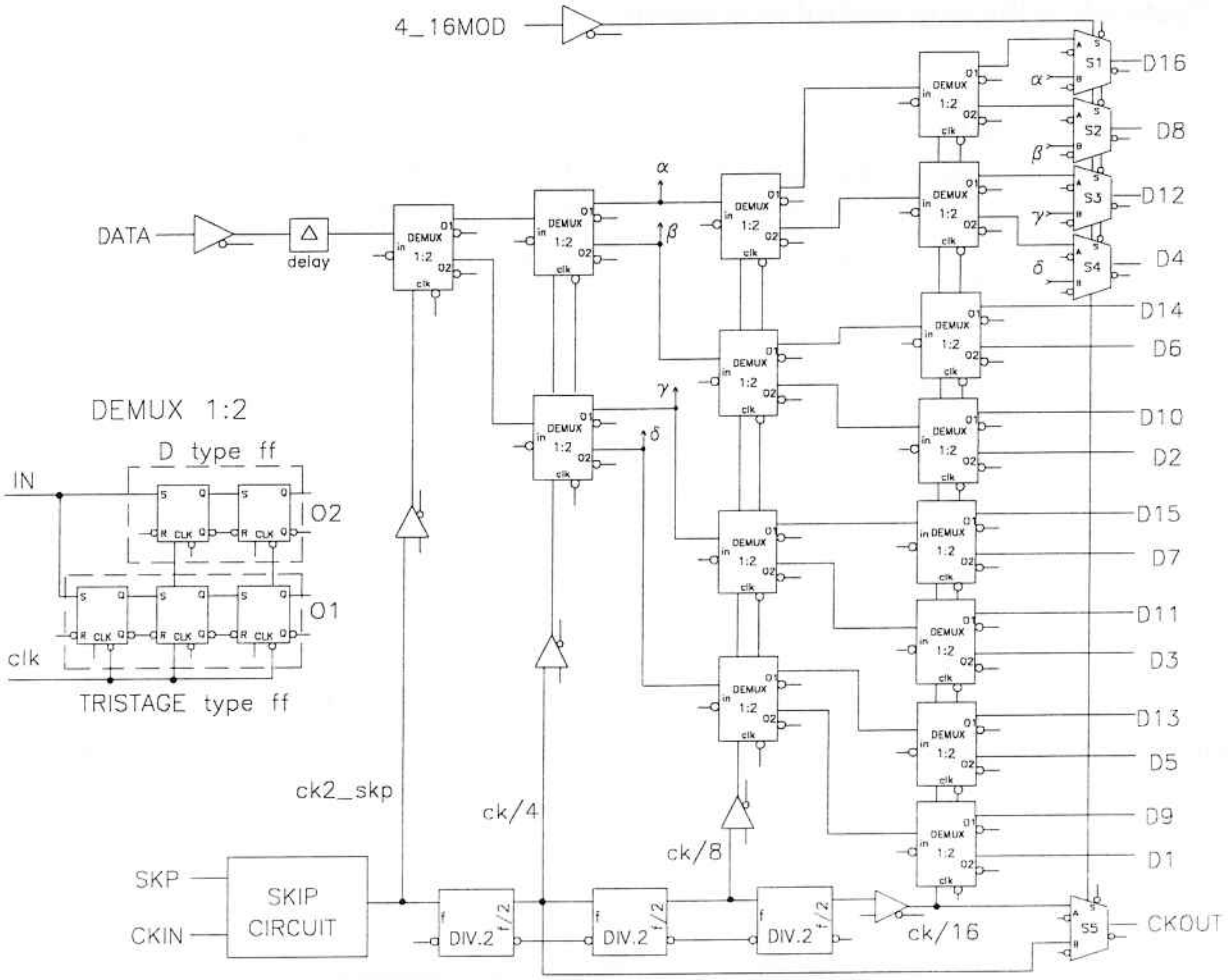

Figure 1. Topology of 1:4/1:16 demultiplexer.

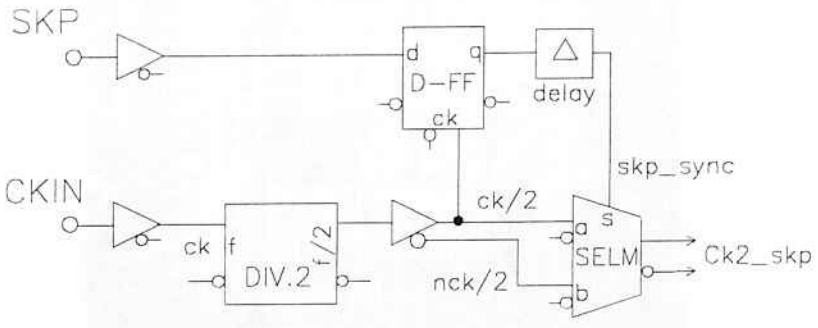

Figure 2. Skip circuit topology .

A detailed time diagram of the proposed skip circuit is shown in figure 3. The skip circuit is sensitive to transitions of the asynchronous control signal (SKP) applied to its input. The skip control signal is synchronized to clock/2 using a D flip-flop and actuates the selector SELM, connecting either clock/2 or its complement to the selector output. The relative phase between clock/2 and the skip control signal at the selector inputs was carefully adjusted during the circuit design. As a result, half cycle of the signal at the selector output (Ck/2_skp) is skipped with minimum spike effects when the skip control is actuated.

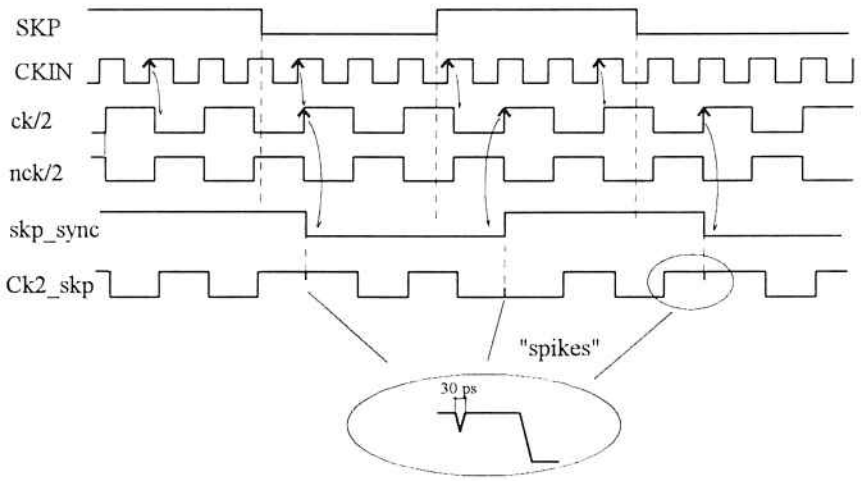

Figure 3. Time diagram of skip circuit.

ECL-compatible I/Os were integrated to all inputs and outputs of the circuit. The circuit was layouted at CPqD-Telebras using manual place and route procedures for minimizing the layout parasitic.The circuit was construtected by TriQuint Semiconductor, Inc. and the chip area is $(2.5\ mm)^2$. Figure 4 presents a microphotograph of the chip.

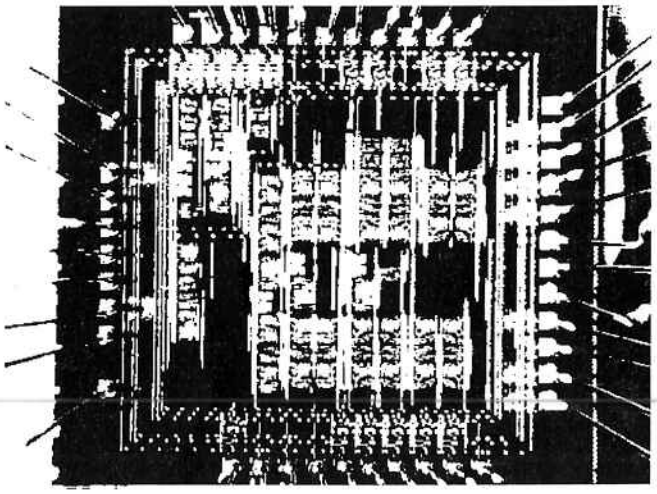

Figure 4. Microphotograph of the demultiplexer IC with skip circuit.

3. SIMULATION RESULTS

The simulation of high-speed digital circuits is usually done at two different steps. In the first step the circuit is simulated before we have information concerning the circuit layout. However, the wiring capacitance that come from the metallic interconnects can not be neglected at high-speed and has to be estimated from an appropriate formula. This preliminary simulation allow the designer to check the functionality of the circuit architecture and to optimize the overall circuit performance. The influence of the variations of fabrication process and environment temperature on the circuit performance can be evaluated on this simulation stage, to prove the possibility of constructing this circuit with an acceptable fabrication yield.

Once the desired results are obtained from the first simulation stage, circuit layout can start. After a preliminary circuit layout is done, a back-annotation is performed to extract the wiring capacitance and the pos-layout simulation can be performed. On this second simulation step allows the designer to check the circuit performance and to do any needed change on the circuit layout to improve the circuit operation at high-speed.

In both preliminary and pos-layout simulations it is necessary to developed test vectors to represent signals applied to the circuit inputs. The test vector should be as complete as possible in order to simulate all the possibilities of input signal combinations. When we are simulating digital circuits with low and medium complexity, as in the case of demultiplexers, it is possible to generate a long test vector that allows an exhaustive simulation of the circuit. Long test vectors are then generated to test the circuit functionality.

A complete simulation of all the functions of the demultiplexer was done using a long test vector to simulate all the combinations of the following items:

- circuit operation as 1:4 demux and a 1:16 demux;
- the actuation of the skip circuit on both 1:4 demux and a 1:16 demux operation modes;
- relative phase between input data and input clock signals deviating up to ± 20% from the nominal value;
- circuit operation when the standard cell parameters range from 0.7 to 1.5 times their nominal values due to temperature and process variation.

In order to create a long test vector for simulation of the demultiplexer, an ideal pseudo-random generator was implemented in the same file as the circuit to be

simulated. The pseudo-random generator topology and its connection to the demultiplexer circuit is shown in figure 5.

The pseudo-random generator employs an n (4 or 16) bit shifter register using D type flip-flops operating at the same input clock rate as the demultiplexer circuit. As shown in figure 5, some or all outputs of the shifter register drive a XNOR gate, and the resulting signal is feedback to the data input of the shift register, generating a pseudo-random sequence on the its outputs 1 to n. The outputs 1 to n of the shifter register are retimed by the signal clock/n through a bench of latch's, generating the vector of signals [d1m, d2m ....d16m]. This same signals are present at the q output of the shifter register but multiplexed on time, consisting the input data driving the demultiplexer under simulation. The proper operation of the demultiplexer can be checked by means of a simple comparison between the demultiplexer output vector [d1, d2, d3....d16)] and the signal vector [d1m, d2m, ...d16m].

The phase shifters $\Delta\Phi$ inserted between the pseudo-random generator and the demultiplexer allows to adjust the relative phase between data and clock inputs of the circuit under simulation.

The simulation file containing the pseudo-random generator and the demultiplexer was used to perform a pos-layout simulation of the demultiplexer and skip circuits considering a relative phase of 180° ± 20% between the input data and clock signals. The standard cell parameters were varied from 70% to 150% their nominal values to simulate the circuit behavior under process and temperature variation. The simulation results demonstrated the required circuit performance over all the simulated range. However, at 2.5 Gb/s an external delay should be added to the input data path when the standard cell parameters deviate more than -8%/+23% from nominal values.

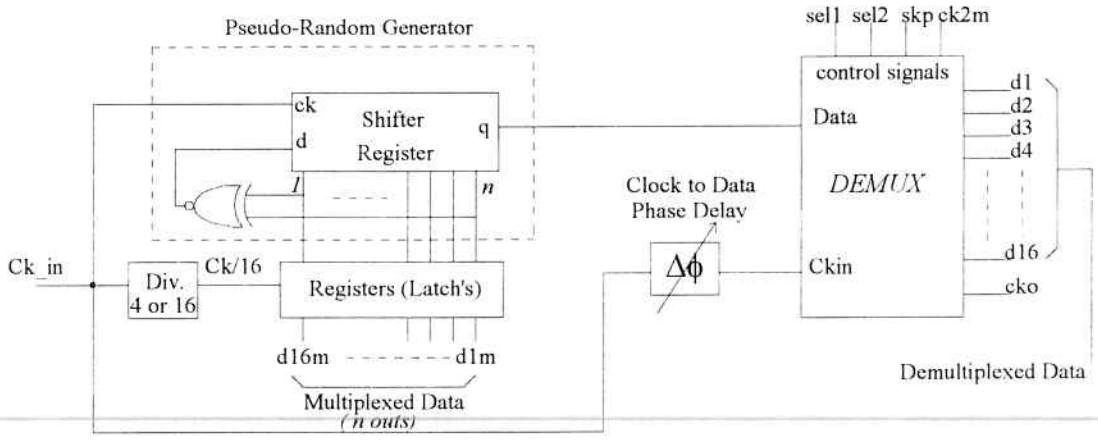

Figure 5. Demulttiplexer simulation arrangement with ideal pseudo-random generator.

4. EXPERIMENTAL RESULTS

The demultiplexer IC was mounted in a multilayer ceramic package and measured in a test fixture with controlled impedance 50 Ohm signal lines. The input signal lines were terminated to -2.0 V through 50 Ohm resistors placed close to the package. The IC was biased with -5.2 V supply voltage, presenting 1.4 W of power dissipation and signal output levels compatible to ECL standards.

The functionality of the demultiplexer was demonstrated by measuring the circuit performance with low speed signals (10 Mb/s clock) and high speed signals (622 Mb/s and 2.488 Gb/s clock) at room temperature. The circuit was driven by input data and clock signals with 180° of relative phase and ECL logic levels. Figure 6 shows typical input clock, output clock and output data wave forms of the IC operating as a 1:4 demultiplexer at 622 Mb/s clock, when a 1/8 signal pattern is applied to the input data port. The measured rise and fall times for the output data signal shown in the figure were 630 ps and 430 ps, respectively. The relative phase between the output clock and the output data signals was 185°.

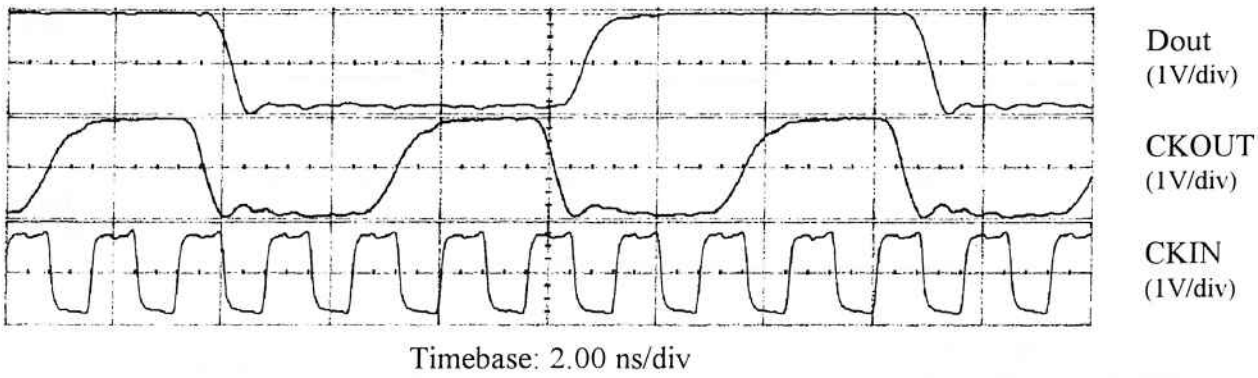

Figure 6. Input clock, output clock and output data wave forms for 1:4 demux at 622 Mb/s clock rate.

The performance of the IC operating as a 1:16 demultiplexer at 2.488 Gb/s clock rate is presented in figures 7 and 8. Figure 7 shows the input and output clock signals wave forms, demonstrating the right operation of the clock divider circuit up to 2.488 Gb/s.

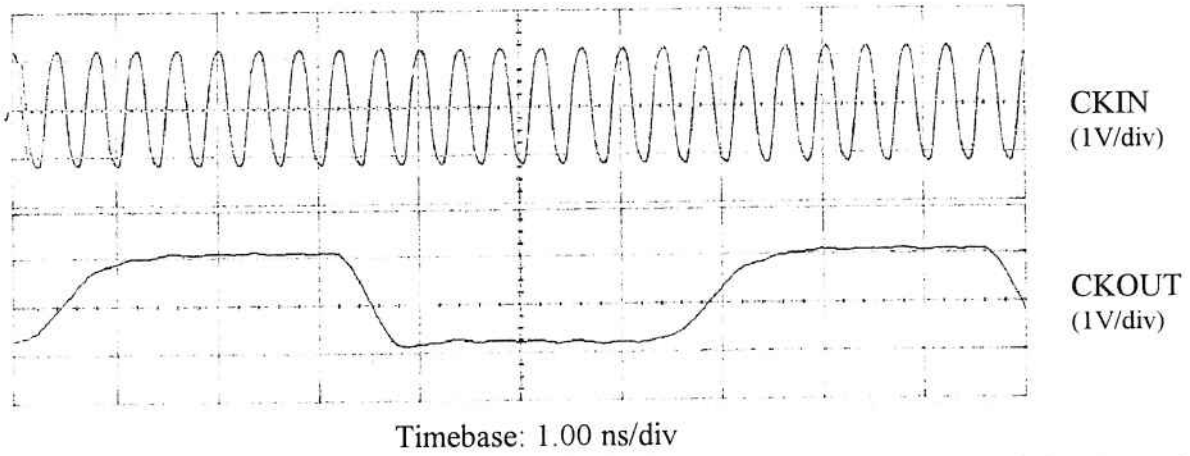

Figure 7. Input and output clock wave forms for the 1:16 demultiplexer at 2.488 Gb/s clock rate.

Figure 8 shows the good alignment between the output data and output clock signals when a pseudo random signal is applied to the demultiplexer data input.

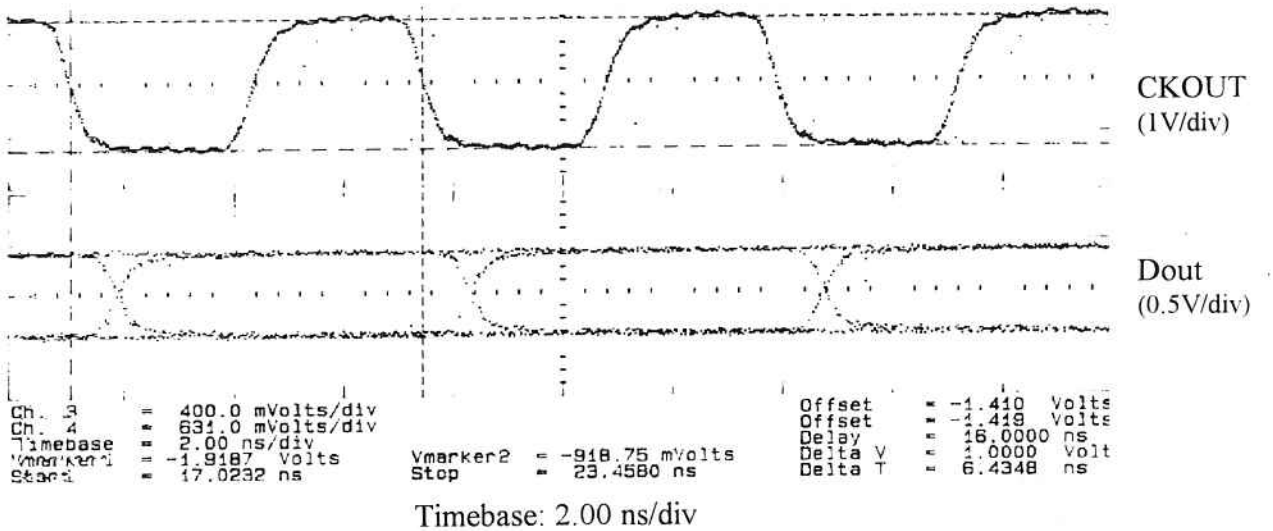

Figure 8. Output clock and output data wave forms for the 1:16 demultiplexer at 2.488 Gb/s clock rate.

The effectiveness of the skip circuit proposed in this paper was experimentally verified for the IC operating at 1:4 and 1:16 demultiplexer modes up to 2.488 Gb/s.

The demultiplexer circuit was also tested bypassing the first clock divider and driven the circuit with clock/2 instead of clock signal, and demonstrated the required performance. This operation mode may be used in the case the variation of the circuit technology made the first clock divider to fail at 2.488 Gb/s.

Table I presents the main characteristics of demultiplexer ICs reported on the literature, employing GaAs MESFETs with gate length ranging from 0.5 to 1 μm.

The experimental results obtained for the demultiplexer IC presented in this paper are in good agreement with published data. The ratio between the operation rate and the power consumption of the demultiplexer could be increased employing a full-custom design approach in order to use both DCFL and SCFL logic gates on the implementation of the circuit. Considering a 1 μm GaAs MESFET technology, the use of SCFL logic gates operating at clock and clock/2 and DCFL logic gates operating at clock/4, clock/8 and clock/16 would result on the decrease of the power consumption without degrading the high-speed performance of the circuit.

Table I - Characteristics of demultiplexer circuits employing GaAs MESFETs

Ref.	Circuit function	Lg (μm)	Logic family	Clock rate (Gb/s)	Power consumption (W)
4	demux 1:8/1:16	na	BFL	2.0	2.0
5	demux 1:16	0.6	SCFL/DCFL	2.5	1.22
this paper	demux 1:4/1:16 & skip circuit	1.0	SCFL	2.5	1.4
6	demux 1:16	0.7	DCFL	3.2	1.3
7	demux 1:4	0.7	SCFL	4.0	3.7
8	demux 1:16	0.5	LSCFL	4.6	1.6
9	demux 1:8	0.5	DCFL	8.0	1.9
10	demux 1:8 & skip circuit	0.5	SCFL	10.4	3.8
11	demux 1:8	0.5	SCFL	20.0	7.5

5. CONCLUSIONS

An experience on the design of high-speed digital GaAs ICs was reported, emphasizing the issues on circuit architecture, layout, fabrication and characterization at Gb/s rates.

A 2.488 Gb/s demultiplexer with low power dissipation was designed to operate either as a 4-bit demux or a 16-bit demux. A skip circuit employing a new topology was integrated to the demultiplexer.

The circuit was constructed using 1 μm MESFET SCFL standard cells from a commercially available foundry service. The demultiplexer operated up to 2.488 Gb/s with 1.4 W of power dissipation. The experimental results demonstrated the effectiveness of the proposed skip circuit.

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REFERENCES

1. R. B. Nubling *et al.* "High-Speed 8:1 Multiplexer and 1:8 Demultiplexer Implemented with AlGaAs/GaAs HBT's," *IEEE Journal of Solid State Circuits*, vol. 26, no. 10, Oct. 91, pp. 1354-1361.
2. M. Ida, N. Kato and T. Takada "A 4-Gbits/s GaAs 16:1 Multiplexer/ 1:16 Demultiplexer LSI Chip," *IEEE Journal of Solid State Circuits*, vol. 24, No. 4, Aug. 89, pp. 928-932.
3. M. Bagheri *et al.* "11.6-GHz 1:4 Regenerating Demultiplexer with Bit-Rotation Control and 6.1-Ghz Auto-Latching Phase-Aligner IC's Using AlGaAs/GaAs HBT Technology," *IEEE Journal of Solid State Circuits*, vol. 27, no. 12, Dec. 92, pp. 1787-1793.
4. B.Cheney, et al, "Design and Test of 2-Gb/s GaAs 16/8-bits Mux/Demux Pair", *IEEE J. of Solid-State Circuits*, vol.24,no.2, Apr. 89, pp. 463 - 466.
5. Product Selection Guide: ASICs, Telecomunications and Data Communicatioons - VITESSE Semiconductor Corporation, Aug. 1995.
6. N. Higashisaka, M.Shimada, A.Ohta, K. Hosogi, Y.Tobita Y. Mitsui, "GaAs DCFL 2.5 Gbps 16-bit Multiplexer/Demultiplexer LSI's", *IEEE J. of Solid-State Circuits*, vol.29, no.7, Jul. 94, pp 808-14.
7. P. S. Lassen, High-Speed GaAs Digital Integrated Circuits for Optical Communication Systems, *PhD thesis*, Electromagnetics Institute, Technical University of Denmark, May 93.
8. M. Ida, N. Kato and T. Takada "A 4-Gbits/s GaAs 16:1 Multiplexer/ 1:16 Demultiplexer LSI Chip," *IEEE Journal of Solid State Circuits*, vol. 24, No. 4, Aug. 89, pp. 928-932.
9. K. Tanaka et al, "8-Gb/s 8:1 Multiplexer and Demultiplexer IC's Using GaAs DCFL Circuits", *IEEE J. of Solid-State Circits*, vol.27, no.10, Oct. 92, pp 1359 - 1363.
10. K. Ishida, et al, "A 10-GHz 8-b Multiplexer / Demultiplexer Chip Set for SONET STS-192 System", *IEEE J. of Solid-State Circuits*, vol.26, no.12, Dec. 91, pp. 1936 - 1943.
11. T. Seshita, et al, "A 20 GHz 8 bit Multiplexer IC Implemented with 0.5um WNx/W-Gate GaAs MESFET's", *IEEE J. of Solid-State Circuits*, vol.29, no.12, Dec. 94, pp 1583-87.

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