Reconfigurable SOI-MOSFET: Past, Present and Future Applications

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***Abstract*— This paper presents a historical analysis of reconfigurable field effect transistors (RFETs). History shows the naturalness of its development from the evolution of integrated circuits (ICs) technology. Next, its operating principles are detailed to further study the variety of structures proposed in the specialized literature. Among these structures, the Back Enhanced SOI MOSFET (^{BE}SOI MOSFET) has been studied in detail, which stands out for its simplicity of fabrication and the possibility of integration with conventional technologies. The ^{BE}SOI MOSFET is used to present proofs of concept for RFET applications such as: reconfigurable digital circuits, light sensor, permittivity-based biosensor and charge-based biosensor. The latter may allow, for example, obtaining a glucose sensor. Finally, future perspectives of applications of RFETs are presented, as in systems of protection of the intellectual property of ICs.**

***Index Terms*— Reconfigurable-FET; Sensor; Biosensor; SOI-MOS; Electrostatic doping.**

I. Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) presented itself as a promising technology, with great potential for growth, in the early 1960s, as G Moore [1] shrewdly observed. The signs perceived by Moore to elaborate his famous article were the optimization of the costs of an integrated circuit with the shrinkage of the MOSFETs and the increment of functions inserted in this integrated circuit.

Some fabrication techniques were developed to maintain the downscaling and its advantageous reduction in the costs per function of the ICs. One of these techniques is the use of SOI (silicon-on-insulator) wafers that allow an intrinsic dielectric isolation between the devices and the substrate, mitigating undesirable effects of reducing the size of the devices [2].

In the early 1990s, the SIMOX technique [3] was the most used in the production of SOI wafers, but it was necessary to measure and keep the concentration of defects at the interfaces under control [4]. Therefore, at the end of the process of obtaining the SOI wafers, it was necessary to measure its main characteristics.

The pseudo-MOS (Ψ-MOS) [5] was presented as a non-destructive technique to electrically characterize these SOI wafers. This technique consists of obtaining characteristic curves of MOS transistors, using only a metallic base to bias the substrate of the SOI wafers, and two probes to polarize different regions of the silicon on the insulator. In other words, this means to use the substrate as the gate terminal and the buried oxide from the SOI wafer as the gate oxide. To obtain source and drain terminals (V_S and V_D), two probes touch the silicon over the insulator. Fig. 1 shows the basic concept of pseudo-MOS.

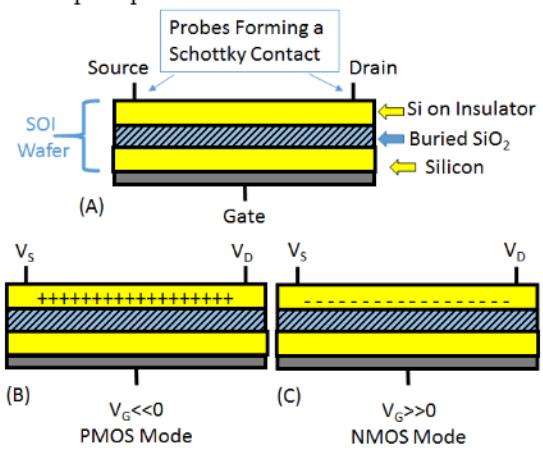

Fig.1 Pseudo-MOS basic structure (A); gate bias to program PMOS mode (B) and gate bias to program NMOS mode (C).

Therefore, the substrate bias (used as a gate, V_G) allows the formation of an inversion/accumulation layer at the silicon/buried oxide interface, and this allows the electric current between source and drain. The electric characteristics of this device make it possible to extract various electrical parameters such as the mobility of both carriers: electrons and holes. This fact permits the pseudo-MOS application in the electrical characterization of SOI wafers.

Later, the Smart-Cut® technique [6] would make the interface between Si and buried SiO_2 as good as the best MOS device interfaces, making characterization techniques like pseudo-MOS less necessary.

As important as the characterization technique are the concepts contained in the pseudo-MOS. The ambipolar electrical transport through Schottky junction [5] and the so-called electrostatic doping [7]. These concepts are very important for today's reconfigurable transistors (RFETs). The original experiment from pseudo-MOS already made it possible to obtain NMOSFET and PMOSFET transistors, selected by bias, to operate at different times and in a single wafer.

Ambipolarity is sometimes treated as an undesired effect, since it increases the leakage current (high off-state currents). In a study on Schottky barrier Thin-Film Transistors (TFT) [8] it was proposed the use of a second gate for the device (Fig. 2). This is used to suppress unwanted carrier current. This second gate is currently called the programming gate and is another important concept for today's reconfigurable transistors.

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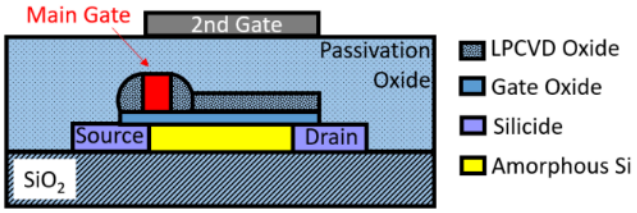

Fig.2 Schottky barrier Thin-Film Transistor (TFT).

These works ([5] and [8]) provide the bases for RFETs independently, from structures that share a thin layer of semiconductor on insulator, a programming gate to select the carriers to be used (electrostatic doping) and contacts Schottky with the semiconductor. In other words, the concept of reconfigurable transistors emerges naturally from the analysis of devices with these basic properties. These properties become more common from the intense study of SOI substrates.

The SOI-CMOS group of the Laboratory of Integrated Systems (LSI) at University of Sao Paulo (USP) has been dedicated to the electrical characterization and simulation of SOI devices since the early 1990s [9]. This research group also developed the fabrication of the first three photolithograph steps Fully Depleted SOI (FD SOI) transistor in Brazil for education application [10] and the first fully electron-beam-lithography SOI FinFET in Latin-America for proof of concept (Fig. 3) [11, 12].

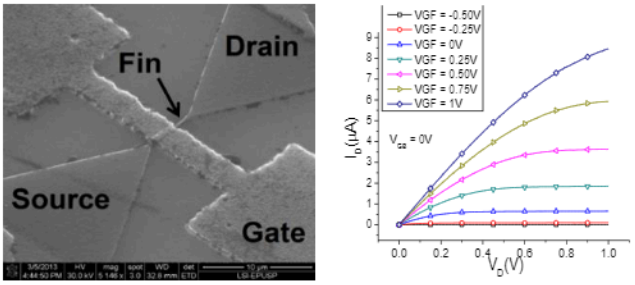

Fig.3 Fully electron-beam-lithography SOI FinFET fabricated at LSI/USP. (A) MEV picture and (B) output electrical characteristics.

Based on this background on SOI devices, it was possible to propose and fabricate the first Brazilian SOI reconfigurable transistor (RFET) [13] called the ^{BE}SOI MOSFET (Back Enhanced Silicon-On-Insulator MOSFET) as shown in Fig. 4 . Since then, this device has been used for many applications like reconfigurable logic circuit [14], sensor [16] and biosensor [17], through numerical simulations and experimental results.

The ^{BE}SOI MOSFET presented a performance improvement using Ultra-Thin Body and Buried Oxide (UTBB) SOI wafer [15].

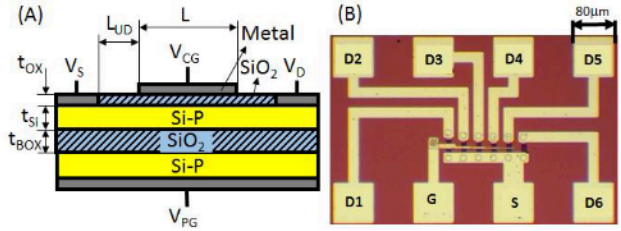

Fig.4 (A) ^{BE}SOI schematic structure and (B) picture of the fabricated transistors (L-array). Gate (G), common source (S) and six individual drains (D1-D6).

Furthermore, the concept of reconfigurable transistors can be applied in silicon devices (such as ^{BE} SOI), or in other semiconductor materials such as transition metal dichalcogenides such as: MoS_2, $MoSe_2$, WSe_2 [18]. This incredible versatility, in applications and in materials, makes RFETs a kind of emerging device of great interest.

This paper presents the working principles of reconfigurable transistors (RFETs), their most used structures, applications using a specific RFET called ^{BE}SOI for digital circuits, sensor and biosensor, and a perspective for future applications.

II. RFET Working Principle

In order to better understand the reconfigurable-FET (RFET), this section firstly describes their working principle using the ^{BE}SOI MOSFET structure. Then, the formation of the source and drain contacts are explained due to their importance for the correct functioning of RFETs.

A. Reconfigurability

The main idea of an RFET device is to define its type (PMOS or NMOS) after the processing through a bias applied to the programming gate (V_{PG}). Fig. 5 illustrates the working principle of a ^{BE}SOI [19].

For enough negative V_{PG}, holes are induced at the back interface, allowing the hole conduction between source and drain, that is, the ON state-region (Fig.5C) when it is working as a PMOS. The bias applied to the control gate (V_{CG}) modulates the channel, controlling or even blocking the hole current, and for V_{CG} higher than the threshold voltage V_T (PMOS) the device is in the OFF-state region (Fig.5A). On the other hand, an enough positive V_{PG}, electrons are induced at the back interface, allowing the electron conduction between source and drain, leading to the ON-state region (Fig.5D) when it is working as a NMOS. The V_{CG} can increase or even block the electrons current, and for V_{CG} lower than V_T, (NMOS) the device is in the OFF-state region (Fig.5B) [19].

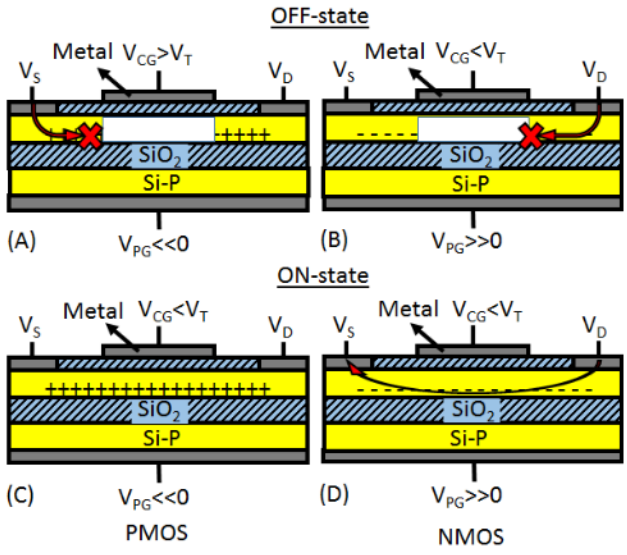

Fig.5 ^{BE}SOI working principle. A) PMOS OFF-state region; B) NMOS OFF-state region; C) PMOS ON-state region; D) NMOS ON-state region.

B. Source and Drain Contacts

In an RFET device, the source and drain contacts need to allow conduction of both carriers (electrons and holes), which is connected with the source and drain contact type (ohmic or Schottky). Figs. 6 and 7 explain the formation of an ohmic and a Schottky contacts, respectively, through a charge model (Figs. 6A, 6B, 7A and 7B) and their respective band diagram (Figs. 6C, 6D, 7C and 7D) for a metal/P-type (Figs. 6A, 6C, 7A and 7C) or metal/N-type semiconductor (Figs. 6B, 6D, 7B and 7D) [20].

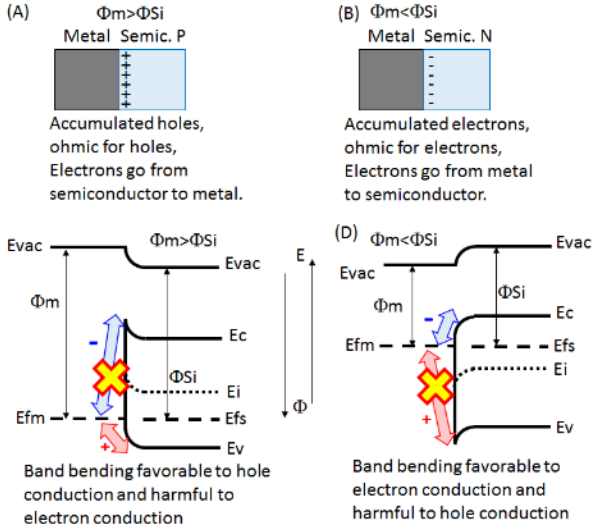

Fig.6 Formation of an ohmic contact. (A) Charge model for a Metal/P-type semiconductor contact, (B) Charge model for a Metal/N-type semiconductor contact, (C) Band diagram for a Metal/P-type semiconductor contact, (D) Band diagram for a Metal/N-type semiconductor contact.

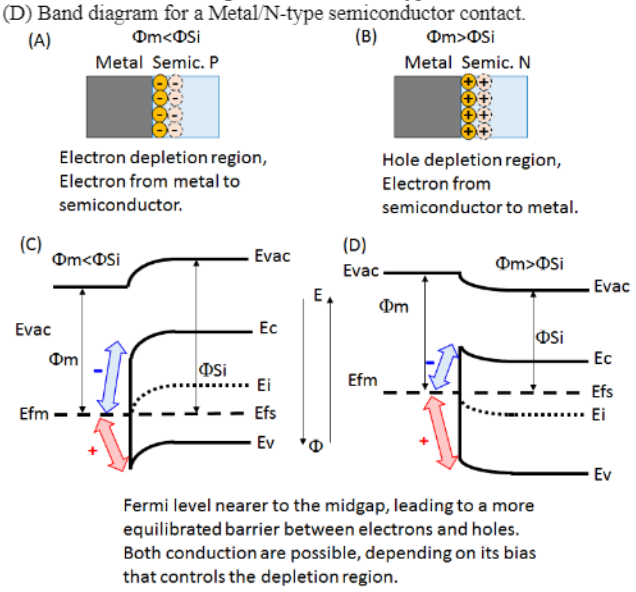

Fig.7 Formation of a Schottky contact. (A) Charge model for a Metal/P-type semiconductor contact, (B) Charge model for a Metal/N-type semiconductor contact, (C) Band diagram for a Metal/P-type semiconductor contact, (B) Band diagram for a Metal/N-type semiconductor contact.

The electrical contact between a metal and a semiconductor is ohmic type when an accumulation layer forms at the semiconductor interface. Therefore, in a metal/P-type semiconductor contact with the metal workfunction higher than the semiconductor one ($\Phi_M > \Phi_{Si}$, Fig.6A), an accumulated layer of holes forms at the interface. After reaching the equilibrium, with this hole accumulated layer, any arriving hole can easily pass through this junction. However, any arriving electron is easily recombined, preventing the electron conduction. Therefore, an ohmic junction for holes is formed.

Analogously, in a metal/N-type semiconductor contact with $\Phi_M < \Phi_{Si}$ (Fig.6B), an *accumulated* layer of *electron* forms at the interface. This electron accumulated layer facilitates the electron conduction and prevents the hole conduction. As a conclusion, an ohmic junction for electrons is formed. In the band diagram (Fig.6C for hole conduction and Fig.6D for electron one), this phenomenon is observed by the difference of energy between the Fermi level in the metal (Efm) and the valence band (Ev) for holes (red arrow) and the difference between the Fermi Level in the metal and the conduction band (Ec) for electrons (blue arrow).

On the other hand, in a metal/P-type semiconductor contact with $\Phi_M < \Phi_{Si}$ (Fig.7A), a depletion region (fixed negative charges) forms at the interface. Similarly, in a metal/N-type semiconductor contact with $\Phi_M > \Phi_{Si}$ (Fig.7B), a depletion region (fixed positive charges) forms at the interface. In both situations, the Fermi level is nearer to the midgap and, consequently, the barriers seen by electrons and holes are more symmetric (Figs. 7C and 7D). Therefore, in both cases, the conduction is possible depending on the applied bias.

In ^{BE}SOI devices, the device type (NMOS or PMOS) is defined by the V_{PG}. Among the four ^{BE}SOI generations already fabricated, two materials were used as a source/drain electrode: Aluminum [13, 15, 19, 21] and Nickel Silicide [14, 19]. Nickel Silicide is a midgap material, therefore, a more symmetric current level was achieved between the NMOS and PMOS ^{BE}SOI. Aluminum may present both behaviors, that is, it can show high drain current (I_{DS}) for holes and very low for electrons, or the opposite, depending on the annealing process after Aluminum deposition. When annealed, a thin P-type layer is formed at the interface, leading to an ohmic contact behavior, which favors the PMOS ^{BE}SOI (Figs.8A and 9) [20]. However, the Aluminum workfunction forms a Schottky contact with the silicon channel, which favors the NMOS ^{BE}SOI (Fig.8B and 9). [19, 21]

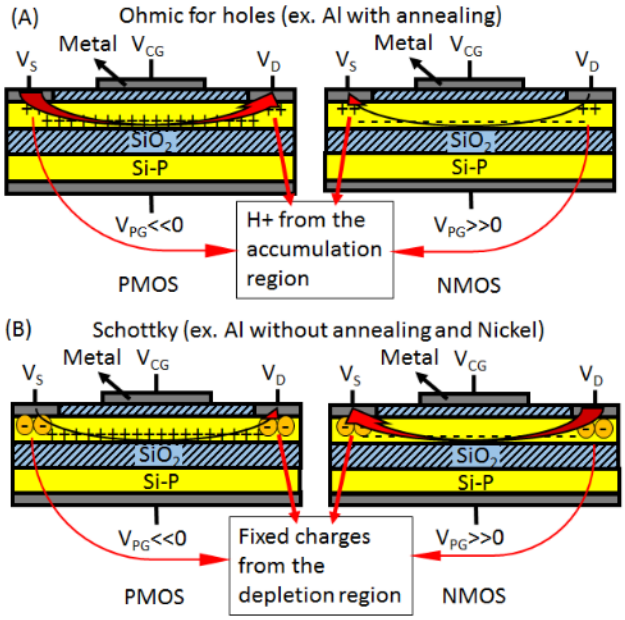

Fig.8 Ohmic (A) and Schottky (B) source and drain contacts behavior in PMOS (left) and NMOS (right) ^{BE}SOI MOSFET.

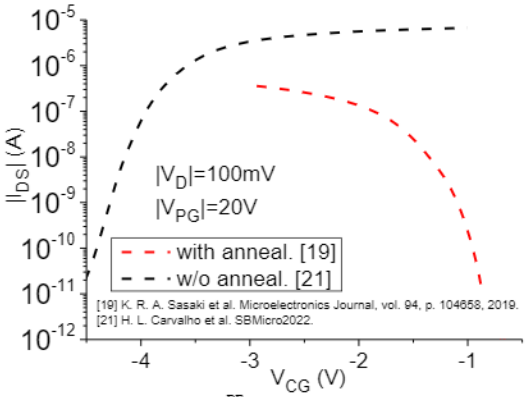

Fig.9 Transfer Characteristic of ^{BE}SOI devices. PMOS drain current with annealed Al S/D contacts and NMOS drain current with no-annealed Al S/D contacts.]

III. Different Types of RFET Structures

In order to achieve the previous operation, there are different RFETs structures in the literature as illustrated in Fig.10 [22, 23]. In Figs. 10A and 10B, the programming gate simultaneously controls the Schottky barriers in both junctions, source-channel and drain-channel, defining the transistor type (NMOS or PMOS). While the control gate modulates the channel, allowing the on/off states (Fig. 10D).

On the other hand, in Fig. 10C, the source-channel and drain-channel independently determine the transistor state and type. The programming gate determine the transistor type through the drain-channel junction, while the control gate allows the conduction or cease the drain current through the source-channel junction (Fig. 10E).

This principle has been explored on RFETs in planar, nanowire devices and other materials [24-27]

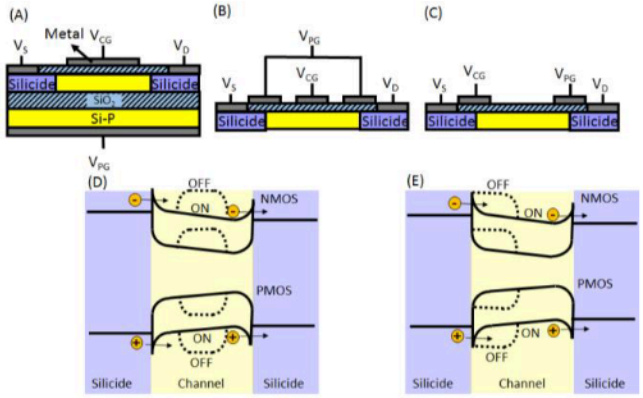

Fig.10 Two types of reconfigurable FETs and their band diagram: (A) and (B) with simultaneous control of the transistor's type at source and drain Schottky junctions and (C) with independent control. (D) is the band diagram of the (A) and (B) configurations and (E) is the band diagram of the (C) configuration.

A third RFET structure is a planar structure like Fig. 10A, with two source and two drain contacts: two source/drain contacts for hole conduction (Fig. 11A) and the two others for electron current (Fig. 11B) [28]. They take advantage of the higher drive current of both contacts (hole current in ohmic contact and electron current in Schottky contact), without reducing the other carrier conduction due to the higher Schottky barrier. This structure is one of the approaches for achieving equilibrated drain current level for N-type and P-type RFETs. Others already reported methods are the use of a midgap source-drain contact [14, 19, 29] or a strain technique [30].

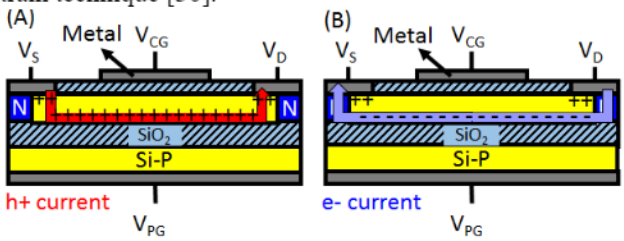

Fig.11 Planar RFET with two source/drain ohmic contacts (A) and two source/drain Schottky contacts (B).

IV. RFET Applications

RFETs have been reported for different applications such as different sensors and circuits. Ref. [16] explores the ^{BE}SOI RFET application as a light sensor (visible or UV spectra) (sub-section A). Ref. [31] studies the ^{BE}SOI RFET as a permittivity and charge-based biosensor (sub-section B) and refs. [32-35] discuss the RFET performance in a logic circuits (sub-section C) as shown below.

A. Light sensor

Due to the buried oxide and thin silicon channel, the SOI technology is more immune to radiation than the MOSFETs, which means that a ^{BE}SOI light sensor would present a lower sensitivity. The underlap region of ^{BE}SOI MOSFET (region between gate electrode and source/drain contacts) can be used as a light sensor. Electron-hole pairs are generated by the light, increasing the drain current (Figs. 12A and 13A) proportional to the underlap area. On the other hand, for small underlap area (smaller channel length, L, and width, W), if the transistor is biased in the subthreshold region, the sensitivity can also be detected (Fig.12B). In this case, the light-generated electrons go to the front interface, which reduces the threshold voltage of the back interface through the front-back interfaces coupling (Fig. 13B) [16].

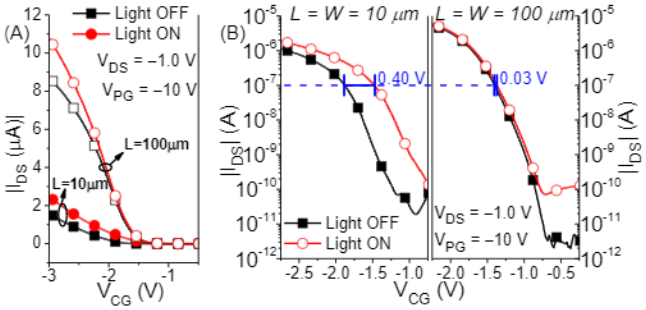

Fig.12 Light detection through the drain current raise (A) and threshold voltage shift (B) methods for L=W=10µm and L=W=100µm.

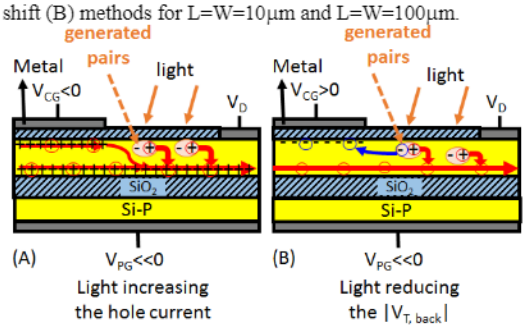

Fig.13 Different mechanisms to improve the current conduction on a ^{BE}SOI MOSFET light sensor: by increase the number of charges and by reducing the threshold voltage of the back interface.

B. Biosensors

RFETs have also been extensively studied for biosensing applications, present in a large range of areas such as health, agriculture and food industries [36, 37]. Biosensors are devices capable to detect and convert variations of a specific biological stimulus to an electrical signal. The field effect transistor (FET) based biosensors have gained much attention thanks to their reduced size, integration with the processing circuit, reduced mass production cost, fast response time and reduced sample volume [38, 39]. Two types of FET-based sensors are explored: the permittivity-based and the charge-based biosensors. [31]

i. Permittivity-based sensor: as a field effect sensor, the electric permittivity of the biomaterial affects its drain current thanks to the electric field from gate electrode that reaches the gate oxide-silicon interface. The material of interest would be put on the gate insulator or in part of them, changing the effective dielectric constant (Fig.14A) [40]. Table I shows some examples of substances and their dielectric constant ($k = \varepsilon/\varepsilon_o$).

Table I. Examples of substances and their dielectric constant.

Substance	k
Uricase	1.54 [41]
Biotina	2.63 [41]
APTES	2.57 [42]
Protein	5.8 [43, 44]

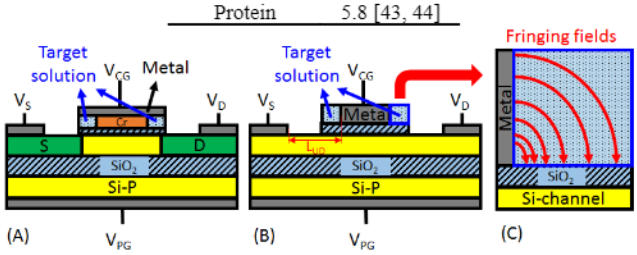

Fig.14 Structures of the permittivity-based sensors: sensing by altering the effective dielectric constant (A) and the fringing fields (B and C).

In a second permittivity-based sensor (Fig.14B), the biomaterial is placed on the underlap regions, acting on the channel by the fringing electric field of the front gate electrode (Fig.14C) [31]. The ^{BE}SOI's sizes were optimized to improve their sensitivities (Table II). The highest sensitivities were observed for thicker buried oxide thickness t_{BOX} (250nm) and front gate oxide t_{OX} (20nm), thinner channel thickness t_{Si} (5nm) and underlap length L_{UD} around 50nm for n-type ^{BE}SOI (a better discussion can be seen in sub-section B-ii). No significant influence was observed for the channel length. An increase up to one order of magnitude was achieved in this optimization.

Table II. Permittivity-based biosensor optimization. Reference devices have t_{OX}=10nm, t_{Si}=10nm, t_{BOX}=200nm, L=1μm, W=1μm, L_{UD}=100nm. Optimized devices have t_{OX}=20nm, t_{Si}=5nm, t_{BOX}=250nm, L=100nm, W=1μm, L_{UD}=50nm [31].

k	Biosensor sensitivity			
	N-type		P-type	
	Ref.	Opt.	Ref.	Opt.
5	0.3	2.0	0.3	1.9
10	0.6	6.1	0.7	5.3
15	1.0	11.8	1.1	9.4
20	1.4	**18.4**	1.6	13.8

ii. Charge-based sensor: This type of sensor detects variation of the biomaterial charges. Different amount of biomaterial charges induces different amount of carriers participating in the current. In an ISFET (Ion-Sensitive-FET, Fig.15A) [45], for example, the metal gate is replaced by a material that is sensitive solely to the ion of interest (e.g. H^+ in a pH-meter) and the target solution. This ion H^+ changes the effective potential at the front interface, altering the current conduction.

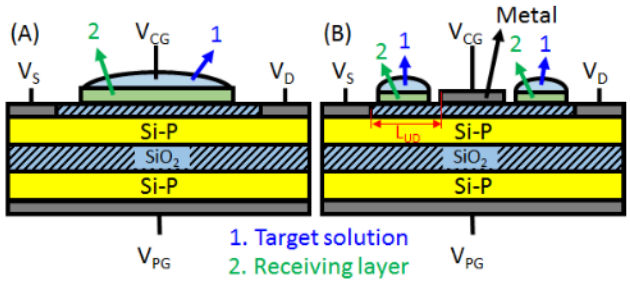

Fig.15 Structures of the charge-based sensors: with the sensing solution on the gate oxide as in an ISFET (A) and on the underlap regions (B).

In a structure like the one used for the permittivity-based sensor, i.e., the biomaterial is placed on the underlap regions (Fig. 15B), the ^{BE}SOI's sizes were also optimized for the highest sensitivities (Table III) [31]. The highest sensitivities were achieved for thicker t_{BOX} (250nm), longer L_{UD} (1μm) and opposite trends for t_{OX} and t_{Si} when comparing N- and P-type ^{BE}SOI (N-type: t_{OX}=5nm and t_{Si}=20nm; P-type: t_{OX}=20nm and t_{Si}=5nm). Again, no significant change was observed for the channel length analysis. An increase up to two order of magnitude higher sensitivity was achieved in this optimization.

Table III. Charge-based biosensor optimization. Reference devices have t_{OX}=10nm, t_{Si}=10nm, t_{BOX}=200nm, L=1μm, W=1μm, L_{UD}=1μm. Optimized devices have W=1μm , L_{UD}=1μm and t_{BOX}=250nm for both N- and P-type devices. The other dimensions are: L=100nm, t_{OX}=5nm, t_{Si}=20nm for n-type and L=1μm, t_{OX}=20nm, t_{Si}=5nm for PMOS transistor [31].

Q_{bio} ($\times 10^{10}$ cm^{-2})	Biosensor sensitivity			
	N-type		P-type	
	Ref.	Opt.	Ref.	Opt.
5	<0.1 `(0.02)	<0.1 (0.04)	0.2	1.6
10	<0.1 (0.05)	0.1	0.5	5.2
50	0.3	0.7	4.1	236.5
100	0.8	1.8	12.7	**1812.3**

Relating these two sensor's types (permittivity and charge-based), shorter underlaps are better for permittivity-based, while longer ones are better for charge-based (Fig.16) [31]. Considering that the receiving layer or the target solution has to enter in the cavity to be sensed, there is a minimum limit for the sensing area. Thus, a permittivity-based sensor becomes impracticable for large molecules without additional equipment to pull the solution in those cavities, which is not the case for in-situ applications. Therefore, a charge-based sensor is more promising.

When analyzing the type of the RFET, Fig.17 schematically shows the sensitivities for N-type and P-type ^{BE}SOI [31]. N-type ^{BE}SOI presented higher sensitivities for positive charges while p-type ones demonstrated better performance for negative charges.

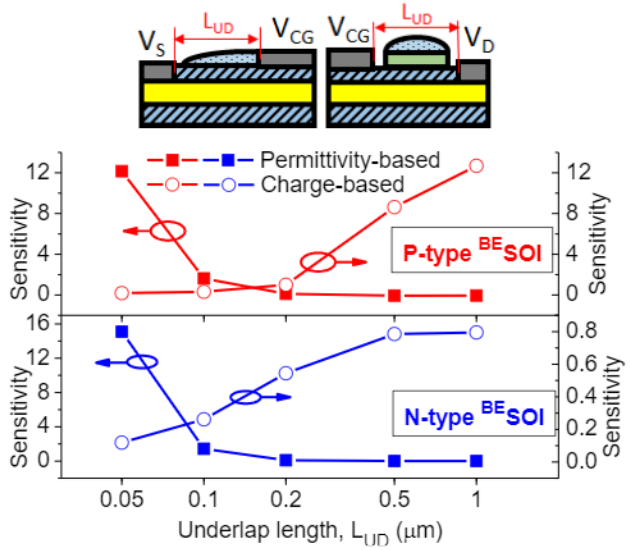

Fig.16 Sensitivities for permittivity-based and charge-based sensors as a function of the underlap length in P-type and N-type ^{BE}SOI.

It bring us an additional freedom degree of the RFETs applied as a biosensor: the same transistor can work to sense positive and negative charges by changing the V_{PG} and the receiving layer after being built.

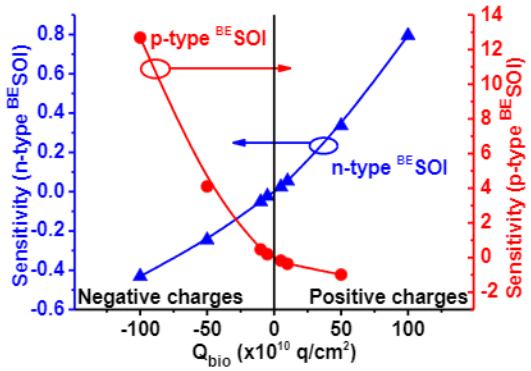

Fig.17 Schematic plot of the sensitivities for positive and negative biological charges in N-type and P-type ^{BE}SOI.

Some examples of RFETs applied as specific biosensors are the glucose and/or the hydrogen peroxide (H_2O_2). Equations (1) and (2) describe the catalysis reaction of the glucose with the formation of the hydrogen peroxide as a sub-product [46]:

$$\beta\text{-D-glucose} + O_2 \xrightarrow{Glucose-oxidase} H_2O_2 + \text{gluconic acid} \quad (1)$$

$$H_2O_2 \rightarrow O_2 + 2H^+ + 2e^- \quad (2)$$

In [47], the structure and preliminary measurements were developed focusing on future fabrications of the ^{BE}SOI biosensors of glucose and/or hydrogen peroxide, showing a reduction on the threshold voltage with the H_2O_2 concentration M_{H2O2} (Table IV).

Table IV. Threshold voltage variation with the H_2O_2 concentration [47].

M_{H2O2} (mM)	V_T (V)
30	1.15
50	1.12
70	1.10
100	1.09

C. Circuits

RFET devices have also been reported for applications in circuits. RFETs presents the advantage of providing different circuits in a same wafer area. In [14, 33] different RFETs were built and analyzed as logic inverters to demonstrate their proof of concept (Fig. 18). Both circuits are logic inverters but with switched transistor type.

After, to demonstrate the change in circuits, [32, 34] analyzed a NAND circuit that change to a NOR circuit using RFETs (Fig. 19). In this case, the concept of an explicit reconfigurability was used, i.e., the reconfigurability is achieved by only altering the transistor from N-type to P-type or vice-versa.

On the other hand, an implicit reconfigurability is used in [48] to implement a XOR gate also using RFETs (Fig.20A). Here, a combination of inputs results electrically to different truth tables. In this reference, the V_{PG} was also used as an input (B) applied to the bottom RFET (and B' applied to the top RFET), shifting the transistors from P-type bottom RFET / N-type top RFET to N-type bottom RFET / P-type top RFET and vice-versa. These two transistors configurations lead to a buffer or a logic inverter circuits that, together, result to a XOR truth table (Fig.20A). Also, one can notice that if the input B was applied to the top RFET (and B' to the bottom RFET), the same circuit can present a XNOR truth table (Fig.20B). [32] also analyzed RFETs as XOR/XNOR, MUX, MAJ-NOT and full adder circuits. [49] explores the XNOR gate for neural network applications and [35] applied RFETs as a non-volatile-memory.

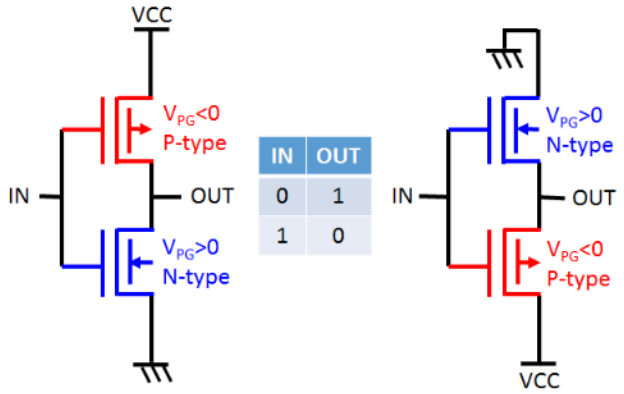

Fig.18 RFET logic inverters and their truth table.

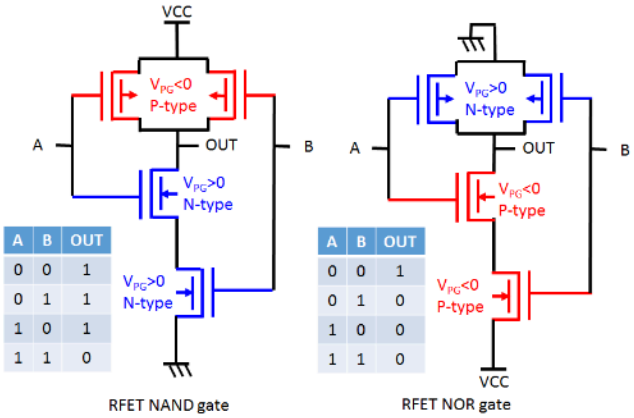

Fig.19 RFET NAND/NOR gate and their truth table.

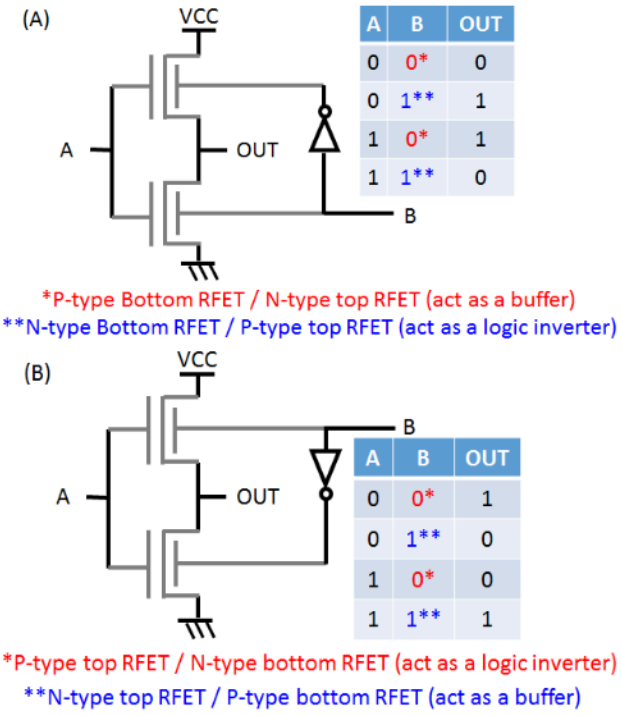

Fig.20 RFET XOR (A) and XNOR (B) gates and their truth table.

V. RFET FUTURE PERSPECTIVES

The reconfigurable transistors (RFET) show promise in some applications already studied and discussed in this paper. However, there are possibilities not yet fully explored.

A. *Hard Security*

These are systems designed to provide integrated circuits (IC) more security against theft of intellectual property, for example. Actually, it is a recurrent precaution in the industry, the insertion of methods that make it difficult for specialists in reverse engineering. They use some methods like visual inspection of ICs, side channel attacks, and controlled fault injection to obtain secrets of design and development.

The inspection consists of exposing the IC (removing the packaging) and obtaining a set of images of all the layers that form it (via Scanning/Transmission electron microscope). After obtaining the image of a layer, the next layer is searched through an Electromechanical Polishing (CMP), for example [50]. And in this way, it is possible to discover a lot about the functioning of an IC, such as, for example, which components form it and how they are connected to each other.

The use of RFETs for IC assembly can make the task of analyzing the operation from the inspection much more difficult, since their electrical behavior depends on polarization. Not that RFETs make reverse engineering impossible, but they make it difficult. Inspection alone would not be enough. It would be necessary to combine other techniques.

Side Channel Attacks are the analysis of a device's behaviors. For example, the power consumption and the execution time of a task. The current level of RFETs is bias dependent through the programming gate. This means that some delays in the execution time of the tasks can be projected, making this type of attack more difficult.

Fault injection consists of causing faults in the system's operation. When they are analyzed together, internal details are revealed. Changes can be made to the power supply of the ICs, in the clock frequency, or even change the operating temperature [51].

Since the RFETs present different behaviors from the traditional CMOS for these injected faults, the combination of both to form hybrid ICs would bring an additional level of variables to be analyzed, making attacks on intellectual property more difficult or at least more expensive. At this point it is necessary to remember that no system is 100% safe. Identifying an intellectual property of ICs is just a matter of time and money [52]. The purpose of countermeasures should be to make reverse engineering so expensive that it does not result in economic benefit.

^{BE}SOI is a simple RFET, which can be inserted into many traditional CMOS ICs without significant cost increase, yet it can make reverse engineering significantly more expensive. That is why RFETs is a promising device for Hard Security applications.

B. *Doping-free double contact ^{BE}SOI*

The future possibilities of RFETs are not restricted to new applications. The evolution of the device itself is an alternative for new applications or even to become more competitive in applications dominated by conventional technologies.

In RFETs, the need for a Schottky contact at the source/drain junctions causes a reduction in the current level, compared to a conventional FD SOI, for example [25]. For this reason, double-contact devices, as in Fig.11, look promising. However, the need for doping makes control difficult due to problems such as random doping fluctuations. This is not a difficulty unique to RFETs but also to other ultrathin layer devices.

In the case of ^{BE}SOI, an alternative is the use of two different types of contact metal, allowing ohmic contact for each carrier independently. As the contact characteristic is determined by the choice of contact metal type, doping problems are avoided and ultrathin layer devices become viable. With ohmic contacts the current levels are higher, and closer to conventional technologies.

VI. CONCLUSION

In summary, reconfigurable field effect transistor (RFET) is a very versatile device, and besides the main application on reconfigurable logic circuits, it can be also used for integrated sensor and biosensor applications.

Among the different RFET structures, a planar ^{BE}SOI MOSFET was specially described, which stands out for its simplicity of fabrication and the possibility of integration with conventional technologies. The applications of ^{BE}SOI MOSFET on reconfigurable digital circuits, light sensor, permittivity-based and charge-based biosensor were demonstrated and explained in this paper.

There are many applications already demonstrated and many others unexplored for this class of devices like hard security and, therefore, they can be considered as a device of great emerging interest.

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