A Fast Readout Electronic System for Accurate Spatial Detection in Ion Beam Tracking for the Next Generation of Particle Accelerators

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***Abstract*— This paper presents the design, implementation, and measurements of a complete electronic frontend intended for high-resolution spatial detection of ion beams at counting rates higher than 10^6 particles per second (p/s). The readout system is made up of three main multichannel building blocks, namely, a transimpedance preamplifier, a signal-conditioning line receiver, and a charge-to-digital converter, as well as some off-the-shelf components. The preamplifier and the line receiver have been specifically designed and optimized to minimize the overlapping probability of ion beams tracking, at high counting rates, in low-pressure gaseous secondary electron detectors. Experimental results are shown, considering α particles sources and particles beams, featuring an adaptive shaping time frame of 170–230 ns with a peak signal-to-noise ratio of up to 25 dB. These performance metrics are competitive with the state of the art, demonstrating the suitability of the reported data acquisition and instrumentation system for precise and fast particle tracking detection.**

***Index Terms*— Detectors, particle tracking, radioactive ions beams (RIBs), readout electronics, spatial detection.**

I. Introduction

RECENT research studies in new isotopes like superheavy and exotic nuclei (those with either an excess of neutrons or protons) have prompted the interest of the scientific community for the development of new instrumentation and measurement techniques to obtain a deeper understanding and knowledge of the nuclear structure and the reaction mechanisms behind these weakly bound radioactive elements with short half-lives, which can be produced at laboratory. To this purpose, the new generation of particle accelerators are able to produce low-energy radioactive ion beams (RIBs), with less than 10 MeV/u [1], at counting rates higher than 10^6 p/s. Due to the large angular aperture and low energy of these beams, their tracks must be detected before the target impact point, to accurately determine the incident energy of the particles, which give rise to the nuclear reactions and to reconstruct the kinematics of such nuclear reactions fragments. To collect these data, a precise and fast electronic readout system is required for both spatial and time detections of the particles involved in the reactions, thus taking advantage of the huge amount of statistical information generated [2], [3].

Although a number of electronic readout systems have been developed in the past for nuclear detectors [4]–[17], very little has been done for the spatial detection in tracking of particles produced by low-energy RIB with 10^6 counting rates. Indeed, the most common approach to implement the front-end electronic detection system is based on the conceptual architecture shown in Fig. 1(a). In this scheme, a charge-sensitive preamplifier is used to amplify the input charge coming from the detector, and the preamplifier output is shaped and then digitized using a peak-sensing analog-to-digital converter (ADC) [18].

The scheme in Fig. 1(a) has been mostly used for energy measurements [18], in which the relevant information—the amount of energy—is directly related to the value of the signal

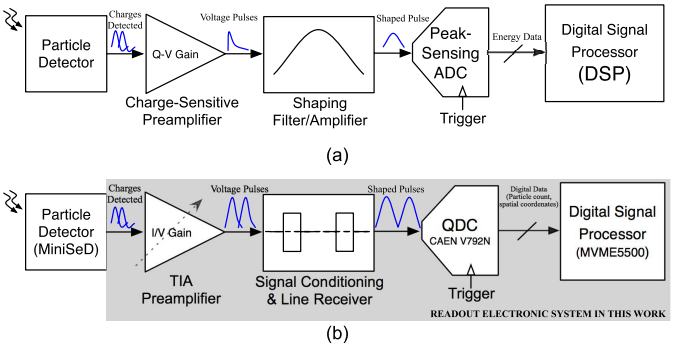

Fig. 1. Conceptual block diagram of an electronic readout system for particle detectors. (a) Based on a charge-sensitive preamplifier and a peak-sensing ADC. (b) Based on a preamplifier and a QDC (approach followed in this paper).

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peak amplitude, instead of the duration of an event. Indeed, this piece of information—not only related with the value of the charge detected but with the time interval in which is detected—is destroyed by the charge sensitive amplifier, thus making the detection of two consecutive particles more difficult as either the counting rate or the input charge from the detector are increased [4].

An alternative implementation of the readout system is conceptually shown in Fig. 1(b), where a fast transimpedance preamplifier (TIA) is used at the front–end interface connected to the detector, and its output signal, after some signal conditioning, is digitized by a charge-to-digital converter (QDC) [18]. One of the most challenging circuits in the readout system of Fig. 1(b) is the preamplifier, due to its early position in the chain. This has motivated the development of different alternative implementations of this building block [4], [8], [10], [19]–[21]. To the best of the authors' knowledge, reported solutions were only focused on the partial implementation of some blocks in Fig. 1(b). However, these solutions are not suitable to discriminate between the two consecutive events when the occurrence rates are higher than 10^6 p/s, and correspond to particles produced by low-energy (<10 MeV/u) ion beams.

This paper contributes to this topic and proposes a complete readout electronic system capable of detecting particles at counting rates over 10^6 p/s with a peak signal-to-noise ratio (SNR) larger than 25 dB. The system is intended to cope with the specifications of spatial measurement in low-pressure gaseous mini-secondary electron detectors (Mini-SeDs) [2], [3], [22], although the presented techniques, design methodologies, and circuit strategies can be applied to other detectors with similar physical conditions and electrical specifications. The presented system is based on the scheme of Fig. 1(b), and combines off-the-shelf electronic components—like the QDC—with other building blocks (preamplifier and line receiver), which have been specifically synthesized and designed to cope with target specifications. A systematic top-down/bottom-up design/verification methodology has been followed to optimize the performance of the overall system for target specifications. A number of measurements—considering different experiment conditions and production sources—are shown to validate the presented approach.

This paper is structured as follows. Section II describes the architecture of the proposed readout electronic system, giving an overview description of Mini-SeDs, and the electrical system-level specifications. Section III presents the design and implementation of main building blocks, namely, the preamplifier and the line receiver. Finally, the experimental results are given in Section IV and the conclusion is drawn in Section V.

II. Readout Architecture and System-Level Specifications

As stated in Section I, the proposed readout electronic system is based on the conceptual scheme shown in Fig. 1(b), intended to detect particles at a rate over 10^6 p/s in a Mini-SeD. The physical characteristics of this detector will determine the electrical specifications and the specific topology required for the different building blocks embedded in the readout electronics.

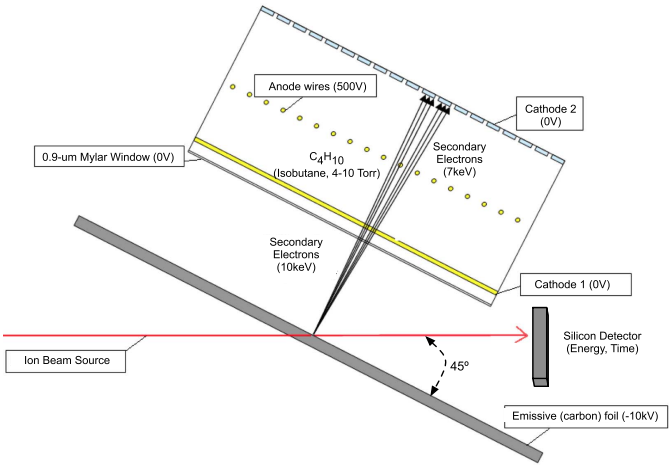

Fig. 2. Illustrating the operating principle of the Mini-SeD.

A. Background on Mini-SeDs

Mini-SeD is a kind of gas ionization multiwire chamber that works at low pressure and has demonstrated to be very suitable for the detection of low-energy ion beams with large angular and energy straggling, thus allowing an accurate reconstruction of the trajectory (tracking)—position and time-of-flight (ToF)—of individual particles at high production rates before the nuclear reaction.

The structure and working principle of an SeD are detailed in [2] and [22] and conceptually shown in Fig. 2. Essentially, the complete detection device is made up of three main parts, namely, an emissive foil, an electrostatic guiding and focalizing system, and a detector prototype Mini-SeD [3]. The latter is composed of an anode placed between the two grounded cathodes. The anode consists of a wire plane, where each wire has a diameter of 20 μm. One of the cathodes is a wire plane (72 wires linked in a 3-by-3 array) of 50-μm diameter, and the other is made of 28 copper strips implemented in a printed circuit board (PCB) with 2.54 pitch. This way, the low-energy heavy ions pass through the emissive foil (placed at 45° respecting to the beam line at 0°) and the secondary electrons generated in the collisions are accelerated by an electrical field and focused by a longitudinal magnetic field toward the detector, which can be filled with different gas mixtures at low pressure (typically from 4 to 10 torr) for developing proposals.

The position in particle tracking is characterized by the spatial coordinates, which are in turn obtained by measuring and analyzing the center of gravity of the data generated by the charge distribution induced in the cathodes by the movement of the charge created inside the detector in an avalanche process. The ToF of the ions can be calculated from the anode signals of two different Mini-SeDs in the same beam line. The resulted time signals from the anode—after some amplification and conditioning—can be also used to trigger the QDC in

TABLE I
PHYSICAL PARAMETERS OF THE MINI-SED IN GEANT4

Parameter	Value
Energy of the incident beam	1MeV/u
Mylar window thickness	0.9μm
Emissive foil voltage	-10kV
Magnetic field	100G
Electric field	600V/m

Fig. 1, as will be shown later. The precise characterization of particles tracking—in terms of the spatial coordinates—strongly depends on the nature of charge signals provided by the detector cathodes, which indeed constitute the input signals for the readout electronic system driving the detector.

B. Readout Electronic Specifications

The Mini-SeD can be modeled as a current source for the behavioral high-level simulation of the readout electronic system to be designed. The most important electrical parameters that characterize the current signal provided by the detector cathodes are the following: 1) the peak current signals at each of the 64 cathodes, I_C; 2) the rise/fall time, $t_{r,f}$; and 3) the average time of an event, i.e., the arrival time of a particle, which is the inverse of the particles production rate—1 μs in the case of 10^6-p/s counting rate.

To obtain the most precise values for I_C and $t_{r,f}$, the Mini-SeD was simulated using GEANT4—a computer-aided design tool for the modeling and simulation of particle detectors [23], [24]. To this purpose, the dimensions and physical properties of the different materials used in the detector were included in the simulator, together with some of the physical conditions in which the Mini-SeD is going to operate—summarized in Table I.

Unfortunately, the model used in GEANT4 does not consider some important limiting factors like the avalanche currents produced at the active areas of the detector, the current induced by the secondary electrons at the cathodes, and the parasitic impedances and capacitances at the cathodes. These effects must be considered to obtain an accurate estimation of the electrical parameters of the current source. To this end, the behavioral model parameters used to model the Mini-SeD were completed and refined by comparing the system-level simulations with measurements taken on the Mini-SeD when tested together with an older electronic readout equipment at CEA-Saclay laboratories [19], [25]. Multiple system-level simulations were carried out to match the results obtained by the experiments under different conditions and production sources. According to these experimental tests and the simulations carried out using GEANT4, it was concluded that the Mini-SeD can be modeled as a current pulse source with the following parameters: pulse amplitude, $I_C = 23$ μA, and rise/fall time, $t_{r,f} = 10$ ns. These parameters constitute the system-level specifications for the electronic readout system developed in this paper and described in the following section.

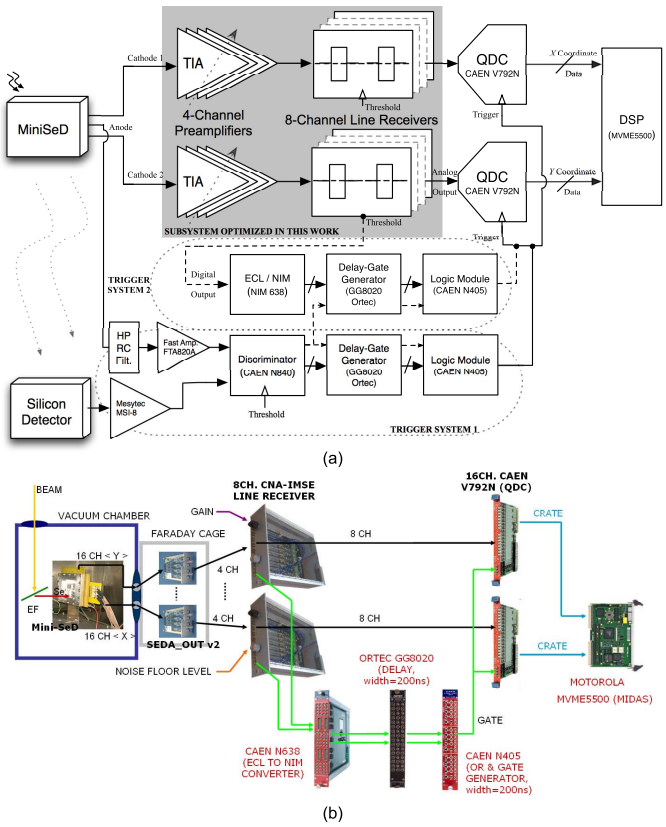

Fig. 3. Proposed readout system. (a) Conceptual architecture. (b) Block diagram highlighting the main parts and subcircuits.

C. Block Diagram of the Proposed Readout Electronic System

Fig. 3 shows the architecture of the proposed readout electronic detection system, which is intended to cope with the system-level specifications of the input current signal provided by the Mini-SeD cathodes. To this end, the Mini-SeD—placed inside a vacuum chamber—is connected to eight 4-channel[1] TIAs, which are driven by four 8-channel signal-conditioning line receivers that accommodate the signal ranges to be discriminated and digitized by two 16-channel V792N QDC modules from CAEN. The resulting digital data are finally processed by an MVME5500 single-board processor from Motorola, and statistically analyzed using using multi instance data acquisition system (MIDAS) [26]. This way, the presented system is able to extract the information related to the spatial coordinates (X, Y) in the trajectory followed by the particles, detected in a 16×16 main grid formed by the two cathodes of the Mini-SeD (Fig. 2).

To detect valid events, the QDC is triggered (depending on the detection system setup) only when a real particle is detected. To this purpose, the trigger signal can be generated by capturing the information related to the particles detected by both the anode of MiniSeD and a silicon detector. Then, a specific 200-ns pulsewidth signal waveform is generated

[1]The number of channels was chosen to adapt the presented readout electronics to the test equipment and experimental conditions available at CEA-Saclay laboratories, where the first measurements were carried out and compared with the previous preamplifiers and electronic readout systems. However, such a number of channels can be adapted to the required measurement set-up, based on the same architecture shown in Fig. 3.

TABLE II
ELECTRICAL CHARACTERISTICS OF THE MAIN READOUT BUILDING BLOCKS

Building Block	Parameter	Value
QDC (V792N)	Input impedance	50Ω
	Analog input range	$[-1\text{V},15\text{mV}]$
	Fixed Transient Delay	15ns
ELC-NIM Conv. (N638)	ECL logic zero range	$[-1.95,-1.48]$ V
	ECL logic one range	$[-1.17,-0.84]$ V
	NIM logic zero range	$[-0.20,1.00]$ V
	NIM logic one range	$[-1.80,-0.60]$ V
	Transient delay	2ns
Delay-Gate Gen. (CG8020)	Pulse width range	[70ns,1μs]
	Output delay range	[70ns,1μs]
	Fixed Transient delay	20ns
Logic Module (N405)	Pulse width range	[20,800ns]
	Fixed Transient delay	14ns

by the trigger system as the time window of the QDC for integrating the detected charge signal. This trigger system—denoted as Trigger System 1 in Fig. 3(a)—is made up of several parts. On the one hand, the signal provided by the silicon detector is amplified by an 8-channel preamplifier (MSI-8 from Mesytec). On the other hand, the signal provided by the Mini-SeD anode is filtered by a second-order *RC* filter, which acts as a low-pass (LP) filter for the supply voltages and as a high-pass (HP) filter for the anode output [Fig. 3(a)]. Both detected signals are compared with a threshold voltage in a 8-channel discriminator (N840 from Caen), which is used as the input for a delay-gate generator GG8020 from Ortec and, finally to a logic module N405 from Caen, that accommodates the data to trigger the QDC only when particles are detected by both detectors simultaneously, thus discriminating valid events from noise with an appropriate SNR. An alternative trigger generator—denoted as Trigger System 2 in Fig. 3(a)—can be used. This system is similar to the Trigger System 1, although the additional silicon detector is not used, since it is based on a digital control signal provided by the line receiver.

All the off-the-shelf components in the presented readout system of Fig. 3(b)—whose main electrical characteristics[2] are summarized in Table II—have been properly selected to cope with the required specifications of the particles spatial detection with Mini-SeD. However, due to the very demanding specifications for the preamplifier and the line receiver—in terms of SNR and transient response—to detect low-amplitude (<23 μA) current-mode signals with $t_{r,f} = 10$ ns, a specific design is carried out to optimize the performance of these subsystems according to these input signal and spatial detection system characteristics.

[2]Datasheets of all off-the-shelf IC parts used in the proposed readout system are available online.

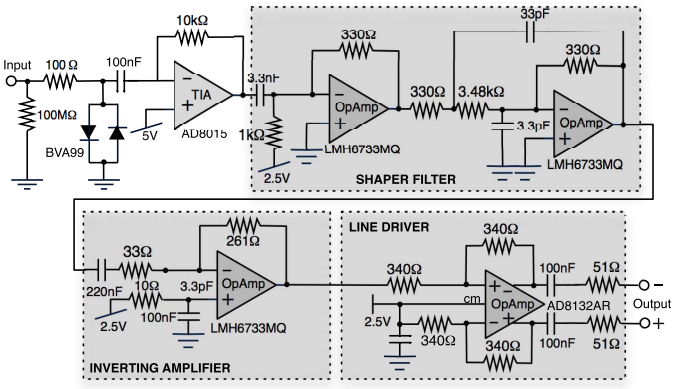

Fig. 4. Schematic diagram of one of the channels of the proposed preamplifier system (referred to as SEDA).

III. DESIGN OF MAIN BUILDING BLOCKS

The 4-channel preamplifier used in the readout system—referred to as secondary electrons detector preamplifier (SEDA) in Fig. 3(b)—has been designed to process charge signals coming from the Mini-SeD cathodes, tracking high counting rates of RIB with around 1 μs of average arrival time between the two consecutive particles. To relax the bandwidth specifications, the current signals waveforms coming from the cathodes—with peak amplitudes of 23 μA and $t_{r,f} = 10$ ns—are shaped so that they can be digitized by the QDC during an integration time period of 200 ns, i.e., a 20% of the average particles arrival time. This way, the number of events can be modeled as a Poisson distribution whose main parameters are $\lambda = 1$ μs and $K = 200$ ns, with λ and K being the average arrival and the integration time, respectively. Thus, there will be overlapping if two consecutive particles are detected within a 200-ns time frame. Taking this into account and that the detector output signals are current pulses with 20-ns duration, this constitutes less than 2% of overlapping probability between the two consecutive valid events. Another important design specification is the SNR, which should be high enough to discriminate current peaks generated in the cathodes when particles are detected, typically on the order of a few microamperes. Finally, other two important design parameters to be considered are the output impedance of 50 Ω and the input parasitic capacitance of 30 pF. The latter is limited by the cables used to connect each preamplifier channel—outside the vacuum chamber (Fig. 3)—to the detector.[3]

A. Preamplifier Topology and Simulated Performance

Fig. 4 shows the schematic diagram of one of the four (identical) channels of the proposed preamplifier. The circuit is composed of a TIA subcircuit, a shaper filter, an

[3]A PRO POWER RG179 coaxial cable with 40-cm length and 64 pF/m parasitic capacitance was used to connect the Mini-SeD–placed inside a vacuum chamber–and the proposed readout system. The overall load capacitance of 30 pF, was estimated from the coaxial-cable capacitance and those parasitic capacitances associated to the corresponding connectors–approximately 2 pF each one. Simulations carried out by using this lumped capacitor model–instead of considering the cable as a transmission line–allow us to accurately predict the parasitics effects associated to the cable.

ac-coupled inverting amplifier, and a line driver. An electrostatic discharge (ESD) diode-based protection circuit is placed at the input node to avoid damages caused by high voltage sparks and other experimental setup interference signals. The different preamplifier integrated circuit (IC) parts have been chosen to fulfill the required electrical specifications detailed above. To this purpose, a simulation-based design process has been followed from system-level specifications to building-block specifications and final physical (PCB) implementation. This way, a preliminary selection of several ICs was considered according to the electrical characteristics detailed in their data sheets, and they were simulated to select the most appropriate components that satisfy the overall system performance in terms of the required SNR and speed specifications.

The TIA in Fig. 4 was implemented using the AD8015 IC from analog devices. This circuit transforms the current signals coming from detector cathodes into voltage signals with a transimpedance gain of 80 dBΩ within a 240-MHz bandwidth, keeping the same value of the input $t_{r,f}$ and minimizing the probability of overlapping signals. In this configuration, this building block has an input referred noise spectral density of 3 pA/$\sqrt{\text{Hz}}$. The effects of parasitic capacitance on both signal bandwidth and noise figure have been considered in the simulations. Thus, considering a 30-pF input parasitic capacitance due to the cable, the TIA output total noise power is 3.35 mVrms within a 32.7-MHz signal bandwidth—in good agreement with the overall electronic front-end specifications described in Section II.

Another important block of the preamplifier system in Fig. 4 is the shaper filter, which is needed to slow down the preamplifier output signal. This block is implemented by a biquad filter configuration made up of a *RC* HP filter, a buffer, and a second-order LP filter. The cutoff frequency of the *RC* HP filter was set to 50 kHz to reduce the TIA output offset error and flicker noise. Both the buffer and the biquad filter were implemented using LMH6733 operational amplifiers configured with 0-dB gain, yielding a shaping time lower than 200 ns—in agreement with the required speed performance.

The gain of the preamplifier is provided by the fourth block in Fig. 4, implemented as an ac-coupled inverting amplifier based on the LMH6733MQ operational amplifier. This inverting configuration was designed and tested to have a variable gain from 0 to 18 dB, by properly changing the feedforward and feedback resistors connected to the opamp.

The last building block used in the preamplifier chain is a differential line driver. This block—implemented using an AD8132 opamp—was designed to properly transmit the required high-speed differential signals over 50-Ω coaxial cables connecting the preamplifier and the line receiver in Fig. 3, thus minimizing the line reflections as well as the common-mode and ground noise.

To validate the preamplifier performance, a number of simulations of the circuit in Fig. 4 were carried out using National Instruments Multisim [27], considering the SPICE models of all circuit components and building blocks, thus allowing us to make accurate simulations of the overall system. To this end, a 30-pF input parasitic capacitance and a current source with the same characteristics as Mini-SeD output current waveform signals, i.e., $t_{r,f} = 10$ ns, 23-μA current peak, and 1-μs period, were considered. Table III sums up the simulated performance, showing the main features for different values of the LP cutoff frequency at the shaper output. The 20-MHz bandwidth configuration was chosen to optimize the tradeoff between the required SNR and shaping time. Using this configuration, the main simulated performance metrics of the preamplifier are summarized in Table IV. As an illustration, Fig. 5 shows the transient response of one channel of the preamplifier considering an input current pulse, by depicting the output signal waveforms at the output of the main building blocks, and showing a correct performance of the circuitry.

TABLE III
SIMULATED PERFORMANCE OF THE SHAPER FILTER FOR DIFFERENT VALUES OF THE LOW-PASS FILTER (LPF) CUTOFF FREQUENCY

Cut-off Freq. (MHz)	10	15	20	25	30
Total Noise (mVrms)	1.60	1.61	1.63	1.68	1.78
Peak Voltage (mV)	54.0	81.0	102.0	118.0	130.0
Peak SNR (dB)	30.6	34.1	35.9	36.9	37.3
Fall/Rise time (ns)	38/92	35/63	33/37	30/27	29/26
Shaping time (ns)	300	200	170	160	160

TABLE IV
SIMULATED PERFORMANCE OF THE PREAMPLIFIER FOR DIFFERENT INVERTING AMPLIFIER GAINS AND 20-MHZ LPF CUTOFF FREQUENCY

Inverting amp. gain	4	8
Total Noise (mVrms)	3.28	6.57
Peak SNR (dB)	35.7	35.7
Peak Voltage (mV)	±200	± 400
Fall/Rise Time (ns)	33/37	33/37
Shaping Time (ns)	170	170

B. Line Receiver

As stated in the previous sections, a line receiver is used to adapt the output signals provided by the preamplifier to the electrical requirements of the QDC in Fig. 3.

Fig. 6 shows the conceptual schematic of one of the channels of the line receiver. It is made up of three main building blocks, namely, a programmable-gain differential amplifier, a comparator, and an *LC* passive filter. The front-end differential amplifier, implemented with an AD830JRZ IC part, transforms the fully differential input signal into a single-ended signal, and adapts the signal range to the QDC with a programmable voltage gain. This gain can be reconfigured from 1 to 8 by properly selecting the feedback resistor to be 1, 100, 300, and 700 Ω, with respect to the input resistor (100 Ω) using an ADG1412YRUZ switch from analog devices. These component values were chosen to get the

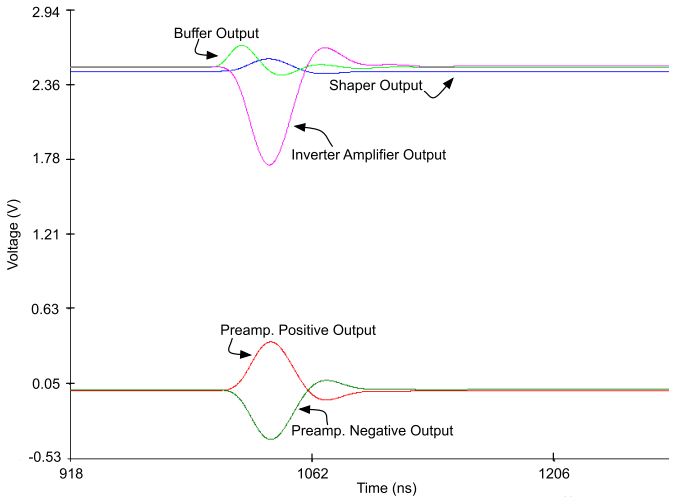

Fig. 5. Illustrating the simulated performance of the preamplifier. Note that the TIA output waveform is the same as the buffer output—depicted in this figure—except for the dc level (3.7 V for the TIA output and 2.5 V in the case of buffer output).

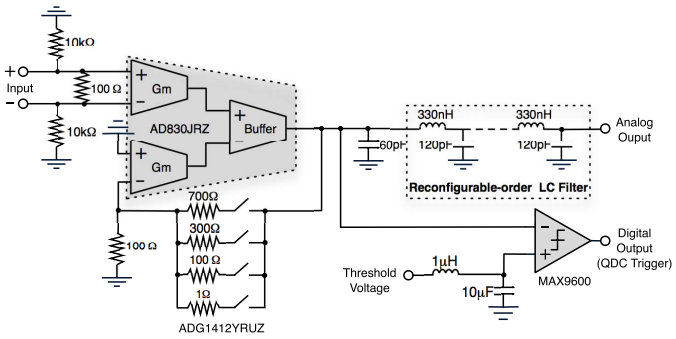

Fig. 6. Schematic diagram of one channel of the proposed line receiver.

desired performance even considering the impact of circuit parasitics.

The output of the line-receiver differential amplifier is used as an input to the comparator to generate a trigger signal that activates the QDC [Fig. 3(a)] only when a valid event (particle) is detected. This way, the comparator output provides a logic one if the amplifier output voltage is high enough compared with a tunable threshold voltage to guarantee that a valid event has been detected. Otherwise, the comparator output is a logic zero. The logic levels are set according to the emitter-coupled-logic (ECL) input range and noise margins of the ECL–Nuclear Instrumentation Module (NIM)[4] converter, thus being within [−0.84 and −1.17] V for a logic one and [−1.48 and −1.95] V for a logic zero, which are converted to the NIM logic digital input (gate) of the QDC.

The last block in Fig. 6 is an *LC* passive filter, which is used to synchronize both the digital input signal of the QDC (gate) with the analog output of the differential amplifier, so that the latter signal can be properly processed by the QDC within the time interval in which it is activated when a valid

[4]The term NIM logic is normally used to denote Nuclear Instrumentation Module logic.

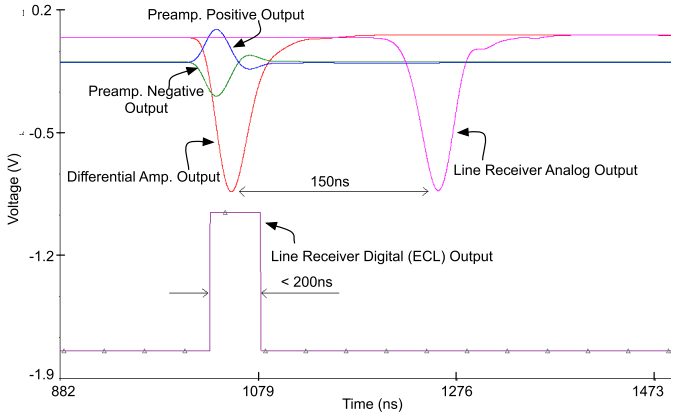

Fig. 7. Illustrating the simulated performance of the line receiver with unity gain.

TABLE V
SIMULATED PERFORMANCE OF THE LINE RECEIVER FOR DIFFERENT VALUES OF THE DIFFERENTIAL AMPLIFIER GAIN

Differential amp. gain	**1**	**2**	**4**	**8**
Peak Voltage (V)	−0.7	−1.16	−1.67	−2.11
Overall Gain	0.88	1.45	2.10	2.63
Shaping Time (ns)	150	160	185	290
SNR (dB)	34.7	33.9	30.6	26.1

event is detected—200 ns in our case. To this purpose, the filter order can be configured to achieve the required delay between both signals. A 150-ns delay can be obtained in our case with an *LC* filter of twenty-third order. This way, the gate signal delay can be tuned by the GG8020 block to synchronize that signal with the analog output of the line receiver (analog input of the QDC). Note that, as the input impedance of the QDC is 50 Ω, the *LC* filter must be designed to match this impedance within the required frequency range, i.e., from 50 kHz to 20 MHz. As an illustration, Fig. 7 shows the simulated waveforms at the output of main blocks of the line receiver, when it is excited by a preamplifier output signal of ±400-mV peak voltage, demonstrating a correct timing and synchronization. Table V sums up the simulated performance of the line receiver, showing its main features for different differential amplifier gains.

IV. SYSTEM IMPLEMENTATION AND MEASUREMENTS

The proposed readout system has been designed to work outside the vacuum chamber, in which the Mini-SeD is placed. The connection between the detector and the electronic front-end is shown in Fig. 8(a), illustrating the detailed implementation of the 4-channel preamplifier [Fig. 8(b)] and the 8-channel line receiver [Fig. 8(c)]. A number of experiments have been carried out to verify the performance of the presented readout system, considering the signal stimuli and environment conditions detailed in the following sections.

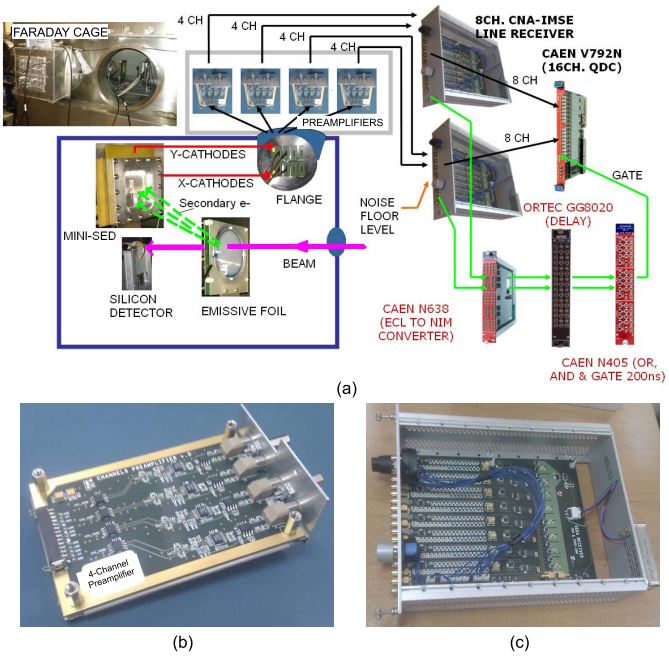

Fig. 8. Implementation of the proposed readout system and measurement setup. (a) Connection with the vacuum chamber including the Mini-SeD. (b) Preamplifier PCB subsystem. (c) Line receiver PCB subsystem.

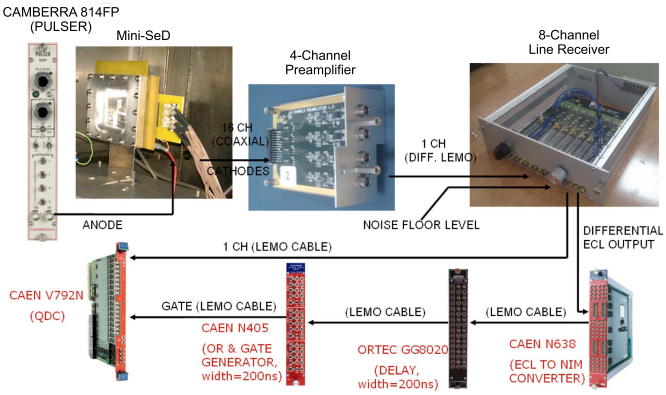

Fig. 9. Measurement setup used in the pulse-generator experiment.

A. Pulse Generator Experiment

The first experiment was based on a pulse generator input signal, which emulates the input signal applied at the anode of the Mini-SeD. To this purpose, the instrumentation setup shown in Fig. 9 was considered. An impulse signal waveform, with a peak amplitude of 0.45 V, 20-ns rise time, and 10-ms period, was used to induce the same quantity of charge in the Mini-SeD cathodes, thus emulating a particle detection event.

The cathodes output current signals were transmitted by the cables to the feedthrough connectors installed on the flange of the vacuum chamber, which has been developed for connecting detectors inside with the readout system outside the chamber. Thus, after being preamplified, fully differential signals with ±200-mV peak voltage and 150-ns shaping time are obtained.

Fig. 10 shows the analog output waveforms obtained for different values of the differential-to-single-ended gain

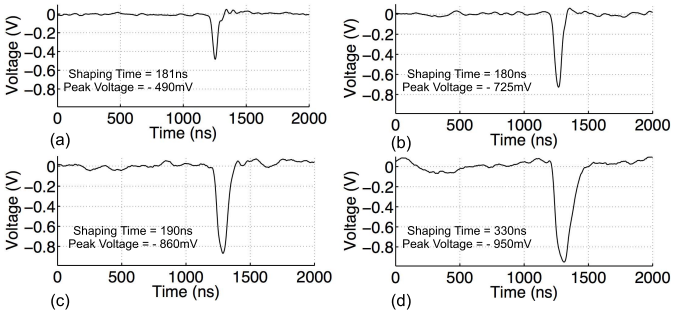

Fig. 10. Output waveforms of the line receiver for an input pulse and different values of the differential-to-single-ended gain. (a) Gain = 1. (b) Gain = 2. (c) Gain = 4. (d) Gain = 8.

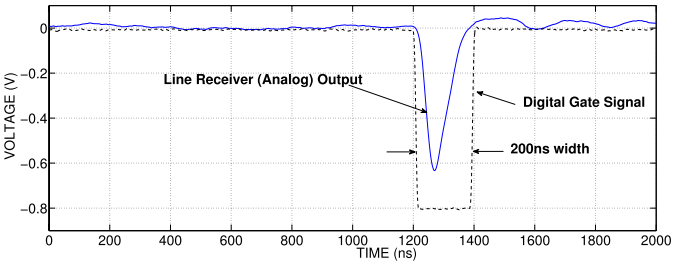

Fig. 11. QDC inputs: digital gate signal and line receiver analog output.

programmed from 1 to 8. It can be shown as to how the output signal of the proposed line receiver has a reconfigurable gain, $t_{r,f}$, and shaping time of 1.2–2.4, 70–228, and 180–330 ns, respectively. These waveform characteristics are in good agreement with predicted simulation performance and are very appropriate to be digitized by the QDC.

Note that, the QDC needs to be activated only when a real event is detected. This is illustrated in Fig. 11 that shows the digital gate signal generated by the trigger system 2 [Fig. 3(b)] with the digital output signal of the line receiver. Note that the analog signal can be perfectly detected and integrated by the QDC, because the trigger signal is only generated when an input pulse is detected. The 200-ns width gate signal provided by this trigger is generated and delayed by the GG8020 module to be synchronized with the analog output, thus guaranteeing a correct detection of real events, even considering the effect of variations in the component values of different channels.

B. Experiment With a Source of α Particles

The second experiment was carried out using a triple source of Plutonium (^{239}Pu), Americium (^{241}Am), and Curium (^{244}Cm), which emit α particles with an average energy of 1.29, 1.37, and 1.48 MeV/u, respectively. As illustrated in the instrumentation setup shown in Fig. 8, the secondary electrons generated by the α particles in the emissive foil, are guided to the active volume of the detector, where they ionize the gas inside, generating electron-ion pairs. The produced electrons generate new ionizations, in the gas, which means more charge (ion and electrons) that are measured by the anode and cathodes and transmitted to the readout system. The electrons distribution around the cathodes gives us the position of the incident particle.

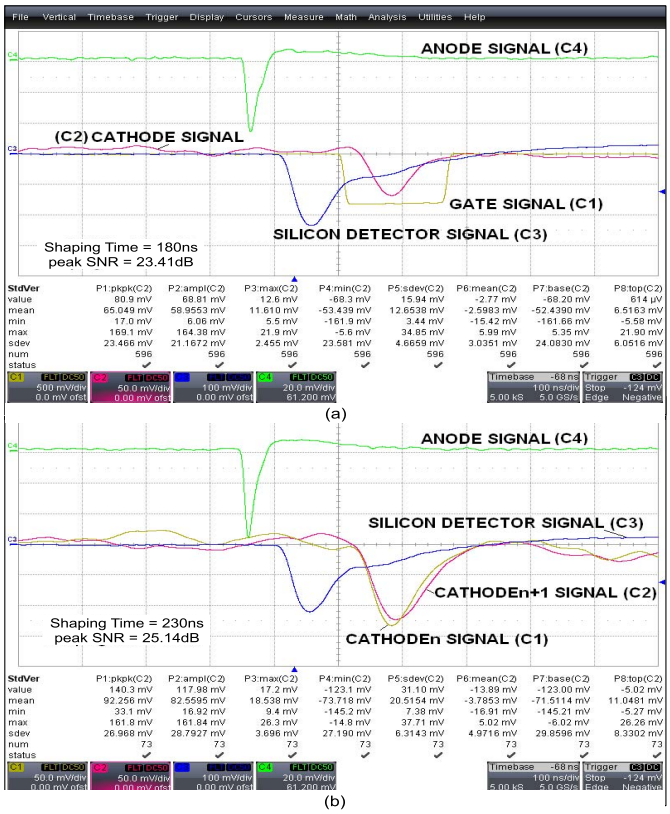

Fig. 12. Output waveforms of the readout system for an input source of α particles and different gains of the receiver line. (a) Gain = 2. (b) Gain = 4.

Fig. 12 shows the signal waveforms of the most important nodes of the readout system, corresponding to different gains of the line receiver, illustrating how the proposed readout system is able to process valid events obtained from real sources. Noise-level measurements are shown in the figure, demonstrating that a maximum peak SNR of 25.1 dB with shaping times of 170–230 ns can be achieved.

C. Experiment With a ^{58}Ni Particle Beam

The third experiment was carried out using a nickel (^{58}Ni) beam at a high counting rate, whose accelerated particles pass through an emissive foil, and as a result of the interactions, secondary electrons are generated and detected by the Mini-SeD (in the same way as explained in Section IV-B). In this case, a single channel silicon surface barrier detector is used to measure the particles of the ^{58}Ni beam after crossing the emissive foil (Fig. 8). This event is also used by the trigger system generator to activate the QDC only when a real particle is detected.

Fig. 13 shows the main output waveforms obtained by the readout system, demonstrating a correct performance to process two consecutive events, with a time delay between them of approximately 400 ns, which means a detection rate over $2.5 \cdot 10^6$ p/s. Finally, Table VI shows the measured performance summary of the readout system, for the different experimental conditions considered. Note that the values of the measured SNR are approximately 5–10 dB lower than those obtained by simulation—shown in Table V. This is

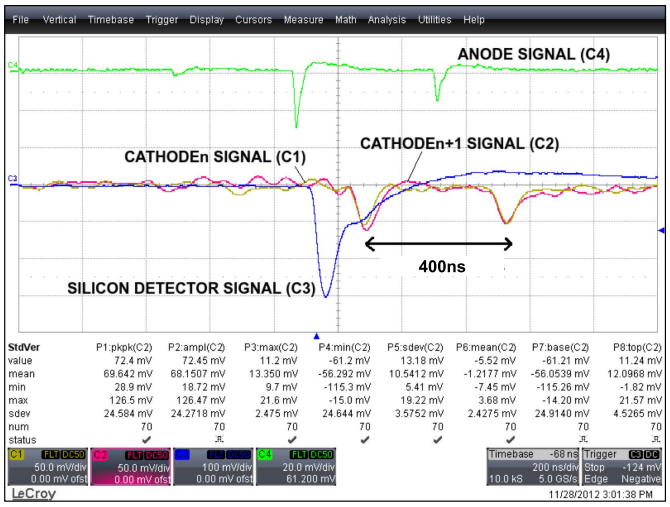

Fig. 13. Output waveforms of the readout system for a ^{58}Ni particle beam.

TABLE VI
MEASURED PERFORMANCE SUMMARY

Receiver Gain	peak-SNR (dB)	Shaping Time (ns)
Source of α particles		
1	23.2	170
2	23.4	180
4	25.1	230
^{58}Ni Particle Beam		
1	23.8	170
2	23.8	180
4	24.1	230

mainly due to external noise sources and electromagnetic interferences, which are present in the measurement setup and lab equipment. To attenuate these effects, different strategies were

considered in the designed PCBs, including among others: the use of separate planes for digital and analog signals; regulators to keep the values of voltage supplies stable; decoupling capacitors in the supply, biasing, and reference signals; and ESD protection diodes, etc. However, in spite of applying these circuit techniques, it is not possible to completely remove some external interferences, especially in a complex lab environment like that considered in this paper. Nevertheless, the values of the measured shaping times and peak SNRs achieved, demonstrate the suitability of the presented readout system to detect particles at rates over 10^6 p/s.

V. CONCLUSION

A complete readout electronic system for precise spatial detection in tracking of low-energy ion beams at a rate over 10^6 p/s has been presented. Instead of using a charge-sensitive preamplifier, the proposed system uses a multi-channel TIA circuit, which has demonstrated to be more

efficient than the previously reported preamplifiers to detect consecutive events with a delay below 400 ns. The proposed front-end electronics is complemented by a line receiver to adapt the detected signals before being digitized by a QDC. These blocks are combined with other off-the-shelf electronic parts to target the required physical characteristics of Mini-SeD. Diverse experimental measurements are shown to validate the presented approach, which constitutes a very promising strategy for the implementation of front-end electronic systems in the next generation of particle accelerators.

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