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A Wideband Down-Converter MMIC with Gain Control for Digital Radio Systems

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A Wideband Down-Converter MMIC with Gain Control for Digital Radio Systems

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Abstract — **This work describes the development of a monolithic microwave integrated circuit (MMIC) down-converter, which integrates a five stage variable gain low-noise amplifier (LNA) and an image-rejection diode mixer. The circuit was implemented with a 40 GHz PHEMT (pseudomorphic high electron mobility transistor) GaAs technology, and operates over the 5.8 to 8.5 GHz band. The measured average noise figure is 2.5 dB and the average gain is 26 dB, with a control range of 35 dB. The MMIC was mounted and characterized in a commercial BGA (ball grid array) package, for application in digital radio systems.**

Index Terms — **MMIC, down-converter, wideband microwave circuit, digital radio system.**

I. Introduction

The MMIC technology offers attractive advantages over its hybrid counterpart, in terms of compactness, low power consumption, reliability and low parasitics, leading to wideband operation. The maturity achieved by this technology, which results in circuit high yield and repeatability, have considerably reduced the price and time for design prototyping. MMIC technology based on pHEMT devices (0.25 μm gate) offers high performance for both high power and low noise design up to 30 GHz.

A MMIC down-converter has been developed, in order to explore these characteristics. Design specifications were based on the 5.8 to 8.5 GHz digital radio band, and the circuit was fabricated at Triquint-Texas Semiconductor GaAs foundry [1]. A MMIC wideband down-converter, featuring gain control, has resulted and is being used for replacing several MIC hybrid blocks, each one specifically tuned for a particular receiver sub-band.

II. Circuit Design

The MMIC down-converter integrates a low-noise variable gain five stage pHEMT amplifier and an image-rejection diode mixer. LO band covers 5.8 to 8.4 GHz, RF band varies from 5.9 to 8.5 GHz, and IF is centered in 70MHz (55 to 85 MHz).

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Four variable attenuators are included at the amplifier inter-stages, and connected to a control voltage VC (-2 to 0V), so that the amplifier gain can be automatically controlled. Input RF power can vary from –90 to –20dBm. The AGC circuitry operates from –45 to –20dBm, in order to maintain the amplifier output power at a constant level (-8 dBm), as well as guaranteeing third-order intermodulation (IM3) specifications at any conditions. Each amplifier transistor is independently biased, and drain currents can be adjusted for optimum noise and gain performance.

The mixer was designed using a phasing scheme for separating signal from image response. PHEMT diodes were employed in the single-balanced mixer structure, and lumped elements were used for implementing the power divider modules, as means for minimizing the GaAs circuit area and broadening operation bandwidth.

The blocks that compose the amplifier and mixer were separately designed in schematics and layout formats, and gradually integrated to their final structure. HP-EESOF [2] and Triquint-Texas MASC libraries [1] were the CAD tools used in the MMIC design and simulation.

A. *Low Noise Amplifier*

A block diagram of the low-noise amplifier is depicted in Fig.1. All stages were implemented using (8x50μm) pHEMT devices. As a first design step, a fitting procedure on the non-linear parameter model was carried out for approximating S-parameters obtained from linear and non-linear transistor models, at nominal bias conditions (Vds=3V; Vgs=-0.52V; Id=40mA).

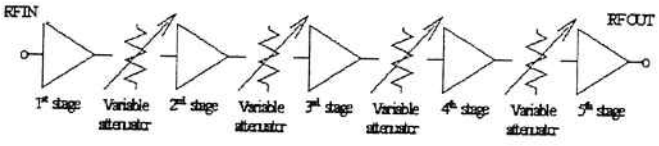

Fig.1 LNA Block Diagram

In the first stage, a short circuit terminated microstrip line provided an inductive series feedback at the transistor source, in order to improve circuit stability and ease input matching for optimum noise figure [3]. Output matching network of the first stage, as well as all other matching networks for the other stages were designed for optimum gain conditions, and implemented with lumped components.

The key element of the variable attenuators is a cold pHEMT (dimension 4x75μm), parallel connected to the circuit (Fig.2). It operates as a variable resistance, as the drain voltage is null, and the gate bias varies between –2V (no attenuation) and 0V (maximum attenuation). In order to minimize the influence of such variable components on the frequency response of the amplifier, two fixed pads were connected at each port of the attenuator.

The final circuit was optimized for low noise, high gain, flat frequency response and good intermodulation performance. Linear transistor models were used for simulating noise and phase delay. Non-linear models and test benches were employed in the simulation of gain and intermodulation performance. Some simulated results obtained for the LNA circuit are shown in Figs.3, 4, 5 and 6 and in Table I. Figs. 5 and 6 show the action of the variable attenuators and AGC circuitry, decreasing the gain as the input power level increases, and maintaining output power level fixed at –8 dBm.

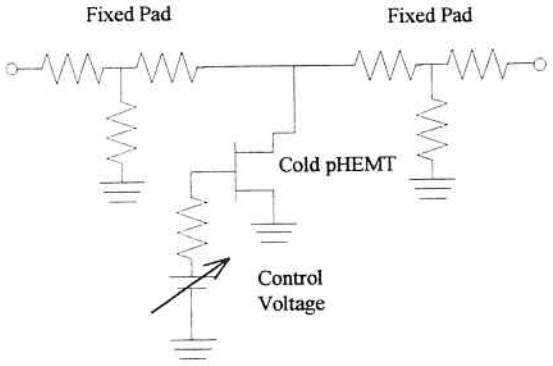

Fig.2 Cold pHEMT Variable Attenuator

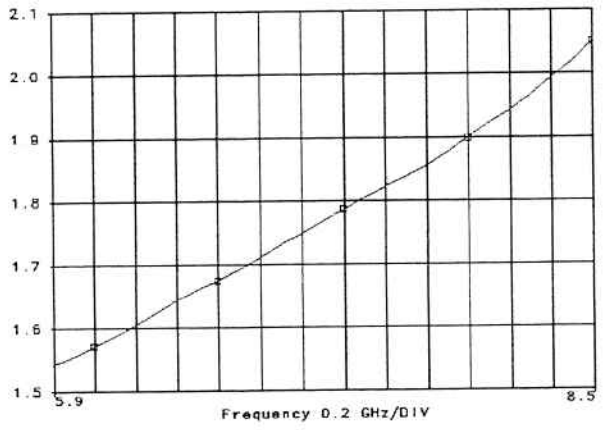

Fig.3 LNA Simulated Noise Figure

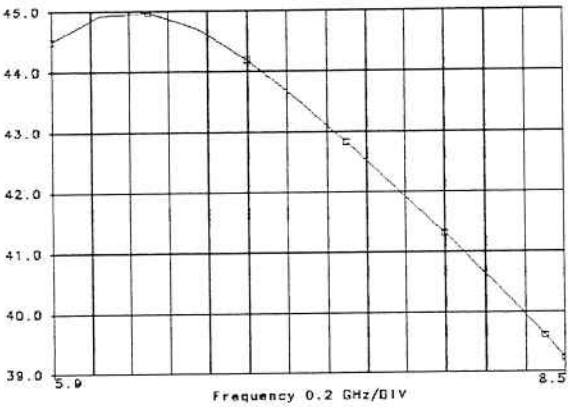

Fig.4 LNA Simulated Gain

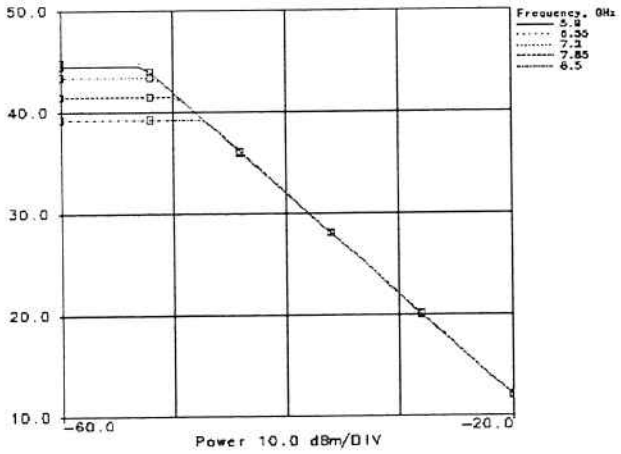

Fig.5 LNA Simulated Gain as function of input power

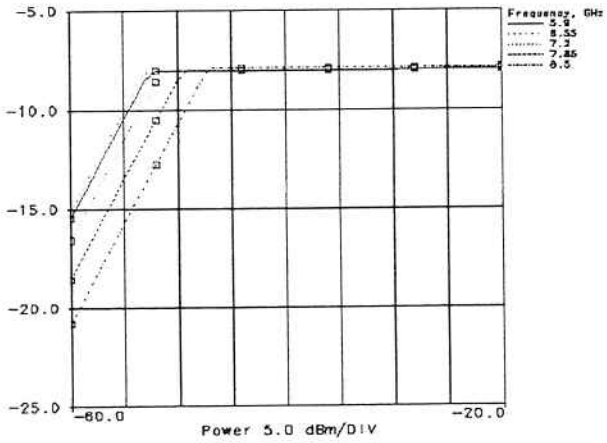

Fig.6 LNA Simulated Output power as function of input power

TABLE I
LNA SIMULATED CHARACTERISTICS

Input Return Loss	≥ 6 dB
Output Return Loss	≥ 12 dB
3rd order intermodulation	≥ 56 dBc

B. Image-Rejection Mixer

The image frequency problem may be overcome by employing the structure shown in Fig.7, named image-rejection mixer [4].

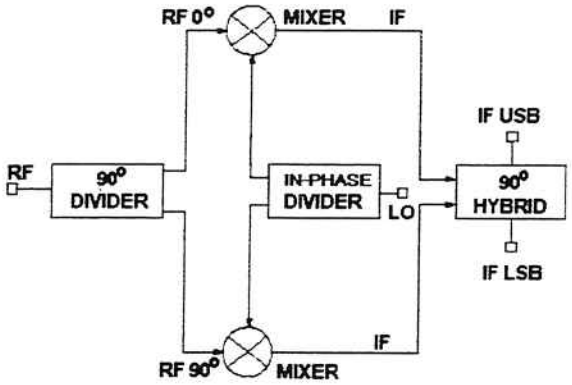

Fig.7 Diagram of Image-Rejection Mixer

The image-rejection mixer is composed by two identical mixers, fed by in-phase LO input signals and 90° out-of-phase RF signals. At the output of both mixers, an IF hybrid is connected to separate the USB (upper-side-band) from the LSB (lower-side-band) IF products. Each basic building block of the image rejection mixer is described next.

1) Local Oscillator Power Divider:

The topology of the local oscillator power divider is based on a lumped element, low-pass Wilkinson power divider (Fig.8) [5], which divides the incident power at port P1 equally between ports P2 and P3.

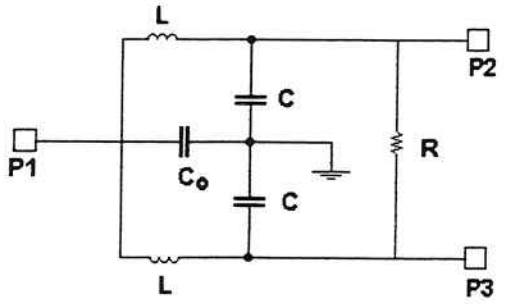

Fig.8 Schematics of Lumped-Element Power Divider

The values of the elements are calculated according to [6]:

$$R = 2Z_0 \qquad L = \frac{\sqrt{2}Z_0}{\omega_0} \qquad C = \frac{1}{\sqrt{2}Z_0\omega_0} \qquad C_0 = 2C$$

where Z_0 is the characteristic impedance (50Ω) and ω_0 is the center angular frequency.

2) 90° RF Divider:

The RF signal must be symmetrically split, but with a 90° phase difference between the outputs. This can be accomplished by cascading LC networks to the output ports of the Wilkinson power divider, as presented in Fig.9.

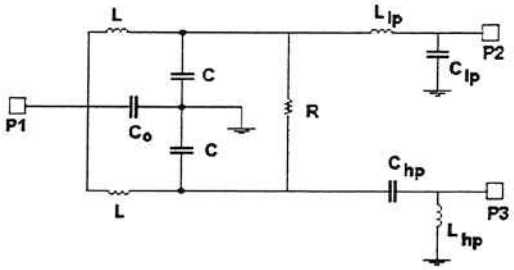

Fig.9 Lumped-Element RF Hybrid

The power divider is followed by two filters – a low-pass (L_{lp} and C_{lp}) and a high-pass (L_{hp} and C_{hp}). The poles of their transfer functions are located, respectively, at $1/(L_{lp}C_{lp})$ and $1/(L_{hp}C_{hp})$. By the appropriate choice of the element values, it is possible to make each filter phase response resulting in 45°, adding up the desired 90° at the center frequency. The electrical performance of the power divider is perturbed by the presence of the filters, and optimization must be applied in the design process.

3) 180° Mixer Hybrid:

The balanced basic mixer employs a 180° rat-race lumped-element coupler. The basic circuit is presented in Fig.10.

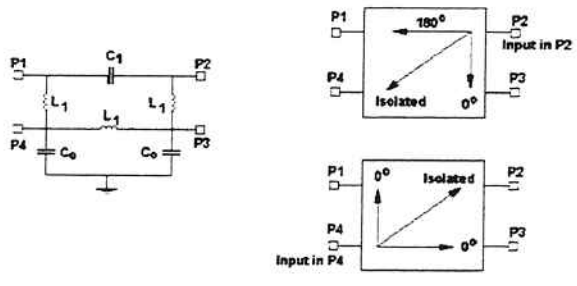

Fig.10 Lumped-Element 180° Hybrid

The design equations [6,7] are:

$$L_1 = \frac{\sqrt{2}Z_0}{\omega_0} \quad C_0 = \frac{\sqrt{2}}{\omega_0 Z_0} \quad C_1 = \frac{1}{\sqrt{2}\omega_0 Z_0}$$

4) Low-Pass Filters:

Low-pass filters, implemented with a single LC section, are used in the mixer circuits for extracting the IF signal. A cut-off frequency of about 500 MHz represents a reasonable tradeoff between performance and component values. It should be noticed that capacitor values must be chosen within a given range, limited by the foundry process. Very large inductors are also undesirable, for their large dimensions, which increases parasitics and electromagnetic coupling.

5) Diode Modeling:

The mixer design was based on an available IPHC (intermediate-power, high-current process) diode model, provided by the foundry [1]. However, the actual circuit was implemented on pHEMT technology. The differences between simulated and measured results might be ascribed to the variation in the model parameters of both devices. Later, some pHEMT diode samples (4x37.5μm) were sent by the foundry (together with the down-converter chips), and then the parameter models were extracted. The procedure consisted in: -DC measurement of the diode IxV characteristic, performed with a HP4145 Curve Tracer; and -AC impedance response, obtained from the S_{11} parameter, with the diode cathode grounded [8]. The latter measurement was implemented using an automated network analyzer HP8510. Table II outlines some differences between the averaged parameters obtained from measured pHEMT diode samples and the original IPHC diode model. Posterior simulations have shown a significant dependence of mixer performance upon diode parameters.

TABLE II
DIODE MODEL PARAMETERS (4x37.5μm devices)

Parameter	IPHC	pHEMT
R_S [Ω]	3.27	8
I_S [A]	$2.37\ 10^{-13}$	$4.6\ 10^{-11}$
N	1.14	1.86
BV [V]	4.05	7.83
VJ [V]	0.71	0.69
C_{j0} [pF]	0.214	0.192

R_S : series resistance
I_S : saturation current
N: ideality factor
BV : breakdown voltage
VJ : forward knee voltage
C_{j0}: zero-bias diode capacitance

6) Single-Balanced Mixer:

The basic schematic of the single balanced mixer is depicted in Fig.11.

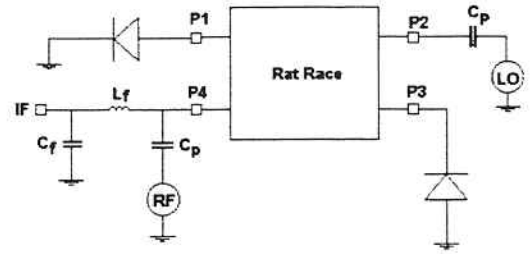

Fig.11 Diagram of single-balanced mixer

The mixer is composed by the 180° hybrid (rat-race), a low pass filter (L_f and C_f), block capacitors (C_p) and two identical pHEMT diodes. The RF signal is applied to the hybrid port P4, resulting in-phase on both diodes, unlike the LO signal, fed at port is P2 and being 180° out of phase on the diodes. The hybrid provides isolation from one source to the other (OL and RF). The high amplitude LO signal, incident 180° out of phase on the diodes, modulates the conductance of both devices. Since they are connected out of phase, i.e., one with its cathode grounded and the other with its anode grounded, both will show an in-phase modulated conductance. Therefore, the RF signal will be presented with a time variant conductance in both diodes, which results in the mixing products being generated. The block capacitors were chosen to be 2 pF.

The monolithic balanced mixer layout is presented in Fig.12. The IF filter was implemented with two parallel capacitors, adding up 6 pF. The large area required by the inductors is one of the tradeoffs when disposing the elements in the layout workspace. The circuit occupies an area of 1,800 μm (x-axis) by 1,100 μm (y-axis).

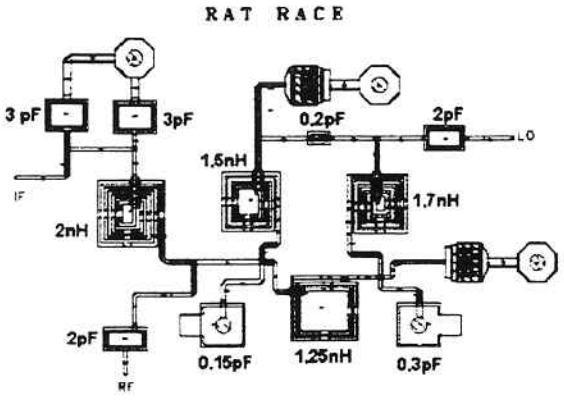

Fig.12 Layout of MMIC balanced mixer

The simulated results obtained for the balanced mixer are shown in Figs.13 and 14.

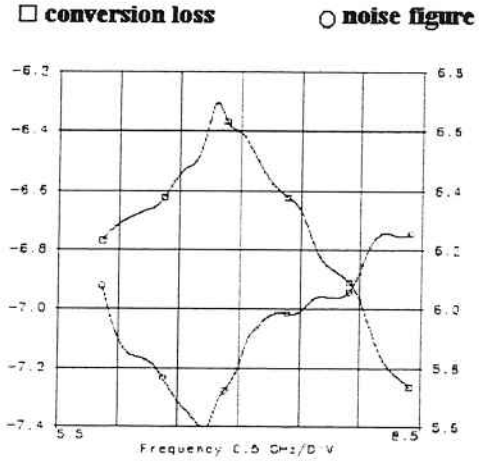

Fig.13 Simulated Conversion Loss and Noise Figure of balanced mixer

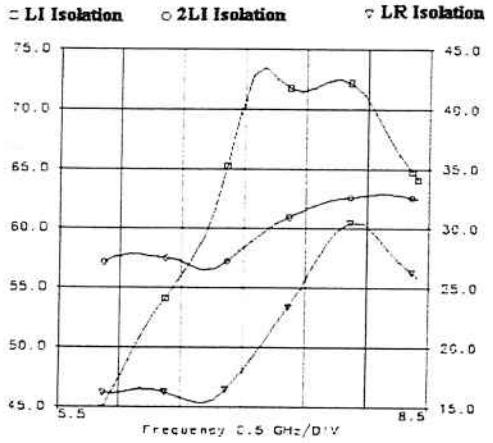

Fig.14 Simulated L/I, 2L/I and L/R isolations of balanced mixer

The simulated results show a conversion loss lower than 7.2 dB, and noise figure lower than 6. The isolation between the LO and IF port is higher than 46 dB. The circuit was simulated with a LO power of 13 dBm, a level for which the conversion loss is minimum at the center frequency (7.2 GHz). Under the same conditions, simulated IP3 point was obtained at 13.4 dBm of RF input.

7) Image-Rejection Mixer:

The image rejection mixer was composed from the previously described circuits. The final layout is presented in Fig.15.

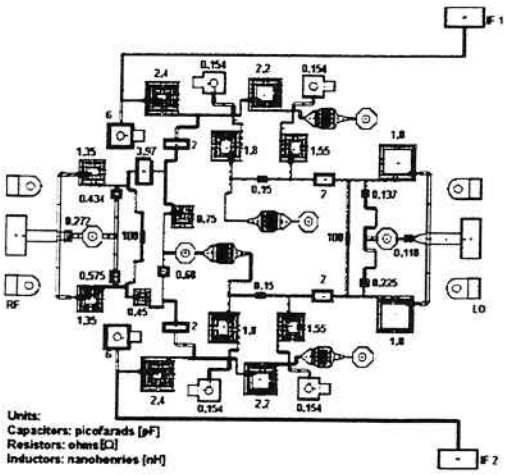

Fig.15 Layout of image-rejection mixer

The circuit occupies an area of 3,106 μm (x-axis) by 3,000 μm (y-axis). It is noted that both IF ports contain the IF USB and LSB responses. The IF hybrid is located off-chip and its role is to separate these IF responses. The chosen IF hybrid output port should correspond to the translated RF signal. The other output port should be terminated by a load. The ratio between the desired and the image response, at the chosen IF port, is named image rejection, as presented in Fig.16.

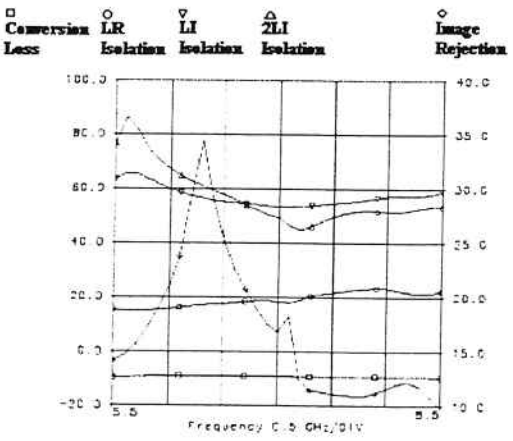

Fig.16 Simulated results of image-rejection mixer

A flat conversion loss can be observed over the operation band. However, the image rejection parameter is a tuned characteristic, since it depends on the amplitude and phase response of the power dividers, and is very sensitive to the symmetry of the image-rejection structure. Such symmetry is more easily obtained in monolithic implementations than in its hybrid counterpart. This explains the wider operation bandwidth that can be achieved with monolithic image-rejection mixers.

III. Circuit Characterization and Results

The final down-converter layout is shown in Fig.17. A photograph of the MMIC is reproduced in Fig.18. The chips were mounted in BGA (ball grid array) packages [9] and inserted in a test jig for characterization (Fig.19).

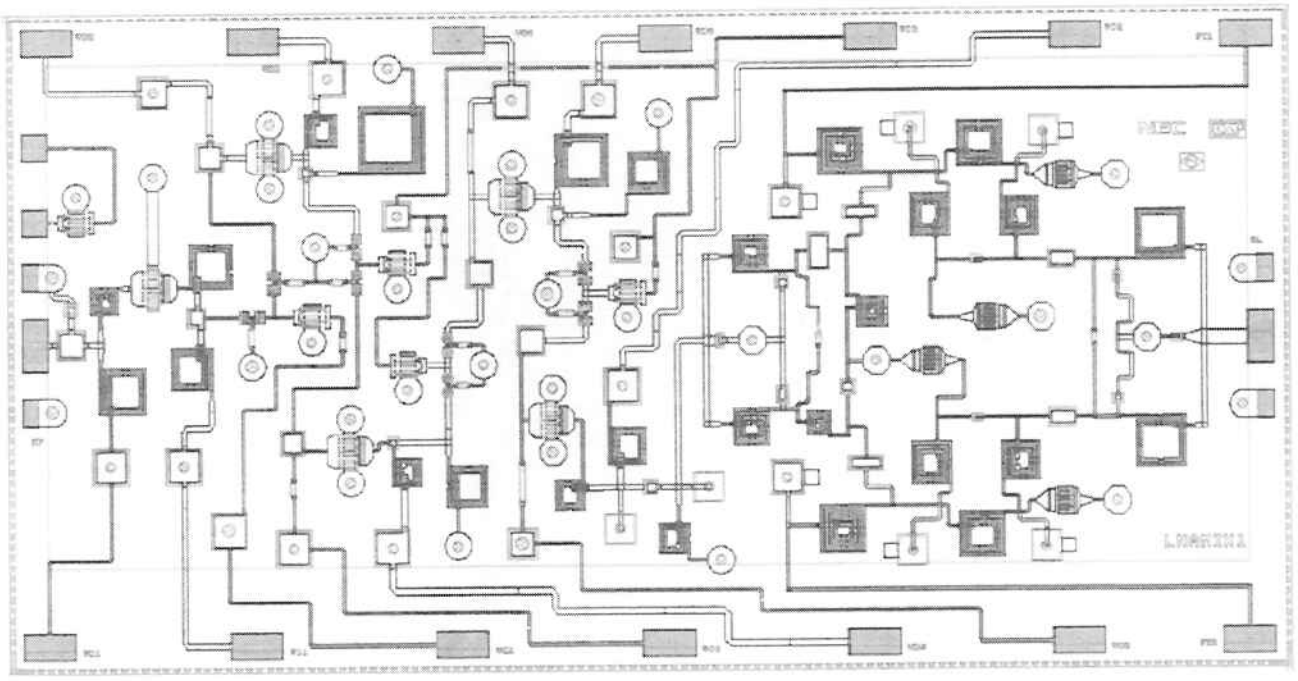

Fig.17 Final Layout of Down-Converter

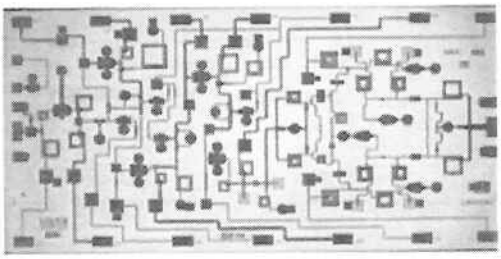

Fig.18 Photograph of MMIC Down-Converter (6.3 x 3.2 mm^2)

The test jig included the IF hybrid, as well as bias and control circuitry. Measurements of the down-converter were performed using sweep generators, a spectrum analyzer (*HP8565E*) and a Noise Figure Meter (*HP8970B*). The local oscillator power was adjusted in + 16 dBm at the mixer input. Measurements and simulations were performed under the same conditions, over the operating band. Fig.20 shows the down-converter simulated and measured gain for the two extreme control voltages (0V and –2V). Other spare conditions of control voltages are also represented, for maximum IF output level (-18 dBm). In Fig.21, the measured gain results for eight chips are presented comparatively with the simulated curve, for control voltage set at –2V (no attenuation). It can be seen that simulation predicted higher gain values than the actually measured results. Such variation could be explained by differences between the diode model parameters (as design was based on IPHC diode model, and the circuit was fabricated with pHEMT diodes) and imperfections in the pHEMT models.

Fig.22 shows the image rejection simulated and measured characteristics for various samples of the down-converter, over the operation band. Although image rejection degenerates towards the higher limit of frequency band, this parameter can be easily tuned through an extra variable capacitor connected between the input terminals of the IF hybrid.

The measured noise figure for eight different chips are displayed in Fig.23. It can be noticed that for all measured characteristics, there is not much dispersion over tested samples, showing a very stable technological process. Table III summarizes the specifications and measured down-converter performance.

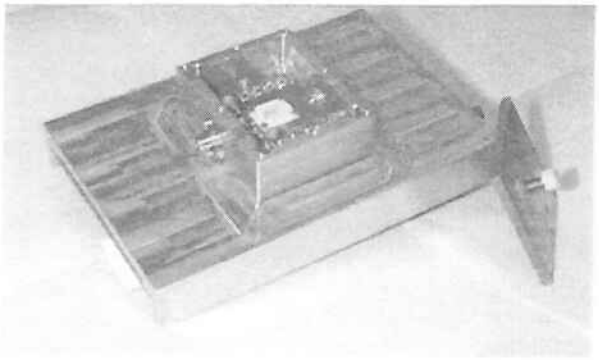

Fig.19 Photograph of MMIC Down-Converter mounted in Test Jig

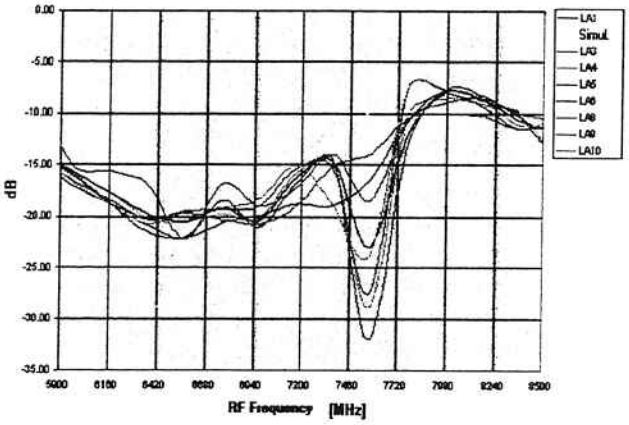

Fig.22 Down-Converter Simulated Image Rejection and and Measured Results for different chips (VC=-2V)

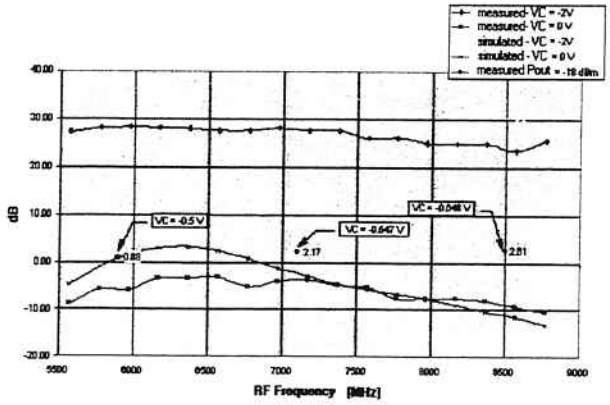

Fig.20 Down-Converter Simulated and Measured Gain (P_{OL}=+16 dBm, P_{RF}= -45 dBm). VC=control voltage

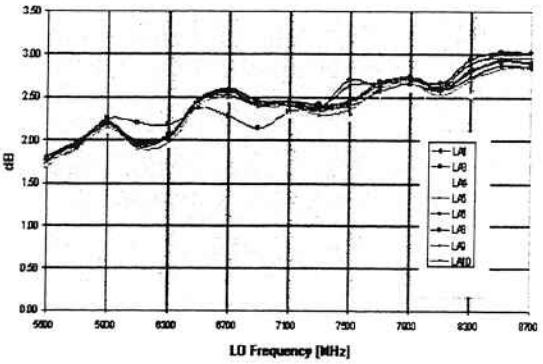

Fig.23 Down-Converter Measured Noise Figure for eight different chips (VC=-2V)

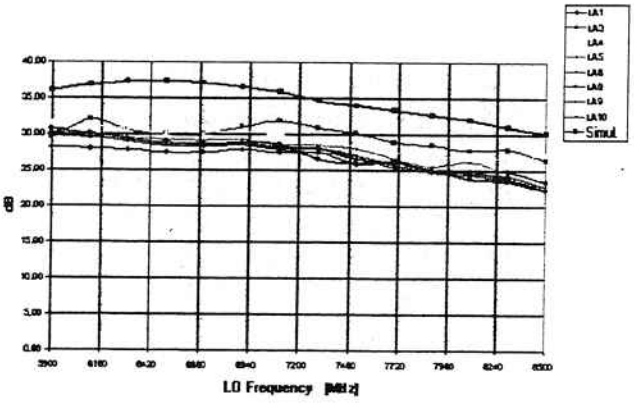

Fig.21 Down-Converter Simulated Gain and and Measured Results for eight different chips (VC=-2V)

TABLE III
DOWN-CONVERTER SPECIFICATIONS AND MEASURED CHARACTERISTICS

LO Band	5.8 to 8.4 GHz
RF Band	5.9 to 8.5 GHz
IF Band	55 to 85 MHz
Linear Gain	26 ± 4 dB
RF input level range	-90 to –20 dBm
LO power level	+ 16 dBm
Noise Figure	≤ 2.8dB
Image Rejection	≥ 8 dB
LI Isolation	≥ 50 dB
3rd order intermodulation	≥ 50 dBc
Output power 3rd order intercept point	+8dBm
RF Input Return Loss	≥ 5 dB
LO Input Return Loss	≥ 8 dB
IF Output Return Loss	≥ 12 dB
DC power consumption	0.6W

IV. Conclusion

The development of a MMIC down-converter based on a 0.25 μm PHEMT GaAs technology has been described. The circuit operates over a wideband (5.8 to 8.5 GHz), with low DC power consumption (600 mW), integrating a low-noise variable-gain five stage amplifier and a diode image-rejection mixer. The chip features 26 dB average gain, with 35dB control range, achieved through four variable cold pHEMT attenuators placed between amplifier stages, and controlled by an AGC circuitry. Average measured noise figure is 2.5dB, and image rejection higher than 10 dB can be obtained over the band. Circuit linearity guarantees third order intermodulation products down to 50 dBc or more, at any conditions, and third order intercept point at +8dBm output IF power. The MMIC was mounted in a commercial BGA package. The characterization of eight different packaged samples, inserted in a special test jig, showed a low dispersion in the MMIC performance. The MMIC fulfils all the specified requirements for operating in digital radio systems, replacing various tuned hybrid down-converters.

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