Reducing Soft Error Rate of SoCs Analog-to-Digital Interfaces With Design Diversity Redundancy

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***Abstract*— In this article, a commercial programmable system-on-chip (PSoC 5, from Cypress Semiconductor) is tested under heavy-ion irradiation with a focus on the analog-to-digital interface blocks of the system. For this purpose, a data acquisition system (DAS) was programmed into the device under test and protected with a design diversity redundancy technique. This technique implements different levels of diversity (architectural and temporal) by using two different architectures of converters (a ΣΔ converter and two successive approximation register (SAR) converters) operating with distinct sampling rates. The experiment was performed in a vacuum chamber, using a ^{16}O ion beam with 36-MeV energy and sufficient penetration into the silicon to produce an effective linear energy transfer (LET) of 5.5 MeV/mg/cm^2 at the active region. The average flux was approximately 350 particles/s/cm^2 for 246 min. The individual susceptibility of each converter to single-event effects is evaluated, as well as the whole system cross section. Results show that the proposed technique is effective to mitigate errors originating at the converters since 100% of such errors were corrected by using the diversity redundancy technique. Results also show that the processing unit of the system is susceptible to hangs that can be mitigated using watchdog techniques.**

***Index Terms*— Design diversity, mixed signal, programmable system-on-chip (PSoC), single-event effects (SEEs), soft errors.**

I. Introduction

RELIABILITY of electronic devices, especially the ones aimed at space applications and man-made radiation environments, is a challenge for integrated circuit (IC) designers. These systems can be affected by radiation due to ionizing particle strikes in sensitive areas of the IC, which may cause a current disturbance, leading to soft errors [1], [2]. These errors may cause bit flips in memories, corrupt operation in processing units, and even cause permanent damage in systems [3], [4].

Electronic systems applied to control, instrumentation, and communication tasks comprise mixed-signal (MS) interfaces that include analog-to-digital converters (ADCs). These circuits are crucial in satellites, spacecraft, and data acquisition systems (DASs) of nuclear facilities and particle accelerators. Therefore, besides the correct functioning of computing units, the reliability of analog-to-digital (AD) and digital-to-analog (DA) interfaces is determinant to the overall system reliability. Examples of works addressing reliability of ADCs against radiation effects and mitigation techniques may be found in [5]–[9]. Some of these works describe neutron and heavy-ion experiments performed on commercial ADCs to evaluate single-event effects (SEEs). However, these experiments are performed without considering any tolerance technique applied to these MS blocks.

The application of a mitigation strategy based on modular redundancy with design diversity to a DAS, prototyped in a programmable system-on-chip (PSoC) device, was proposed by our research group in [8] and [10]. In the above-mentioned works, we performed an extensive fault injection campaign by using a fault injection system based on a pseudorandom number generator implemented in an auxiliary board to select the memory and bit positions to insert the faults and software interruption to perform the bit-flip injection routine [11]. A previous fault injection experiment with a first-generation PSoC device (comprising a simple 8-bit processor) is reported in [12]. In such work, the device was tested without applying any mitigation technique and considering a purely digital application (matrix multiplication).

In this work, we used a device pertaining to the third generation of PSoC family, from Cypress Semiconductor (comprising a 32-bit ARM processor), in a heavy-ion irradiation campaign. The experiments performed in this work are focused on the components of the AD interface of the device. The tested application is a fault-tolerant DAS based on design diversity, comprising three ADCs, besides digital hardware and software resources for controlling the converters and performing the voting tasks. Therefore, this design implements an MS design diversity triple modular redundancy (MS-DTMR) technique [8], [11].

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The main contribution of this article is to evaluate the fault tolerance level of this design diversity-based MS system under SEEs. The application-level consequences of soft errors occurring in the MS interface elements of a system-on-chip are also pointed out in this article. In addition, insights about the reliability implication of using the different architecture of converters, voting schemes, and sampling frequencies are given.

II. Applying Design Diversity Redundancy to MS Interfaces

In a previous work of our research group [8], the application of DTMR to MS circuits was addressed, identifying the possible modes of diversity implementation (time, domain, level, and architecture) and the drawbacks of applying this technique to MS systems.

In this work, we apply the proposed technique to a DAS using the MS interface of the adopted PSoC and test the protected hardware under heavy-ion irradiation. Sections II-A–II-C present, respectively, some background regarding SEEs on ADCs, the basics of the design diversity redundancy technique, and the proposed case study system.

A. SEEs on ADCs

Strongly ionizing particle impacts in sensitive areas of an IC may induce current pulses that can disturb the circuit operation, causing data corruption or permanent device failure. These effects are known as SEEs and may be caused by heavy ions, alpha particles, protons, and neutrons (indirect ionization) [4], [13], [14]. Such events may lead to bit inversion in a memory element resulting in a single-event upset (SEU) [15]. A temporary current pulse induced by an SEE that may propagate into the signal path (either in digital or analog circuits) is known as single-event transient (SET) [16].

The system-level effects of bit inversions in digital systems, caused by SEEs, are also known as soft errors. If the system stops working due to an SEE, the event is classified as a single-event functional interrupt (SEFI). In computing systems, soft errors may lead to incorrect execution of software, generating silent data corruption (SDC), timeout errors, or hang failures.

ADCs present both analog and digital parts that can be disturbed both by SEUs and SETs. SEUs in the registers that store the converted word may lead to high magnitude conversion errors if the most significant bits (MSBs) are flipped. If a control register is affected, such as the ones used to perform calibration, it can lead to lingering or semipermanent errors [6], [9], [17], [18]. Incorrect conversion may be generated also by an SET pulse at the analog part, with a higher probability of producing low magnitude errors, as discussed in [6], [9], and [18].

B. Fault-Tolerance With Design Diversity

Mitigation to soft errors is usually obtained by adding some degree of redundancy, usually hardware or information redundancy. The triple modular redundancy (TMR) technique consists of triplicating the hardware (or part of it) and voting upon the results of the computation done by each TMR copy [19].

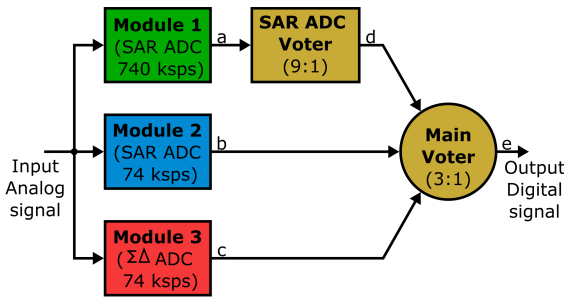


Fig. 1. DTMR DAS architecture.

If the replicated modules are not identical, a DTMR technique is achieved. In this approach, the hardware and software elements used to perform the multiple computations are not copies but are independently designed to meet the system requirements [20]. The main goal of this technique is to avoid multiple errors that may arise due to commonalities among the system copies by using different hardware devices, different clock frequencies, and different software implementations [10].

Examples of the application of design diversity techniques in aircraft from NASA, Airbus and Boeing may be found in [21]–[24]. The assessment of fault tolerance of diversitary architectures in digital and FPGA-based architectures is performed in [25] and [26].

C. Proposed Case Study System

The case study circuit is a redundant DAS, which comprises three 8-bit ADCs operating in parallel: two successive approximation register (SAR) converters and a $\Sigma\Delta$ converter. Besides the hardware diversity implementation, due to different ADC architectures, temporal diversity is achieved due to the different sampling rates of the SAR ADCs (740 and 74 ksamples/s). The system also comprises two software-based voters: one main spatial voter and a temporal voter, which also performs the coarse synchronization of the DAS. The simplified block diagram of the case study circuit is depicted in Fig. 1. Implementation details are given in Section III.

III. Experimental Setup

A. System Implementation Details

The redundant DAS, was implemented in a commercial PSoC (PSoC 5LP from Cypress Semiconductor) manufactured in 130-nm CMOS technology.

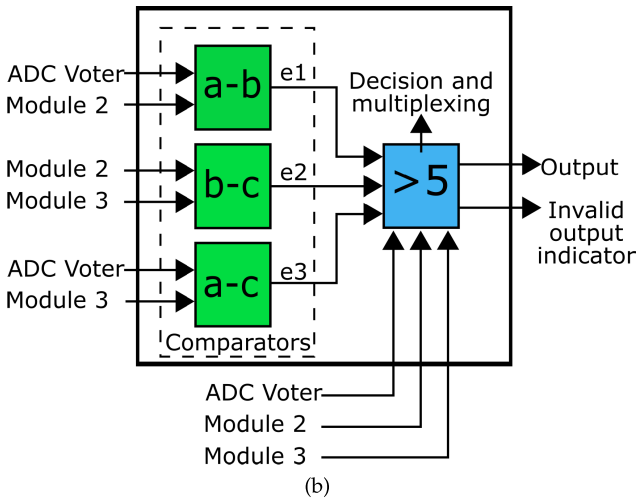
The PSoC has a 32-bit ARM Cortex-M3 CPU (up to 80 MHz), 256 kB of flash memory, 64 kB of SRAM memory, 2 kB of EEPROM memory, and 24 channels of direct memory access (DMA). The device also comprises digital peripherals, such as communication interfaces and programmable logic devices (PLDs), based on universal digital blocks (UDBs), which provides the implementation of various functions, such as timers and counters. In addition, analog peripherals, such as a sigma–delta ($\Sigma\Delta$) AD converter, two SAR converters,

```
void main_voter()
{
    error1 = abs (SAR_ADC_voter_data - module2Data[1]);
    error2 = abs (module2Data[1] - module3Data[1]);
    error3 = abs (module3Data[1] - SAR_ADC_voter_data);

        if (error1 <= 5)
            system_output = SAR_ADC_voter_data;
        else if (error2 <= 5)
            system_output = module2Data[1];
        else if (error3 <= 5)
            system_output = module3Data[1];
        else
            system_output = SAR_ADC_voter_data;

        if ((error1 > 5) || (error2 > 5) || (error3 > 5))
            main_voter_error_det = 1;
}
```

(a)

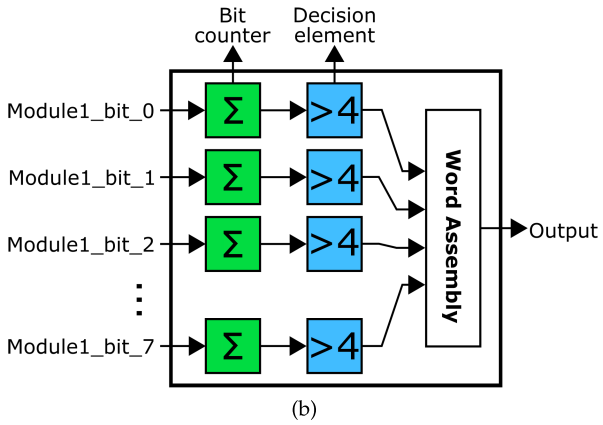


(b)

Fig. 2. (a) Software code of the main voter. (b) Voter block diagram.

```
void SAR_ADC_voter_data
{
    bits = 0;
    SAR_ADC_voter_data = 0;
    for (i = 0; i < 8; i++) bit_counter[i] = 0;
    for (i = 0; i < 8; i++)
    {   for (j = 1;j < 10; j++)
        {  bits = (module1Data[j] & mask[i]) != 0;
        // mask is an aray of bytes previosly defined:
        // mask[8] = {128, 64, 32, 16, 8, 4, 2, 1}
            if (bits == 1)
                bit_counter[i] = bit_counter[i] + 1;
        }
    }
    for (i = 0; i < 8; i++)
    {       if (bit_counter[i] > 4)
            SAR_ADC_voter_data = SAR_ADC_voter_data + mask[i];
    }
}
```

(a)



(b)

Fig. 3. (a) Software code of the temporal bit-by-bit voter at the output of the SAR ADC operating at 740 ksamples/s and (b) its block diagram.

DA converters, comparators, operational amplifiers, and configurable analog blocks, may also be used to implement several analog functions [27].

The main voter of the redundant DAS is based on the concept of word voting [28], performing mutual subtractions between the converted signals, and generating three error signals that allow to select a healthy block to drive the system output. The part of the code that implements the main voter is shown in Fig. 2(a) along with the voter block diagram in Fig. 2(b). Voting upon analog converted signals cannot be done by exact comparison, as in digital voting schemes. Thus, a tolerance window is considered, as shown in Fig. 2. If a signal is faulty, two of the error signals will deviate from the ideal value (zero), and if this error is higher than the tolerance window (5, in this case), the decision element identifies the faulty signal, switching one of the healthy modules to the output.

The SAR ADC temporal voter was implemented using the bit-by-bit voting technique, which is easier to implement when there are many inputs [28]. This technique was chosen because the voting is done upon nine samples (one of the ten samples generated by the faster SAR, within the main voting cycle, is discarded, to avoid a possible tie). For each bit position, the output word is built with the majority of bit values observed at the same position in the nine voted samples. The part of the software implementing this voter is depicted in Fig. 3(a), while Fig. 3(b) shows the voter block diagram. As one will see in Section IV, this choice will have an impact on the reliability level of each voter to SEEs.

In addition to the ADCs and voters, the implemented system also comprises three sample-and-hold blocks, three channels of DMA, and a synchronizer block, needed to accurately synchronize the voting cycles, since the conversion times are different for each converter. In addition, a status register (composed of five circular buffers) is used to continuously monitor the output of the three ADCs and both voters, sending its content to an external computer (by means of a UART-RS232 interface) whenever a fault is detected by the voters. After sending the content of the buffers, the system is reset, reprogramming it in a way that the error is corrected. The size of each buffer was defined in order to store two complete cycles of the test signal (one before and another after the error detection). Due to the time needed to buffer and send the data, a practical "undersampling" is performed, in such a way that the equivalent sampling rate sent through the serial interface is 6720 samples/s, though the converters operate at higher sampling rates.

A signal generator block (composed of an 8-bit DAC) was programed into the PSoC, generating a 120-Hz triangular wave, swinging among the full-scale limits of the converters (0–2 V), in order to serve as input test signal of all ADCs. Fig. 4 shows the overall block diagram of the system implemented in the device under test (DUT).

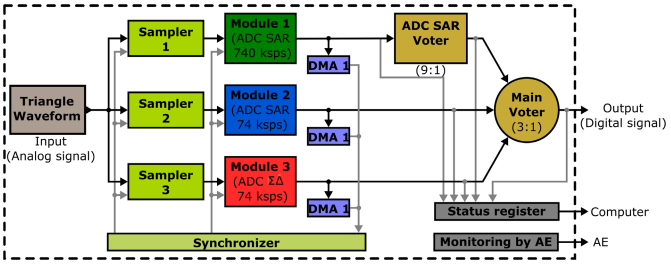


Fig. 4. Details of the full implementation of the DAS in the PSoC device with an internal test signal.

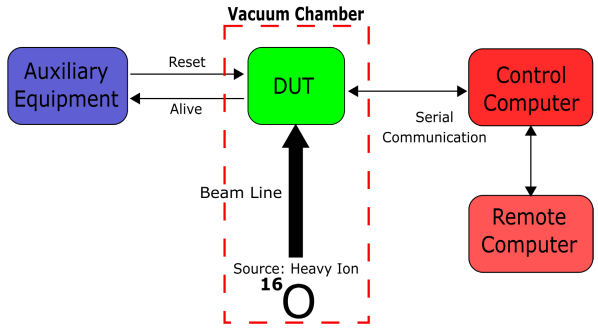


Fig. 5. Experimental setup.

In order to cope with hangs in the overall system, a secondary board is used as a watchdog, which monitors an "alive" signal sent by the DUT. If this signal remains inactive for more than 30 s, this auxiliary board resets the DUT.

B. Heavy-Ion Irradiation

A heavy-ion irradiation experiment was performed at the Laboratório Aberto de Física Nuclear, Universidade de São Paulo (LAFN-USP), Brazil [29], with ion beams produced and accelerated by the São Paulo 8UD Pelletron Accelerator.

The experiment was performed in a vacuum (see Fig. 5), using a ^{16}O ion beam with 36-MeV energy and 22 μm penetration into the silicon. The DUT (with the top package removed) was irradiated at 0° angle, producing an effective linear energy transfer (LET) at the active region of 5.5 MeV/mg/cm^2 with an average flux of approximately 350 particles/s/cm^2. The DUT was irradiated during 246 min, resulting in a fluence of 5.08×10^6 particles/cm^2. The experiment was performed following the ESA/ECC Basic Specification no. 25100 [30].

IV. Experimental Results and Discussion

A. Functional Errors in the Converters

Two well-known system-level effects of SEEs in computing systems are SEFI and SDC. When considering MS systems in which the analog function may be assisted by digital circuits and configured by means of control registers, a deviation on a given register value may affect the "analog" behavior of the system. For this reason, a new system-level error classification is needed. We then propose to use the term "single-event functional deviation" (SEFD) to classify the conditions in

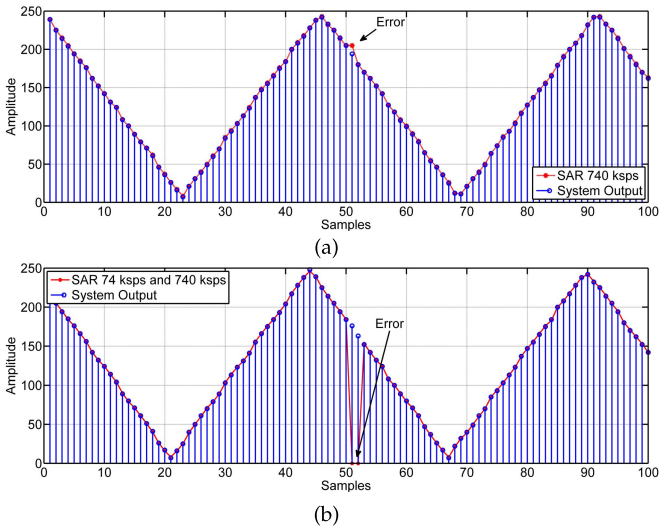


Fig. 6. Examples of SDCs in the SAR @740 ksamples/s module. (a) Small and (b) high magnitude errors.

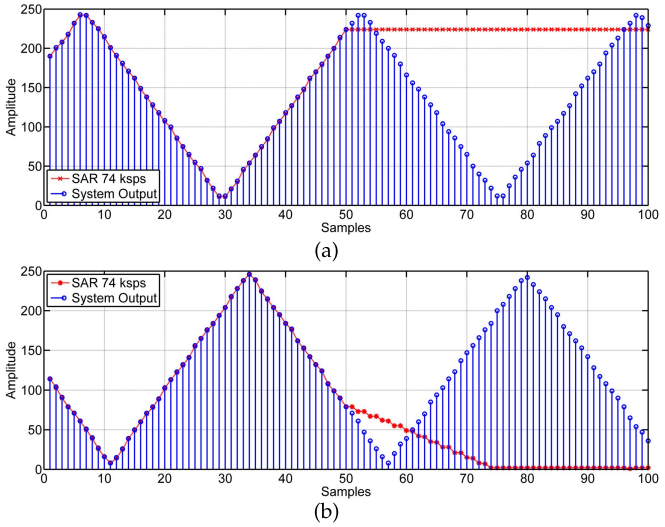


Fig. 7. Examples of SEFIs in the SAR @74-ksamples/s module. (a) Stuck at current sample. (b) Decay to zero.

which a "semipermanent" or lingering error [6], [17], [18] is caused by a single event, in such a way that the system is still operating similar to the nominal case but with a deviated output.

While examples of SDCs in the converters are given in Fig. 6 and SEFI examples are shown in Fig. 7, SEFD examples may be observed in Fig. 8. The SDCs may be related to an error in a data register of the converter or in the memory position in which the current sample is stored (before the voting is completed), while SEFI and SEFD in the converters may be associated with control registers and auxiliary control circuits used to assist the analog part of the converters.

All errors shown in Figs. 6–9 were recorded during the heavy-ion irradiation. The reason for the error to appear always in the sample number 51 in the figures is due to the adopted continuous buffering strategy, which is able to store 50 samples before and 50 after the error occurrence.

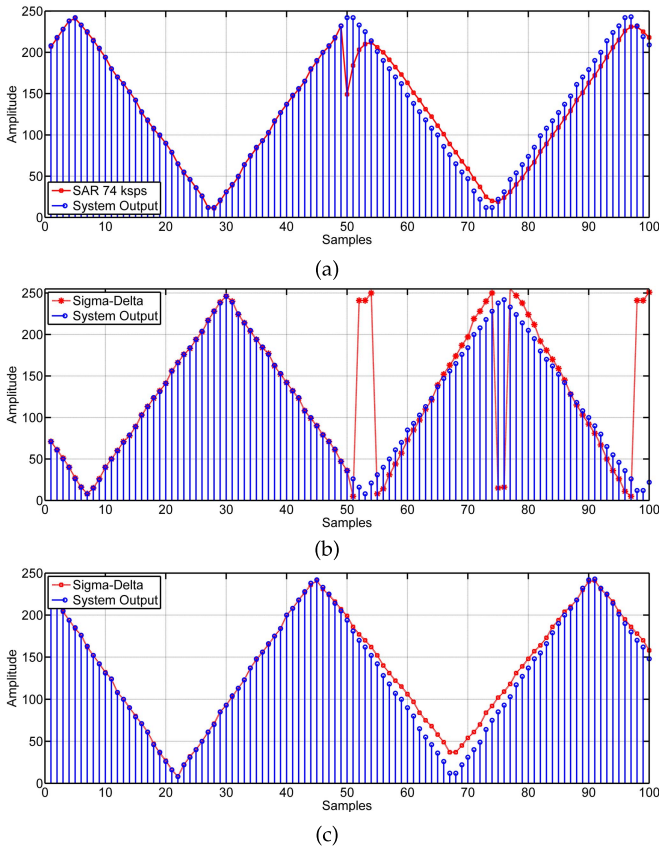


Fig. 8. (a) Examples of SEFDs in the SAR @74 ksamples/s. (b) and (c) Sigma–Delta modules.

Errors were also observed in the SAR ADC temporal voter (as depicted in Fig. 9) even when no error occurred at the nine voted samples originated by the SAR @740-ksamples/s module. On the other hand, no error was observed in the main voter, which means that 100% of the observed SDC/SEFI/SEFD occurring in the converters was tolerated by the proposed system, as shown in Figs. 6–8 (quantification details are given Section IV-B).

The reason for the temporal voting being less reliable than the spatial one is the increased complexity of the former. As there are too many inputs and the bit-by-bit voting technique is applied, this voter relies on using several loops and iterations [as depicted in Fig. 3(a)]. Errors in registers of the loop control variables and in the previously stored mask variable, besides the higher time needed to perform this voting, may be the causes of this behavior. Current works are being directed to evaluate the reliability of different software- and hardware-based voting schemes to be employed as temporal voters in this system.

Fig. 10 shows the observed magnitude errors on the output words of the converters and temporal voter, considering the first subsequent sample after an error detection. (SEFIs are not considered in this figure.) It can be seen that most of the high magnitude errors (whose amplitude difference is $>10\%$ of the full scale) occurred in the temporal voter (ADC voter). Most of the errors observed in the converters are small magnitude deviations, suggesting that a significant number

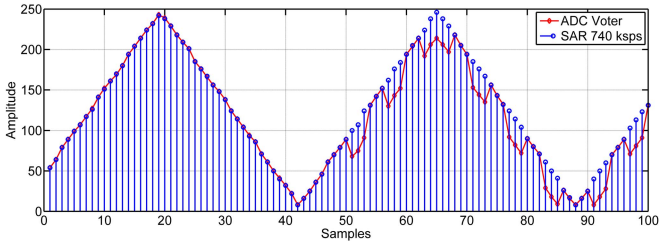


Fig. 9. SEFD in the temporal voter.

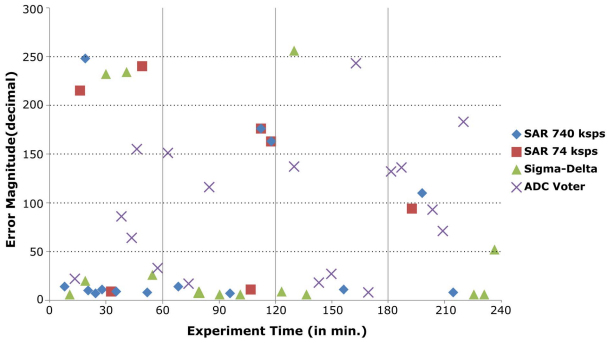


Fig. 10. Magnitude of errors observed in the converters and temporal voter.

of errors originated at the analog part of the converters (in accordance with the results of [6], [9], and [18]). Actually, two errors in the $\Sigma\Delta$ converter generated values that are much higher than the maximum allowed word (255) and are not shown in the plot.

B. Hang Failures and Cross-Section Calculation

The DAS under study is prototyped in a microprocessor-based programmable SoC with the voting and processing performed by software. This way, the fault-free condition of the overall system depends also on the processor correct functioning. Besides the above-described errors in the converters, system-level SEFIs, from here on called *hangs*, were also observed.

During the experiment time, 139 errors were observed. From these errors, 82 are system hangs, and 57 are SDC, SEFI, or SEFD at the converters. Most of the hangs (53) were detected by the external watchdog, and the system was automatically reset. The other 29 hangs were detected and treated manually. For this reason, we classified these errors as critical hangs. We can explain this behavior because, in this experiment, the alive signal sent by the DUT is generated by a clock generator from the hardware peripherals of the PSoC that may still be functional even if the program is not running normally. If we consider interaction of the main program with the watchdog timer, it is expected that these critical hangs can be also treated accordingly.

With the experiment time, ion flux, and recorded errors, we are able to calculate the dynamic cross section of the system, as well as the individual cross section of each converter lane (as depicted in Fig. 11).

Table I summarizes the calculated cross section for each case, which can be also individually calculated for the different

TABLE I

DYNAMIC CROSS SECTION OF THE WHOLE SYSTEM AND INDIVIDUAL CONVERTERS

System Cross Section (cm^2)	
Total	$(4.06 \pm 0.35) \times 10^{-5}$
SDC/SEFI/SEFD (converters)	$(1.66 \pm 0.23) \times 10^{-5}$
System hangs (processor)	$(2.40 \pm 0.31) \times 10^{-5}$
Converters Cross Section (cm^2)	
SAR @740 ksps	$(3.51 \pm 1.11) \times 10^{-6}$
SAR @74 ksps	$(1.75 \pm 0.71) \times 10^{-6}$
$\Sigma\Delta$	$(4.09 \pm 1.09) \times 10^{-6}$

TABLE II

SUMMARY OF ERROR OCCURRENCE RESULTS AT THE DAS

Total Events	(139 ± 12)	**100%**
Hangs	(53 ± 7)	38%
Critical Errors	(29 ± 5)	21%
SDC/SEFI/SEFD (converters)	(57 ± 8)	41%
SAR @740 ksps	(12 ± 3)	9%
SAR @74 ksps	(6 ± 2)	4%
$\Sigma\Delta$ Converter	(14 ± 4)	10%
Temporal Voter	(18 ± 4)	13%
Main voter	0	0%
Unknown errors	(7 ± 2)	5%

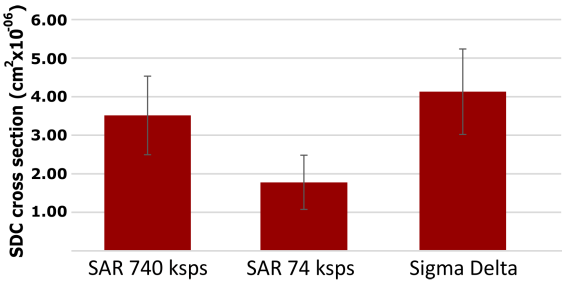


Fig. 11. Dynamic cross section results for the converters, considering SDC, SEFI, and SEFD errors.

error nature (hangs and SDC/SEFI/SEFD). To calculate the cross sections, the uncertainties were calculated considering a Poisson distribution for the error occurrence. Table II summarizes the number and percent of errors according to the affected system part, along with the uncertainties [where (139 ± 12) means uncertainty of 12 in a total of 139 errors, for instance]. The unknown errors are errors that triggered the data transmission from the DUT to the computer but were not identified in the postexperiment analysis (no observed signal deviation). These errors may be related to malfunction of the serial communication interface and bit inversions in the error flag of the voters. Actually, some other communication errors were identified, with garbage data sent through the serial channel. These errors were not computed to generate the cross-section data presented in this article.

Fig. 11 shows a different dynamic cross section for each converter, including those that present exactly the same architecture (SAR converters). The converters cross section considers errors originated due to SETs at the analog part, SEUs at the digital part of the converters, as well as bit flips in the configuration SRAM memory, in bits that are used to program the MS peripherals.

C. Influence of Diversity on Converters Reliability

As expected, the converter operating with an increased sampling rate presented a higher dynamic cross section than its slower counterpart. This is because the higher clock frequency increases the probability of capturing a transient disturbance on the voltage under comparison in the SAR capacitive array, as demonstrated in [9]. In addition, in this oversampled lane, ten samples are stored in the memory in each voting cycle, while a single sample is produced by the slower converters, increasing the probability of an SEU at the stored values, before the data are voted.

Concerning the different architectures operating at the same sampling frequency (SAR and $\Sigma\Delta$), the higher cross section of the $\Sigma\Delta$ converter is due to its complexity since it comprises a third-order modulator (composed of a loop of cascaded integrators), a summing amplifier, a quantizer, and a switched-capacitor DAC, besides a digital decimation (downsampler) and low-pass (averaging) filter [27]. On the other hand, the SAR main blocks are a capacitive DAC, a comparator, and simple digital logic to control the capacitor array by means of a set of analog switches.

Finally, the reliability of each module may be improved by applying design-level techniques if the converters are being designed as part of an application-specific IC (ASIC), for example. As demonstrated in [9], by increasing the capacitance values of the programmable capacitor array (PCA) of SAR converters, as well as the size of the gates that directly control the switches of the PCA, the soft error rate may be reduced with the expense of silicon area. In addition, the digital resources of the converter can be triplicated in a traditional local TMR approach. The latter strategy applies also to the digital part of the $\Sigma\Delta$, namely, the digital filter and decimator blocks.

V. CONCLUSION

In this article, an MS-DTMR system was evaluated under SEEs. The system is composed of three ADCs, comprising different architectures and sampling rates, along with a synchronizing and voting scheme, implementing hardware, and temporal diversity redundancy. The MS-DTMR case study design was prototyped in a commercial PSoC.

Considering the converters operating at the same sampling frequency, the $\Sigma\Delta$ showed a cross section significantly higher than the charge redistribution SAR, given to its increased complexity. When comparing the same architecture (SAR), the dynamic cross section of the copy that operates at higher sampling frequency is also higher, as expected, but still lower than the cross section observed for the $\Sigma\Delta$ converter with lower sampling rate.

The application of the DTMR technique to the AD interface of the PSoC device showed effective to tolerate 100% of the errors originated in the converters. However, the temporal voter at the output of the faster SAR converter showed to be very sensitive to SEEs, especially if compared with the main voter. The main reasons are the relative complexity of the used technique (bit-by-bit voting) and the higher required voting time of this voter. Despite this fact, in all occurrences,

the main voter was able to correct the error originated by the SAR voter. In current studies, different voting schemes are being investigated to replace the SAR voter in order to increase the overall system reliability.

Finally, the overall system is also prone to hangs due to errors in the processor. These errors may be mitigated with existing watchdog methods, besides other techniques usually employed to cope with soft errors in control path elements of processors, when applicable.

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