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Three-phase four-wire unified power quality conditioner structure with independent grid current control and reduced dc-bus voltage operating with inverted/dual compensating strategy

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Summary

This work proposes a 3-phase 4-wire unified power quality conditioner (UPQC) structure, which has ability to operate with per-phase independent grid current control, reduced dc-bus voltage and inverted/dual compensation strategy. Since the grid currents are controlled by the series converter, two distinct strategies, namely, independent current compensation strategy (ICCS) and load unbalance compensation strategy (LUnCS) can be employed. Using the ICCS, the controls of the grid currents are performed independently per-phase, such that the UPQC can operate even when grid voltage outage occurs in one or two phases of the power source. Furthermore, to guarantee the proper parallel converter operation, the dc-bus voltage amplitude must be higher than the grid voltage peak amplitude. Thus, since the parallel converter operation is assured, the functioning of the series converter is also guaranteed because it needs lower dc-bus amplitude to operate. However, depending on the converter topology adopted in the parallel converter, the series converter could be subjected to operate with dc-bus voltage higher than necessary. Thus, to minimize this aspect, this paper proposes a UPQC scheme composed of 3-Leg split-capacitor (3-Leg-SC) and 4-Leg topologies, operating as series and parallel converters, respectively. Thus, besides the use of the ICCS, lower dc-bus voltage is allowed when compared to the UPQC composed of two 3-Leg-SC converters, as well as reduced power switches number is achieved when the propose scheme is compared to UPQC composed of two 4-Leg converters. Extended experimental results based on digital signal controller are presented to evaluate the effectiveness and performance of the proposed UPQC.

KEYWORDS

active power-line conditioning, dc-bus voltage, dual/inverted compensation strategy, independent grid current control, UPQC

Abbreviations: UPQC, unified power quality conditioner; ICCS, independent current compensation strategy; LUnCS, load unbalance compensation strategy; SC, split-capacitor; PQ, power quality; 3P4W, three-phase four-wire; P-APF, parallel active power filter; S-APF, series active power filter; SRF, synchronous reference frame; PLL, phase-locked Loop; SFG, signal flow graph; TF, transfer function; PWM, pulse width modulation; DSC, digital signal controller; PI, proportional-integral; THD, total harmonic distortion; PM, phase margin; IGBT, insulated gate bipolar transitor.

1 | INTRODUCTION

Nowadays, efforts for the improvement of the power quality (PQ) have really grown a lot, mainly due to extensive use of sensible/critical loads. On the other wise, the increasing use of unbalanced and nonlinear loads connected to the electrical power system has contributed to worsen the PQ indicators as line utilization (power factor), load unbalance and harmonic pollution.[1] This happens due to the interaction between the distorted or unbalanced currents drained from the utility grid and the line impedance, which causes utility voltage deterioration and, hence, affects the PQ provided to consumers connected at a point of common coupling. In addition, problems of PQ, as voltage sags/swells can also interfere in the adequate functioning of sensible equipment.

To overcome the most problems related to PQ, single-phase[2] and three-phase series-parallel active power-line conditioners,[3-20] known as unified power quality conditioners (UPQC), have been employed in there-phase three- and four-wire systems (3P3W and 3P4W) by means of different configurations and control strategies.

Usually UPQC topologies applied 3P4W systems are composed of either three-leg split-capacitor (3-Leg-SC)[14,15] or four-leg (4-Leg) converter topologies[16-18] performing the parallel and the series conditioning. The main drawback of the 3-Leg-SC inverter topology, which uses two capacitors in the dc-bus, is associated to its higher dc-bus voltage level when compared to the four-leg (4-Leg) topology. Although higher number of power switches is needed, the 4-Leg topology operates with lower dc-bus voltage. In addition, better controllability for compensating the neutral current by using the additional forth leg is assured.[21,22] Another UPQC topology using two back-to-back 3-Leg converters operating with reduced dc-bus voltage was proposed in Reference 12, where it was performed by introducing capacitors in series with the interfacing inductors of the parallel converter. Although the purpose of reducing the dc-bus voltage has been reached, the use of the series capacitors makes the topology dependent on suitable choice/adjustment of the capacitors. In other words, the previous knowledge of the load characteristics is needed to assure the proper design of the series capacitors, and consequently an adequate operation of the UPQC, since the series capacitors designing will determine how much voltage level will be reduced in the dc-bus. This happens because such capacitors will also provide part of the load demanded reactive power. Therefore, the interdependence between the dc-bus voltage decreasing and the amount of reactive power provided to the load represents a drawback.

This paper proposes an UPQC topology, which is composed of a 4-Leg inverter acting as parallel active power filter (P-APF) and a 3-Leg-SC inverter working as series active power filter (S-APF). The mentioned UPQC configuration become attractive to be used in 3-phase 4-wire systems because the dc-bus voltage amplitude required to assure the series converter operation can always be set lower than the voltage amplitude required to ensure the parallel converter operation. Furthermore, the maximum dc-bus voltage amplitude is always determined by the parallel converter and, hence, in theory, the minimum voltage level needs to be higher than the line-to-line power supply voltage peak amplitude ($V_{dc} \geq \sqrt{2} V_{rms(L-L)}$). As a result, this dc-bus voltage level is enough high to guarantee properly the operation of the S-APF prevent oversizing in the voltage rate. Thus, the proposed UPQC requires lower dc-bus voltage when compared to the UPQC that uses two 3-Leg-SC topologies,[14,15] and requires reduced number of power switches when compared to the UPQC the uses two 4-Leg topologies.[16-18]

For control purposes, conventional strategies of power-line compensating usually use non-sinusoidal voltage/current references to control both voltages and currents of the series and the parallel converters.[3,23] In this paper, the dual/inverted compensating strategy is adopted to control the parallel converter for acting as a sinusoidal voltage source and the series converter for working as a sinusoidal current source.[13,15,16,19,20] As a consequence, the complexity of the reference generation algorithms is reduced due to the sinusoidal control references can be achieved more easily.[20]

To control the output voltages of the UPQC, the controllers based on synchronous rotating frame (SRF) (*dq0*-axes) are used. While the generation of the series current references is obtained in the SRF, in this paper, the current controllers operate in the 3-phase stationary frame (*abc*-axes). A phase-locked loop (PLL) system is also used to calculate the unit vector ($\sin\theta$ and $\cos\theta$) coordinates used in the SRF.

In Reference 19, 3-Leg and 4-Leg converters have been used to perform, respectively, the S-APF and the P-APF of the UPQC. Taken into account the difficulty associated to the control, 3-Leg-SC inverter is relatively easier to control than the 3-Leg inverter due to each leg is a half-bridge inverter and the single-phase decoupled currents go through the semiconductor devices. On the other hand, in conventional applications, it is well-known that the 3-Leg-SC inverter dc-bus voltage of is higher than those found in either 3-Leg or 4-Leg inverters.

In this paper, although the 3-Leg-SC inverter configuration is adopted to operate as S-APF (series converter), the dc-bus voltage amplitude is not higher than that used in the 3-Leg inverter presented in Reference 19. Furthermore, employing the 3-Leg-SC inverter to operate as S-APF allows independent control of the grid currents, as well as

contributes to make the current control simpler. In addition, two different compensating strategies are employed and experimentally tested in this paper. The first, called independent current compensation strategy (ICCS), allows that the grid currents be independently controlled, such as reactive power compensation and harmonic current suppression of the load can be performed. In other words, the 3P4W S-APF can be considered as three single-phase S-APFs operating independently per phase. As advantage, since the grid currents are being independently controlled, the UPQC can operate properly even when voltage outage occurs in one or two of the three phases of the grid voltage. It must be emphasized that a single-phase PLL system[24] must be used in each phase to ensure the proper ICCS operation. The second implemented strategy is named load unbalance compensation strategy (LUnCS). Different from the ICCS, this strategy includes also the compensation of the fundamental negative sequence components present in the load currents, so that balanced and sinusoidal grid currents are achieved. In the LUnCS, a three-phase PLL system proposed in Reference 25, 26 is employed.

It can be noted that the proposed UPQC topology is new in the literature due to it is built using a 3-Leg-SC inverter operating as series converter and a 4-Leg inverter operating as parallel converter. Thus, the main contribution of this paper is the deployment and performance evaluation of a 3P4W UPQC structure with ability to operate with per-phase independent grid current control, reduced dc-bus voltage and inverted/dual power-line compensation strategy. It can also be highlighted that the independent grid current control is only possible if the 3-Leg-SC converter is used as series converter. In addition, will be shown that the UPQC can operate normally even in occurrence of voltage outage that can occur in one of the three phases of the grid.

2 | PROPOSED UPQC TOPOLOGY DESCRIPTION

The proposed UPQC topology highlighting its main operation aspects are presented in this section, where it is compared to other two UPQC topologies used in 3P4W systems.

Figure 1 presents the UPQC topology studied in this paper, where two back-to-back converters are connected to a same dc-bus voltage. A 4-Leg converter is implemented to operate as P-APF,[26,27] while the 3-Leg-SC converter is implemented to act as S-APF.

The harmonic components of the load will circulate through in the parallel converter since it is controlled to work as a sinusoidal voltage source and represents a way of low impedance to these currents. On the other wise, the S-APF represents high impedance way for blocking the load harmonic currents since it is controlled to work as a sinusoidal current source.

The 4-Leg converter was chosen to implemented the P-APF based on the following aspects: (a) operating with reduced dc-bus voltage ($V_{dc} = \sqrt{2}V_{rms(L-L)}$), when compared to the 3-Leg-SC inverter ($V_{dc} = 2\sqrt{2}V_{rms(L-N)}$), representing reduction on the dc-bus voltage level; (b) the neutral current of the load always flows through the 4-Leg converter (fourth leg) reducing the voltage oscillation of the dc-bus when compared to the 3-Leg-SC inverter; (c) since

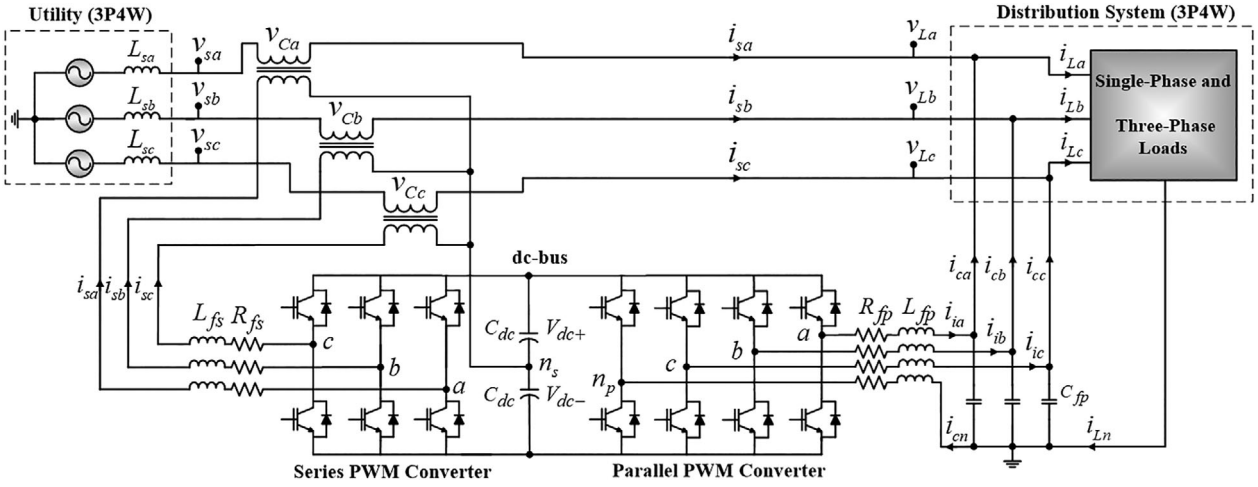

FIGURE 1 Proposed 3P4W UPQC topology composed of 3-Leg-SC and 4-Leg inverters

the current amplitude that flows through the neutral conductor is normally low, reducing the switches power rating of the fourth leg. Compared to the 3-Leg-SC structure, this minimizes the drawback to use an additional inverter leg. On the other hand, the 3-Leg-SC topology was chosen to implement the S-APF based on the following aspects: (a) operation with reduced dc-bus voltage ($V_{dc}/2 = \sqrt{2}V_{rms(L-L)}/2$), allowing the reduction of the series converter over voltage rating; (b) possibility of implementation of both the strategies ICCS and LUnCS; (c) reduced number of switches when compared to the 4-Leg converter.

2.1 | Dual compensation principle

Non-sinusoidal currents and voltages references have been used to control the most UPQC applications.[2-10] Therefore, it is indicated to employ any method for extraction the reference quantities.[2-5]

On the other side, in this paper, a dual compensating strategy[13,14,19] is employed for compensating both grid currents (series converter) and load voltages (parallel converter) by means of sinusoidal references. Thereby, once the compensating references are sinusoidal quantities it is not necessary to use any method to extract such references,[14] simplifying the reference generation algorithms.

In the dual/inverted power-line UPQC compensation strategy the series converter is controlled as a three-phase sinusoidal current source, where the controlled currents are in phase with the respective utility voltages. Thus, since the input currents are sinusoidal, the reactive power is compensated, as well as the load harmonic contents are suppressed. As a result, high power factor is achieved. It can be highlighted that the high impedance path created by the series converter will force the load harmonic currents to flow through the parallel converter which in turn is controlled as a sinusoidal voltage source and must have a low impedance path.

Since the parallel converter is controlled as a sinusoidal voltage source, sinusoidal, balanced, and regulated voltages are provided to the load. In the adopted control strategy, the load voltages are also controlled to be in phase with the utility voltages. As a result, the series converter absorbs from the grid or furnishes to the grid only active power necessary to maintain the UPQC power balance when grid voltage amplitude variations occur (voltage sags/swell). In addition, the low impedance path created by the sinusoidal voltage-controlled parallel converter contributes to the load harmonic currents flow through the parallel converter.

It can be noted that the parallel converter synthetizes only sinusoidal and balanced voltages. Thus, the grid disturbances as voltage sags/swells, voltage harmonics, voltage unbalances, and flickers will emerge at the terminals of the series coupling transformers. Thereby, these disturbances are mitigated since they are indirectly compensated by the series converter. As a result, there is no need to generate non-sinusoidal reference voltages that represent these disturbances. It can be noted that the sinusoidal output voltage references must have constant amplitudes and their grid phase-angle estimation is achieved using a PLL scheme.

3 | ALGORITHMS FOR GENERATION THE UPQC CONTROL REFERENCES

In this section are discussed the strategies employed to create the references of voltage and current of the proposed UPQC. The SRF-based algorithm is employed to create series references of current, while SRF-based controllers are used in the voltage control loops applied to the parallel converter (v_{La}, v_{Lb}, v_{Lc}).

As the SRF-based controller is used to control the load output voltages, the reference voltage in the direct axis d can be set as a continuous value (v^*_{Ld}). On the other hand, since balanced and sinusoidal output voltages are desirable, the voltage in q-axis $\left(v^*_{Lq}\right)$ and v^*_{L0} are set to zero in the control loops. Details of this algorithm are presented in Reference 19.

To generate the series converter current references, two algorithms are employed in this paper. In the first algorithm (ICCS), the grid currents are controlled by means of three per phase current controllers acting on the half-bridge converters. Although the three-phase grid currents can be unbalanced, depending on the load characteristics, they will be always sinusoidal. In this case, both load harmonic currents and reactive power will be compensated, except the fundamental sequence components of the load (negative, zero or both). The second algorithm (LUnCS) includes the load unbalances compensation, so that the input currents will become always sinusoidal and balanced.

3.1 | ICCS algorithm

The ICCS is presented in Figure 2A. It allows treating the three-phase system as three independent single-phase systems. As can be noted, three fictitious three-phase systems which are represented in the stationary reference frame ($\alpha\beta$-axes) must be created in order to obtain the series reference currents ($i^*_{sa}, i^*_{sb}, i^*_{sc}$). For this purpose, each individual load current ($i_{La} = i_{\alpha a}$, $i_{Lb} = i_{\alpha b}$, $i_{Lc} = i_{\alpha c}$) is measured and, after that, it is introduced a phase-delay of $\pi/2$ radians in each of them. Thus, the quadrature currents ($i_{\beta a}$, $i_{\beta b}$, $i_{\beta c}$) are generated and, hence, three fictitious three-phase stationary reference frames are obtained. After that, the direct currents (i_{da}, i_{db}, i_{dc}), are achieved into the SRF (dq-axes) as given by

$$\begin{bmatrix} i_{da} \\ i_{db} \\ i_{dc} \end{bmatrix} = \begin{bmatrix} cos\theta_a & sin\theta_a & 0 & 0 & 0 & 0 \\ 0 & 0 & cos\theta_b & sin\theta_b & 0 & 0 \\ 0 & 0 & 0 & 0 & cos\theta_c & sin\theta_c \end{bmatrix} \begin{bmatrix} i_{\alpha a} \\ i_{\beta a} \\ i_{\alpha b} \\ i_{\beta b} \\ i_{\alpha c} \\ i_{\beta c} \end{bmatrix}. \quad (1)$$

Now, by using low-pass filters (LPFs), the currents (i_{da}, i_{db}, i_{dc}) obtained from Equation (1) are filtered to achieve the currents $i_{d_{dc\_a}}$, $i_{d_{dc\_b}}$, and $i_{d_{dc\_c}}$, which represent the active components of the load currents (i_{La}, i_{Lb}, i_{Lc}).

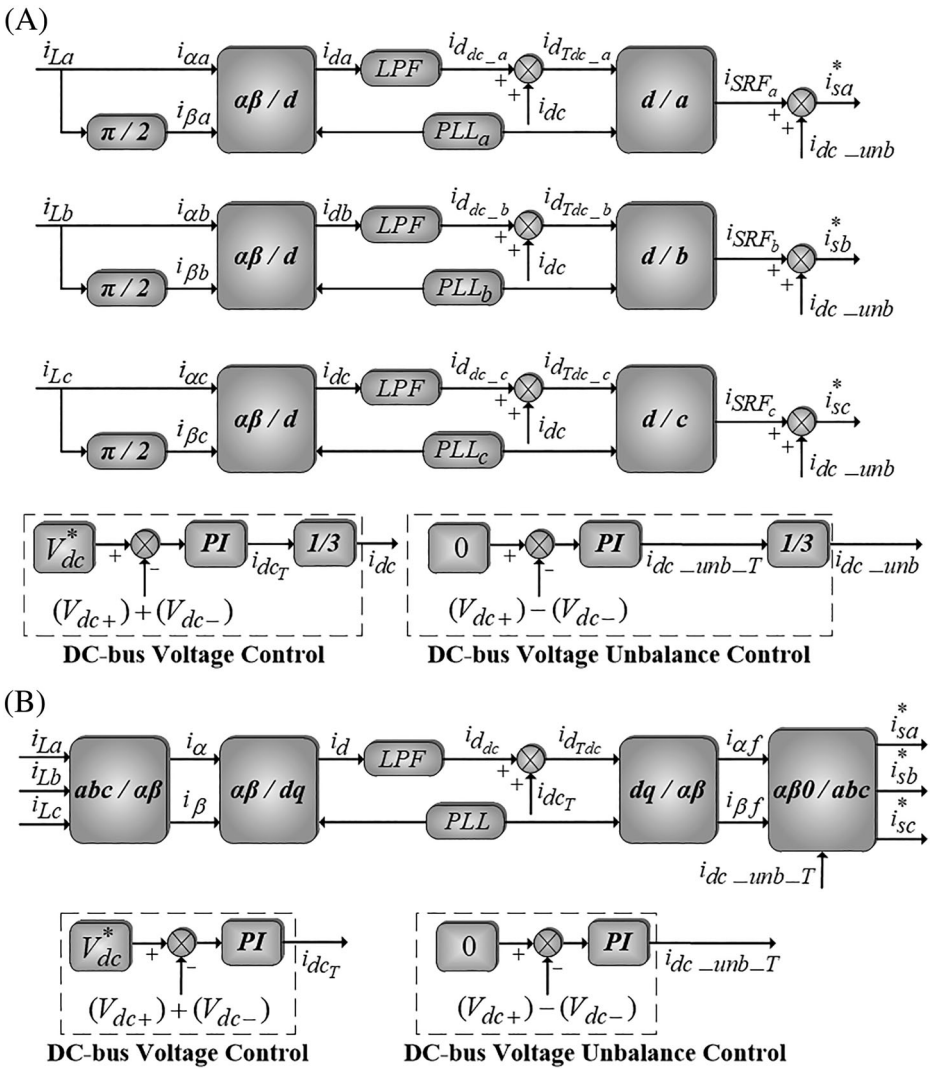

FIGURE 2 SRF-based algorithms: (A) independent current compensation strategy (ICCS); (B) load unbalance compensation strategy (LUnCS)

As can be seen in Figure 2A, the output signal of the DC-bus voltage controller (i_{dc_T}) is divided in three parts resulting the current i_{dc}. After that, i_{dc} is added to the respective direct currents $i_{d_{dc\_a,b,c}}$ due to the need of sharing, among the three phases, the task of regulating the dc-bus voltage in order to compensate the losses associated to passive elements and switches. Furthermore, i_{dc_T} provides the power balance through the UPQC dc-bus, when amplitude deviations between the input voltages (v_{sa}, v_{sb}, v_{sc}) and the output voltages (v_{La}, v_{Lb}, v_{Lc}) occur.

As can be noted in Figure 2A, an additional PI controller controls the dc-bus voltage unbalance by measuring the difference of the voltages V_{dc+} and V_{dc-} and comparing them to zero. Thus, dc-bus voltage unbalance controller output, which is represented by i_{dc_unb}, is added to the SRF outputs ($i_{SRF_a}, i_{SRF_b}, i_{SRF_c}$) resulting in the series current references ($i^*_{sa}, i^*_{sb}, i^*_{sc}$), as given by

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \begin{bmatrix} cos\theta_a & 0 & 0 \\ 0 & cos\theta_b & 0 \\ 0 & 0 & cos\theta_c \end{bmatrix} \begin{bmatrix} i_{d_{dc\_a}} + i_{dc} \\ i_{d_{dc\_b}} + i_{dc} \\ i_{d_{dc\_c}} + i_{dc} \end{bmatrix} + \begin{bmatrix} i_{dc\_unb} \\ i_{dc\_unb} \\ i_{dc\_unb} \end{bmatrix}. \tag{2}$$

3.2 | LUnCS algorithm

The controllers based on SRF are employed used to create the 3-phase compensation current references ($i^*_{sa}, i^*_{sa}, i^*_{sa}$) for the LUnCS, as shown in Figure 2B. In this case, balanced and sinusoidal compensated grid currents are obtained. In the referred algorithm, only an LPF is needed to extract the direct current $i_{d_{dc}}$, which depicts the total load currents fundamental active components. Therefore, the currents involved in the algorithm presented in Figure 2B are given by Equations (3)–(6), as follows:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}, \tag{3}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \tag{4}$$

$$\begin{bmatrix} i_{\alpha f} \\ i_{\beta f} \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} i_{d_{dc}} + i_{dc_T} \\ 0 \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} i_{d_{Tdc}} \\ 0 \end{bmatrix}, \tag{5}$$

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{\alpha f} \\ i_{\beta f} \\ i_{dc\_unb\_T} \end{bmatrix}. \tag{6}$$

It can be seen in Figure 2B, the currents i_{dc_T} and $i_{dc\_unb\_T}$ are employed to control the respective voltage amplitude and voltage unbalance of the dc-bus.

4 | MODELING OF THE SERIES CONVERTER

The modeling and the current controllers of the series converter (*abc*-axes) are presented in this section. The parallel converter (4-Leg inverter) modeling has been presented in Reference 19, where the stability analysis has also been presented. Thus, it is assumed in this paper that the control systems that represent both the PWM converters are always stable.

Different from Reference 19, in this paper the current state-feedback controllers are implemented in the 3-phase stationary frame, while the voltage controllers are implemented in the SRF.

4.1 | Modeling of the series converter

The mathematical model that represents the state-space system of the series converter and their transfer functions (TFs) in *abc*-axes are presented in this subsection. The modelling is developed taken into account identical inductances and resistances of the L-filters (Figure 1), as follows: $L_{fsa} = L_{fsa,\ b,\ c} = L_{fs}$ and $R_{fsa,\ b,\ c} = R_{fs}$. Thus, the system can be represented by the following equations:

$$u_{san_s\_pwm} = v_{Lfsa} + v_{Rfsa} + v_{Ca}, \tag{7}$$

$$u_{sbn_s\_pwm} = v_{Lfsb} + v_{Rfsb} + v_{Cb}, \tag{8}$$

$$u_{scn_s\_pwm} = v_{Lfsc} + v_{Rfsc} + v_{Cc}, \tag{9}$$

where $u_{san_s\text{-}pwm}$, $u_{sbn_s\text{-}pwm}$ and $u_{scn_s\text{-}pwm}$ represent the voltages at the 3-Leg-SC inverter terminals; v_{Lfsa}, v_{Lfsb} and v_{Lfsc}.are the filter inductance voltages; v_{Rfsa}, v_{Rfsb} and v_{Rfsc} are the voltages across the filter inductors resistances; and v_{Ca}, v_{Cb} and v_{Cc} are the voltages across the series transformers.

The equation of state-space is represented by

$$\dot{x}_{sabc}(t) = A_{sa,b,c}x_{sa,b,c}(t) + B_{sa,b,c}u_{sa,b,c}(t) + F_{sa,b,c}w_{sa,b,c}(t), \tag{10}$$

where

$$\dot{x}_{sa,b,c}(t) = \begin{bmatrix} \frac{di_{sa}}{\mathrm{dt}} \\ \frac{di_{sb}}{\mathrm{dt}} \\ \frac{di_{sc}}{\mathrm{dt}} \end{bmatrix}; x_{sa,b,c}(t) = \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}; u_{sa,b,c} = \begin{bmatrix} u_{san_s\_pwm} \\ u_{sbn_s\_pwm} \\ u_{scn_s\_pwm} \end{bmatrix}; w_{sa,b,c}(t) = \begin{bmatrix} v_{Ca} \\ v_{Cb} \\ v_{Cc} \end{bmatrix};$$

$$A_{sa,b,c} = \frac{R_{fs}}{L_{fs}} \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix}; B_{sa,b,c} = \frac{1}{L_{fs}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}; \text{and}$$

$$F_{sa,b,c} = \frac{1}{L_{fs}} \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix}.$$

Thus, I basis of Equation (10), the average model of the series converter can be represented in the signal flow graph (SFG) shown in Figure 3, where $Gs_{PI(a,\ b,\ c)}$ represents the current PI controller TF (*abc*-axes), V_{DC} is the dc-bus voltage, $D_{sa,b,c}$ represents the duty cycles and K_{PWM} is the PWM gain given by $K_{PWM} = 1/P_{PWM}$,[28] where P_{PWM} is the peak amplitude of the PWM triangular carrier (DSC). Then, from Figure 3, the closed loop TFs is given by Equation (11), where $Kp_{s(a,\ b,\ c)}$ and $Ki_{s(a,\ b,\ c)}$ are the proportional-integral compensator gains, and $i^*_{s(a,b,c)}(s)$ is the current references in *abc*-axes. Figure 4A and B presents the complete SFGs involving the generation of the current references, and the current controllers in *abc*-axes considering both the ICC and LUnC strategies, respectively,

$$\frac{i_{S(a,b,c)}(s)}{i^*_{S(a,b,c)}(s)} = \frac{X_1\left(Kp_{s(a,b,c)}s + Ki_{s(a,b,c)}\right)}{L_{fs}s^2 + \left(R_{fs} + X_1Kp_{s(a,b,c)}\right)s + X_1Ki_{s(a,b,c)}}, \tag{11}$$

where $X_1 = K_{PWM}V_{DC}$.

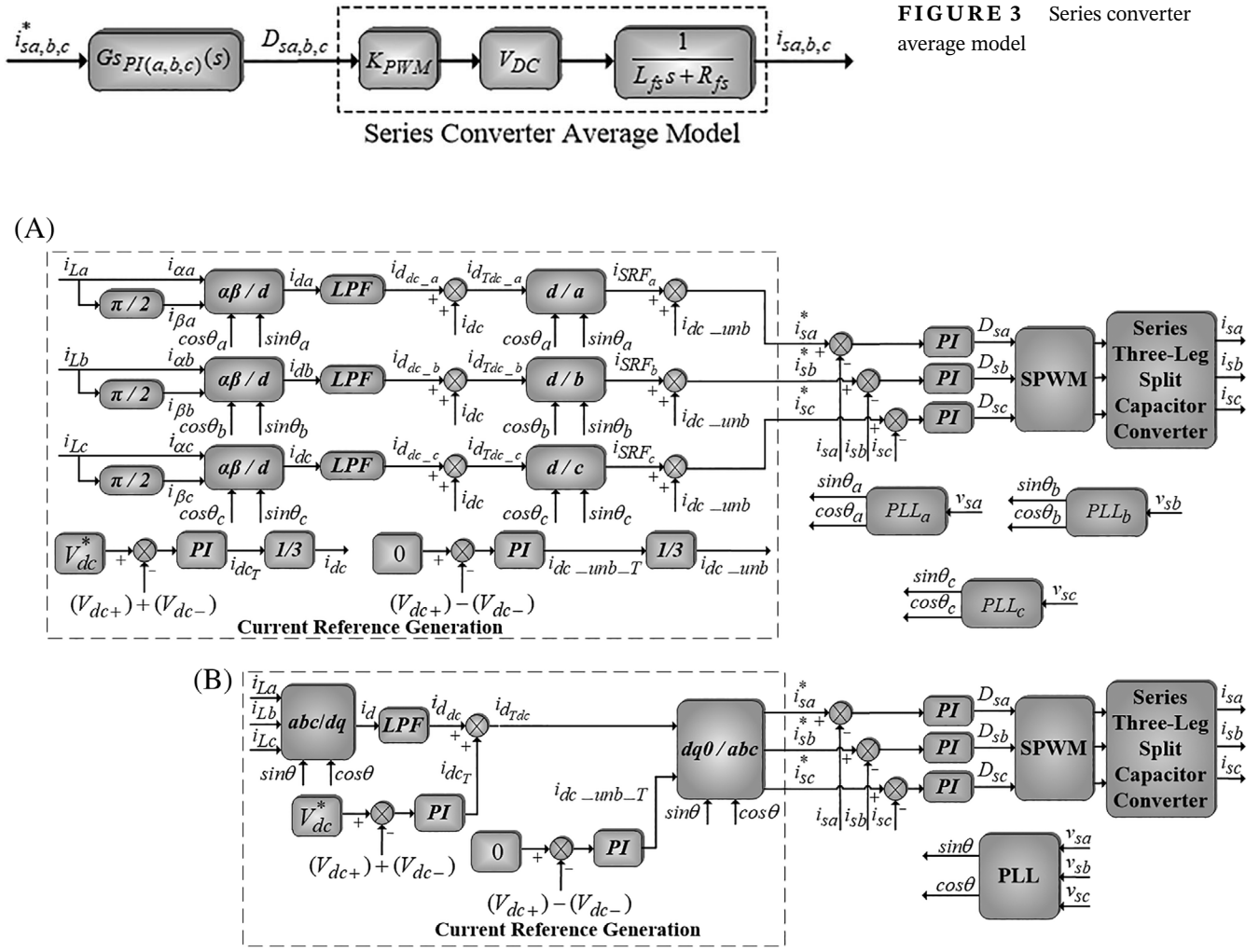

FIGURE 3 Series converter average model

FIGURE 4 Signal flow graph of the series converter: (A) complete SFG involving the generation of the current references and current controllers in *abc*-axes for the ICCS; (B) complete signal flow graph involving the generation of the current references and current controllers in *abc*-axes for the LUnCS

5 | EXPERIMENTAL RESULTS

Figure 5 presents the schematic of the prototype setup used built the UPQC. The algorithms (PLL and SRF) and controllers were embedded into two DSCs (TMS320F28335). In the 3-Leg-SC and 4-Leg converters were used the IGBT modules (SKM100GB 12T4). The parameters used for the experimentation are shown in Table 1. Table 3 presents the controllers' parameters which were obtained based on the design methodology presented in Reference 29. In addition, in Table 2 presents the adopted three-phase non-linear loads used in the tests.

The currents associated to the static behavior of UPQC are presented in Figure 6, where were used the loads shown in Table 2. The two compensation strategies discussed in section 3, such as the LUnCS and ICCS were tested. Figure 6A presents the results considering the LUnCS, where are shown the unbalanced load currents (i_{La}, i_{Lb}, i_{Lc},) and load neutral current i_{Ln}; the compensation currents (i_{ca}, i_{cb}, i_{cc}, i_{cn}) synthetized by the 4-Leg parallel inverter; and the compensated source currents (i_{sa}, i_{sb}, i_{sc}) and the resultant neutral source current i_{sn}. It can be seen, the grid currents are balanced, sinusoidal and have low harmonic contents. In addition, since the neutral load current (i_{Ln}) flows to the parallel inverter, such that $i_{Ln} = i_{cn}$, the neutral grid current i_{sn} is equal to zero. Figure 6B shows experimental results considering the ICCS, in which are shown the unbalanced load currents (i_{La}, i_{Lb}, i_{Lc},) and load neutral wire current i_{Ln}; the compensation currents (i_{ca}, i_{cb}, i_{cc}, i_{cn}) synthetized by the 4-Leg parallel inverter; and the compensated source currents (i_{sa}, i_{sb}, i_{sc}) and the neutral source current i_{sn}. In this case, the grid currents are also sinusoidal, unbalanced, and have reduced harmonic contents. Furthermore, the fundamental component of the load neutral current (i_{Ln}) does not flow

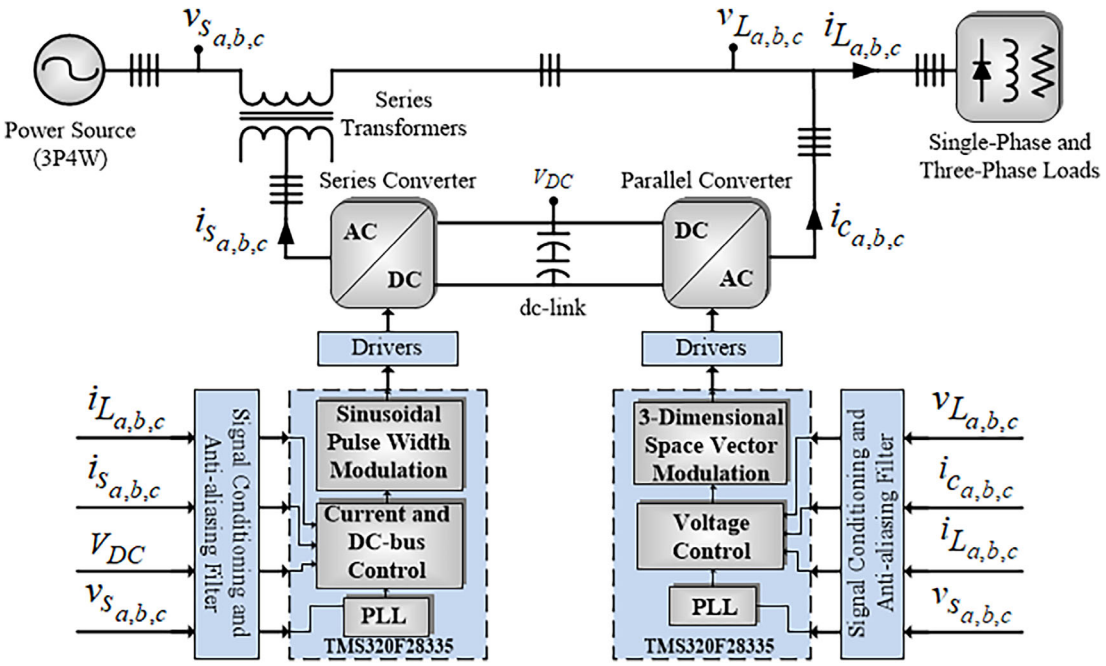

FIGURE 5 Schematic of the UPQC experimental setup

TABLE 1 UPQC parameters

Apparent load power (per phase)	$S_a = 2020$ VA, $S_b = 1310$ VA, $S_c = 1000$ VA
rms utility voltage (line-to-neutral)	$V_{sa,b,c} = 127$ V
Utility grid frequency	$f_s = 60$ Hz
PWM switching frequency (series/parallel converters)	$f_{sw} = 20$ kHz
Parallel converter filtering inductances	$L_{fpa,b,c} = 1.0$ mH
Resistances of the parallel converter inductors	$R_{fpa,b,c} = 0.12\ \Omega$
Parallel converter filtering capacitances	$C_{fpa,b,c} = 85\ \mu$F
Series converter filtering inductances	$L_{fsa,b,c} = 1.5$ mH
Resistances of the series converter inductors	$R_{fsa,b,c} = 0.15\ \Omega$
Series transformers leakage inductances	$L_{dt} = 0.42$ mH
Series transformers resistances	$R_{ta,b,c} = 0.26\ \Omega$
Series transformers (Transformation ratio)	$n = 1$
Voltage of dc-bus	$V_{dc} = 400$ V
Capacitance of the dc-bus	$C_{dc} = 9400\ \mu$F
DSC sampling frequency	$f_a = 40$ kHz
PWM modulator Gain	$K_{PWM} = 2.66.10^{-4}$

through the parallel converter, such that i_{cn} is composed of only harmonic components. Thus, this fundamental component flows through the utility neutral wire, and, hence, the neutral source current i_{sn} is not zero.

The load and grid currents total harmonic distortion (THD) taking into account the UPQC operating based on the LUnCS and ICCS are shown in Table 4, where can be noticed the reduced THDs related to the compensated grid currents.

Figure 7 presents the behavior of the UPQC under load transients. In Figure 7A the loads connected to phases "a" and "c" are disconnected at different times, while the load connected to the phase "b" remains operating continuously.

TABLE 2 Parameters of the loads

3-phase unbalanced loads	Phase "a"	Phase "b"	Phase "c"
3-single-phase full-wave rectifiers	R = 5.7 Ω L = 380 mH	R = 7.2 Ω L = 346 mH	R = 12.9 Ω C = 940 μF

TABLE 3 Design specifications and gains of the PI controllers

P-APF				S-APF		
dq0-frame	Outer loops		Inner loops	*abc*-frame	Kp_s	Ki_s
	Kp_p	Ki_p	Kp_{pi}			
dq	0.2333	549	90	*abc*	447.81	110 760
0	0.2381	526	361			
dc-bus voltage controller				$Kp_{dc} = 0.0357$		$Ki_{dc} = 0.1202$
dc-bus voltage unbalance controller				$Kp_{dc\_unb} = 0.7086$		$Ki_{dc\_unb} = 0.6995$
Crossover frequency of the parallel converter(inner control loops)				$\omega_{c_{ip}} = 2\pi f_s/6\, rad/s$		
Phase margin				$PM_{ip} = 75°$		
Parallel converter crossover frequency (outer control loops)				$\omega_{c_{vp}} = 0.16\omega_{ci_p}\, rad/s$		
Phase margin				$PM_{vp} = 55°$		
Series converter crossover frequency (current controllers)				$\omega_{c_{is}} = 2\pi f_s/9\, rad/s$		
Phase margin				$PM_{is} = 50°$		
dc-bus voltage controller crossover frequency				$\omega_{c_{v_{dc}}} = 125.66\, rad/s$		
Phase margin				$PM_{v_{dc}} = 89°$		
dc-bus loop voltage unbalance controller crossover frequency				$\omega_{c_{v_{dc\_unb}}} = 37.69\, rad/s$		
Phase margin				$PM_{v_{dc\_unb}} = 89°$		

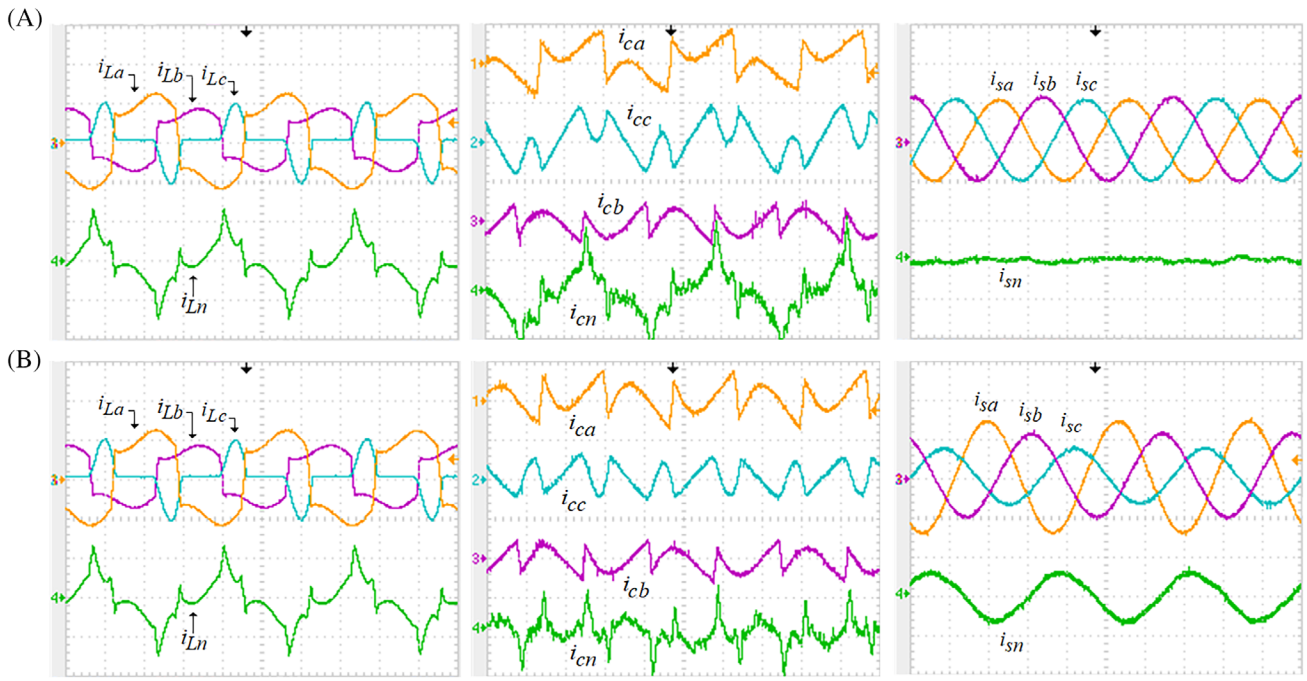

FIGURE 6 UPQC currents considering unbalanced loads (three single-phase loads: (A) UPQC currents for the LUnCS (20 A/div, 5 ms/div): Currents of the load (i_{La}, i_{Lb}, i_{Lc}) and i_{Ln}, parallel converter currents (i_{ca}, i_{cb}, i_{cc}) and i_{cn}, compensated source currents (i_{sa}, i_{sb}, i_{sc}) and neutral grid current i_{sn}; (B) UPQC currents for ICCS (20 A/div, 5 ms/div): (i_{La}, i_{Lb}, i_{Lc}) and i_{Ln}, (i_{ca}, i_{cb}, i_{cc}) and i_{cn}, (i_{sa}, i_{sb}, i_{sc}) and i_{sn}

TABLE 4 Load and grid currents THDs

Compensation Strategies	THD %					
	i_{La}	i_{Lb}	i_{Lc}	i_{sa}	i_{sb}	i_{sc}
LUnCS	29.3	29.8	61.5	1.2	1.1	1.1
ICCS	29.3	29.8	61.5	0.9	1.4	1.8

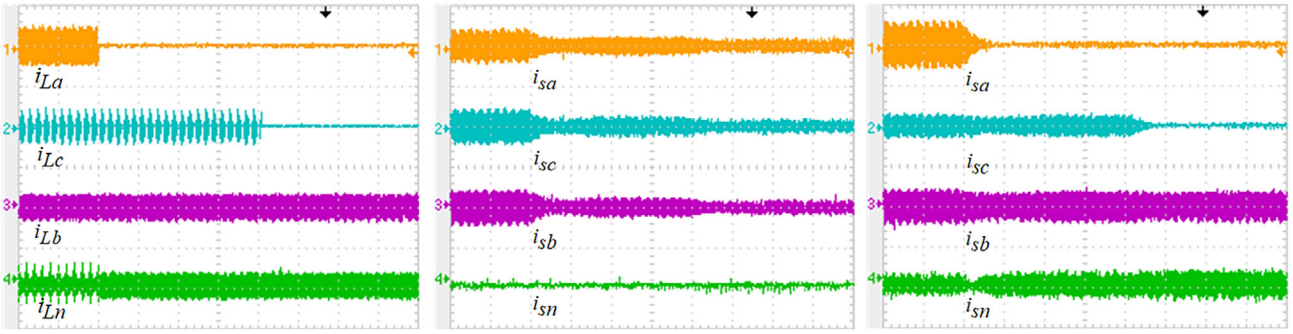

FIGURE 7 UPQC currents considering load transients for LUnC and ICC strategies: (A) Load currents (i_{La}, i_{Lb}, i_{Lc}) and i_{Ln} (50 A/div, 500 ms/div); (B) compensated grid currents for LUnC strategy (i_{sa}, i_{sb}, i_{sc}) (50 A/div, 500 ms/div); (C) compensated grid currents for ICC strategy (i_{sa}, i_{sb}, i_{sc}) (50 A/div, 500 ms/div)

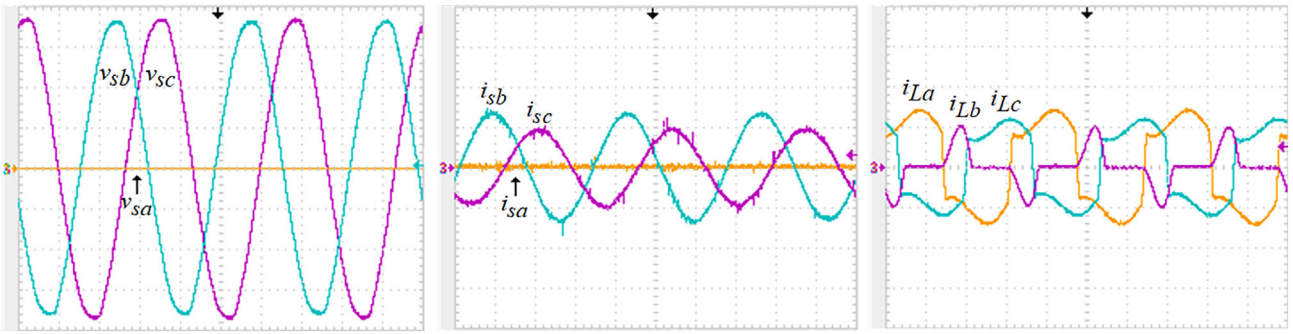

FIGURE 8 UPQC currents and voltages considering the grid voltage outage (ICC strategy): (A) Grid voltages (v_{sa}, v_{sb}, v_{sc}) (50 V/div, 5 ms/div); (B) compensated grid currents for ICC strategy (i_{sa}, i_{sb}, i_{sc}) (20 A/div, 5 ms/div); (C) unbalanced currents of the load (i_{La}, i_{Lb}, i_{Lc}) (10 A/div, 5 ms/div)

It can be noticed in Figure 7B that due to the use of the LUnCS, the grid currents (i_{sa}, i_{sb}, i_{sc}) remain balanced and, therefore, the neutral current i_{Ln} is null. On the other hand, when the ICCS is employed, as shown in Figure 7C, both the currents related to the phases "a" and "c" go to zero ($i_{sa} = i_{sb} = 0$), since their respective loads were disconnected. This test shows that the LUnCS was very useful to maintain the grid currents balanced even under load transients.

Figure 8 presents the UPQC utility voltages (v_{sa}, v_{sb}, v_{sc}), the input currents (i_{sa}, i_{sb}, i_{sc}) and the load currents (i_{La}, i_{Lb}, i_{Lc}), when a voltage outage occurs in phase "a" (Figure 8A). As can be noted, when the UPQC operates with ICCS, even occurring outage in one of the three-phase utility voltages, the system remains operating normally. Figure 8C shows the unbalanced non-linear loads. Thus, the compensated grid currents (i_{sb}, i_{sc}) are also unbalanced as presented in Figure 8B.

The dc-bus voltages dynamic behavior is presented in Figure 9. Figure 9A shows the total voltage (v_{dc}) of the dc-bus and the voltages (v_{dc+}, v_{dc-}) of the split-capacitors, when the control action is used to perform the voltage balance. Figure 9B presents the dc-bus voltages (v_{dc}, v_{dc+}, v_{dc-}) when load transient occurs by disconnecting and reconnecting the phase "a." As can be noticed, the dc-bus voltage is maintained controlled at 400 V.

The static behavior of the UPQC voltages (grid and load voltages) is shown in Figure 10, where the unbalanced utility voltages (v_{sa}, v_{sb}, v_{sc}) with high level of harmonic contents are presented in Figure 10A. The voltages across the

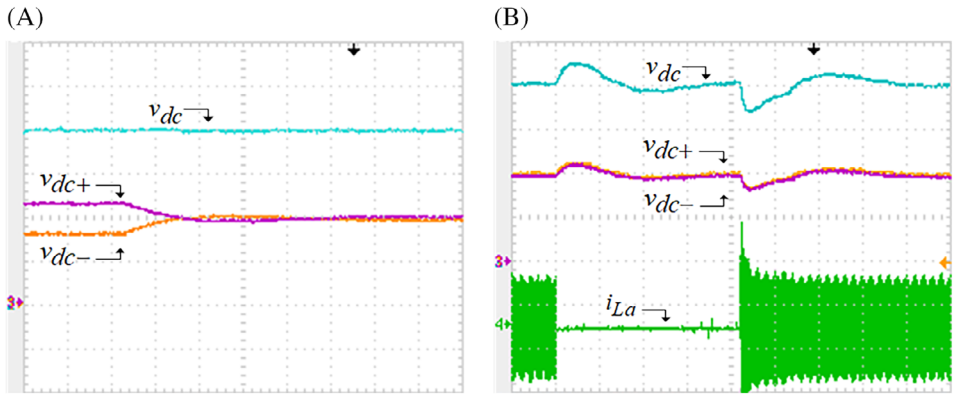

FIGURE 9 UPQC currents and voltages operating with unbalanced 3-phase load: (A) voltages of the dc-bus (v_{dc}, v_{dc+}, v_{dc-}) (100 V/div, 20 A/div, 500 ms/div); (B) voltages of the dc-bus (v_{dc}, v_{dc+}, v_{dc-}) and phase "a" load current (i_{La}) (100 V/div, 20 A/div, 250 ms/div)

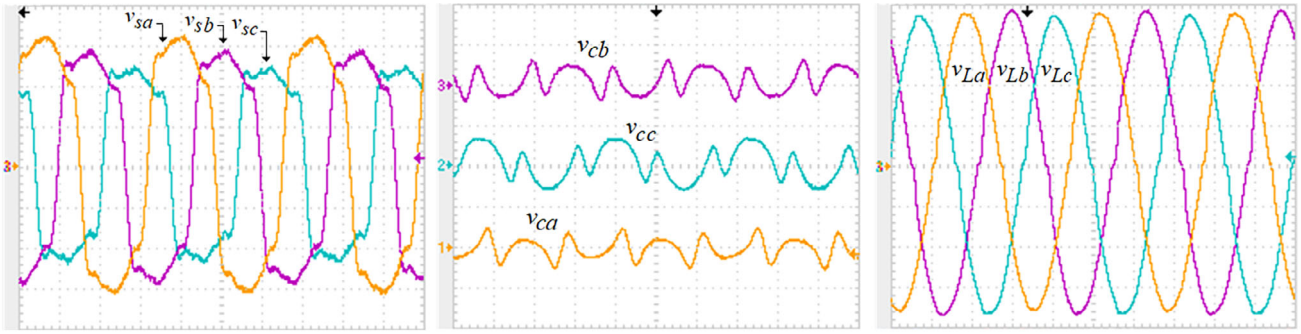

FIGURE 10 UPQC voltages under utility disturbances (unbalances and harmonics): Grid voltages (v_{sa}, v_{sb}, v_{sc}) (50 V/div, 5 ms/div), coupling transformer voltages (v_{Ca}, v_{Cb} and v_{Cc}) (100 V/div, 5 ms/div), and output voltages (v_{La}, v_{Lb}, v_{Lc}) (50 V/div, 5 ms/div)

TABLE 5 Grid and load voltage THDs (%)

Grid			Load		
v_{sa}	v_{sb}	v_{sc}	v_{La}	v_{Lb}	v_{Lc}
29.7	32.8	37.7	1.8	1.7	2.5

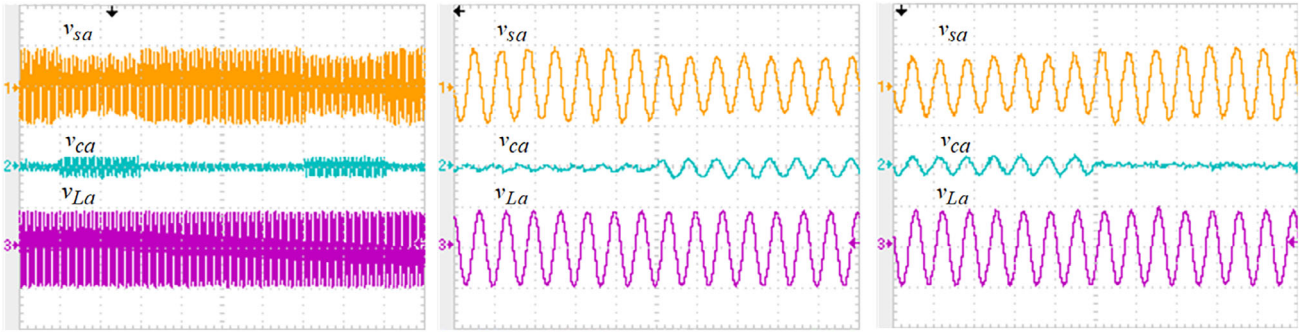

FIGURE 11 Phase "a" UPQC voltage operating under sag disturbance: (A) grid voltage (v_{sa}), output voltage (v_{La}) and coupling transformer voltage (v_{ca}) (200 V/div, 250 ms/div); (B) detail of the utility voltage sag (normal to abnormal condition) (200 V/div, 25 ms/div); (C) detail of the utility voltage sag (abnormal to normal condition) (200 V/div, 25 ms/div)

coupling transformers (v_{Ca}, v_{Cb}, v_{Cc}) are shown in Figure 10B, whereas the load voltages (v_{La}, v_{Lb}, v_{Lc}) are shown in Figure 10C. Thus, the parallel converter feeds the loads with balanced, sinusoidal and regulated voltages. In addition, low voltage THD is achieved. Since sinusoidal load voltage are provided by the parallel converter, the coupling transformers voltages (v_{Ca}, v_{Cb}, v_{Cc}) are composed of the difference between the grid voltages and the load voltages.

Thus, indirect compensation of voltage is performed, since the series transformers absorb the utility disturbances. Table 5 presents the grid and load UPQC voltages THDs, where significant attenuation of the output voltages harmonic is noted.

Figure 11A presents the UPQC dynamic behavior when utility voltage sag disturbances (30%) occur in the phase "a" (v_{sa}) for 30 utility grid cycles. It can be noted, voltage sag disturbances do not interfere in the UPQC voltage (v_{La}) that remains regulated and sinusoidal, as can be observed in detail in Figure 11A and B. In Figure 11 are also shown details related to the compensation voltage v_{Cc}.

6 | CONCLUSIONS

This paper proposed a 3P4W UPQC configuration operating with independent grid current control and possibility to reduce the dc-bus voltage amplitude. The use of the 4-Leg inverter operating as parallel converter allows the deduction of the dc-bus voltage magnitude when compared to that used in the 3-Leg-SC inverter. Thus, since the parallel converter determined the dc-bus voltage amplitude, the adequate operation of the series 3-Leg-SC converter was assured. In addition, the use of the 3-Leg-SC topology as series converter allowed the adoption of two compensating strategies, the ICCS and LUnCS. Using the ICCS, the control of the grid currents could be performed independently per phase. In this case, the UPQC was able to operate normally even in occurrence of voltage outage that occurred in one of the three phases of the grid voltage (phase "*a*"), showing the versatility of the adopted ICCS. On the other hand, the adoption of the LUnCS allowed the operation of the UPQC with balanced grid currents even under any load condition.

Both the UPQC static and dynamic performances were tested by means of extensive practical experimentations, such that both theoretical development and the effectiveness of the UPQC could be confirmed.

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NOMENCLATURE

Ω	Ohm
α	direct stationary reference frame
β	quadracture stationary reference frame
θ	θ_a, θ_b and θ_c (phase-angles)
π	pi
μF	micro-Farady
mH	mili-Henry
s	second

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