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Introduction of the SOI MOSFET Dimensions in the High-Temperature Leakage Drain Current Model

Marcelo Bellodi
João Antonio Martino
Denis Flandre

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INTRODUCTION of the SOI MOSFET DIMENSIONS in the HIGH-TEMPERATURE LEAKAGE DRAIN CURRENT MODEL

Marcello Bellodi, João Antonio Martino and Denis Flandre*
Laboratory of Integrated Systems, University of São Paulo, LSI / PEE / USP
Av. Prof. Luciano Gualberto, 158, trav. 3 - 05508-900, São Paulo, S.P., Brazil
Fax: +55-11-818-5665, E-mail: bellodi@lsi.usp.br or martino@lsi.usp.br
* Microelectronics Laboratory, Université Catholique de Louvain,
E-mail: flandre@dice.ucl.ac.be

ABSTRACT

In this work we studied and modeled the impact of the dimensions on the behavior of the leakage drain current of accumulation-mode SOI MOSFETs operating in the temperature range from 50 to 200°C. The influence of the transistor channel length L and width W on the leakage drain current, which were neglected in the previous analysis, is here modeled from room to high temperature. Experimental data and simulations which support the proposed influence of the dimensions are reported.

I. INTRODUCTION

The interest in SOI (*S*ilicon-*o*n-*I*nsulator) MOS technology has been increasing in the last years, in particular because this technology can be used in severe environments in which conventional bulk MOS circuits can not operate satisfactorily. In particular, integrated circuits may have to operate up to 200 - 300°C, such as in nuclear power plants, engine control, aerospace applications[1].

When conventional bulk MOSFET is used in this high temperature range, it will fail due to the excessive junction leakage currents and threshold voltage shifts [2].

On the other hand, thin-film fully-depleted SOI MOSFETs feature much reduced leakage currents and threshold voltage variations up to elevated temperatures and latch-up is moreover inherently absent in SOI CMOS circuits [3].

The design of high temperature SOI CMOS circuits is then possible but requires accurate modeling of the device characteristics as a function of temperature.

When circuits are operating at high temperature, the increase of junction leakage current is one of the main cause of failure, which is proportional to the area of junctions [3].

In the SOI MOSFET the drain and source junctions area is much smaller (about 15 to 100 times) in comparison to bulk MOSFET and besides the absence of the well junctions in SOI transistors, both contributes to the reduction of the overall standby current consumption of SOI circuits in comparison with bulk circuits [4].

In this work, the SOI MOSFET dimensions i.e., the channel length L and the channel width W, are introduced in the drain leakage current model valid from room to high temperatures [5].

II. EXPERIMENTAL

The devices used were accumulation-mode SOI pMOSFET L-array with W = 20μm and L= 3, 5 and 10μm. These devices have been fabricated in a 3.0μm SOI CMOS process using SIMOX substrate. The thickness of Silicon film t_{Si} is 84nm, front gate oxide t_{oxf} is 32nm, and buried oxide (back gate oxide) t_{oxb} is 398nm.

The leakage drain current I_{Dleak} is extracted from the drain current as function of drain voltage for front gate voltage V_{GF} = 1.0V and back gate voltage V_{GB} = 0V.

The measurements of the I_{Dleak} *vs.* V_D curves were performed using a HP-4145B parameter analyzer and a hot-chuck temperature-regulated from 50 to 300°C.

III. DRAIN LEAKAGE CURRENT MODEL

This empirical model was extracted from the I_{Dleak} *vs.* V_D curves, for the different temperatures of operation, i.e., from room temperature to 200°C. So, to obtain it, we divided, for each operation temperature, the I_{Dleak} *vs.* V_D curve in two regions, as shown in figure 1. These two regions feature an approximated linear dependence of I_{Dleak} on V_D .

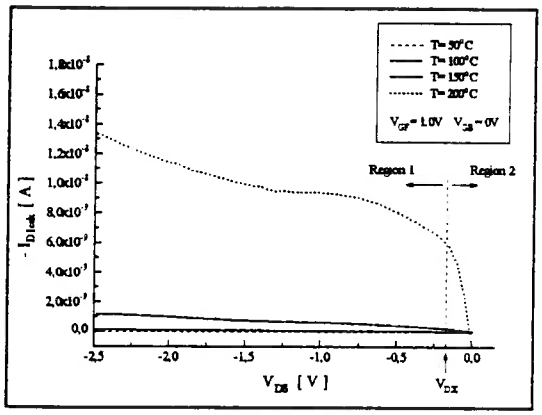

Figure 1: I_{Dleak} *vs.* V_D curves for SOI pMOSFET of W= 600μm and L= 20μm.

In order to empirically fit these I_{Dleak} *vs.* V_D curves, we thus used a double linear fitting, one in region 1 ($-2.5 \leq V_D < -V_{DX}$) and another in region 2 ($-V_{DX} \leq V_D \leq 0$), where the V_{DX} voltage was experimentally obtained. This value is V_{DX} = -0.2V to have better fitting results for the samples measured [5].

At first time, the leakage drain conductance G_{Dleak} was experimentally obtained for different temperatures in regions 1 and 2. In region 1, G_{Dleak} was obtained as a linear regression of I_{Dleak} for $-2.5 \leq V_D < -0.2$V, and in region 2, from a straight line drawn between V_D = -0.2V and the origin $I_D = V_D = 0$ point.

The G_{Dleak} exponential increase with the temperature was experimentally modeled by the expressions (1) and (2) in both regions, as follows:

$$G_{Dleak} = 4.97x10^{-12} \; x \; 10^{\left(\frac{T-50}{54}\right)} \quad : \; T \geq 50°C \text{ and } -2.5 \leq V_D < -0.2V \quad (1)$$

$$G_{Dleak} = 1.92x10^{-11} \; x \; 10^{\left(\frac{T-50}{48}\right)} \quad : \; T \geq 50°C \text{ and } -0.2 \leq V_D \leq 0V \quad (2)$$

Thus, to obtain the drain leakage drain current model, G_{Dleak} equation was integrated as function of V_D, which yields:

$$I_{Dleak} = A \; x \; 10^{\left(\frac{T-T_0}{B}\right)} \; x \; V_D + K \quad (3)$$

The K constant was extracted from the experimental data. In the case of our experimental data, K_1 was optimized as follows:

$$K_1 = -2.92x10^{-12} \; x \; 10^{\left(\frac{T-50}{47}\right)} \quad : T \geq 50°C \text{ and } -2.5 \leq V_D < -0.2V \quad (4)$$

Finally, including (4) in (3) yields:

$$I_{Dleak} = 4.97x10^{-12} \; x \; 10^{\left(\frac{T-50}{54}\right)} \; x \; V_D \; - \; 2.92x10^{-12} \; x \; 10^{\left(\frac{T-50}{47}\right)} \quad (5)$$

For $-2.5 \leq V_D < -0.2V$ and $T \geq 50°C$

In the case of region 2, constant K was determined imposing that I_{Dleak} tends to zero for $V_D = 0V$, this yields $K_2 = 0$. So, from (2) and (3), we derive:

$$I_{Dleak} = 1.92x10^{-11} \; x \; 10^{\left(\frac{T-50}{48}\right)} \; x \; V_D \quad : T \geq 50°C \text{ and } -0.2 \leq V_D \leq 0V \quad (6)$$

IV. INFLUENCE OF THE SOI MOSFET DIMENSIONS

To determinate the influence of the SOI MOSFET dimensions on the behavior of the leakage drain current at high temperatures, we used the MEDICI bidimensional simulator [6]. With this simulator, it was possible to understand how the leakage drain current behaves in function of the temperature and the transistor dimensions.

The objective of that study is to assess:

- Whether the lateral edge parasitic leakage current normally negligible in accumulation-mode SOI p-MOSFETs at room temperature remains negligible at higher temperatures, even for small device width W.
- Which dependence of the leakage current on the device length L dominates at elevated temperature, either the decrease with the increasing length due to the electric field, or the increase with increasing L due to the volume of thermally-generated excess carries [2].

At first time, we observed that for the same operation conditions (bias and temperature), but changing only the transistor channel width W, the module of the leakage drain current is almost constant, as can be seen in figure 2. This effect happens because the influence of the parasitic edge effects are negligible.

Similar experimental behavior was observed, as is shown in figure 2.

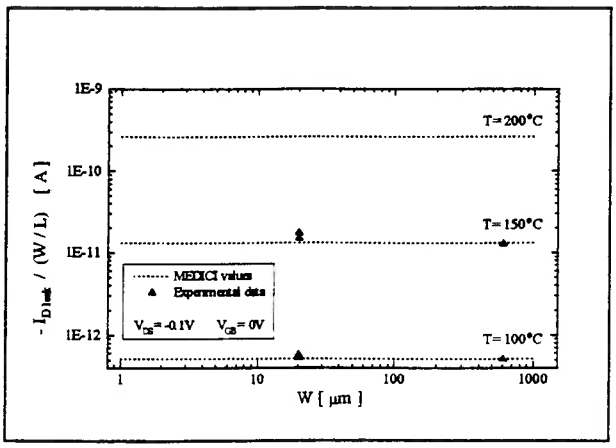

Figure 2: Variation of the leakage drain current as a function of the W in the same conditions.

On the other hand, doing the same simulations, but now changing only the transistor channel length L, we observed that the module of the leakage drain current decreases if L increases, as shown in figure 3.

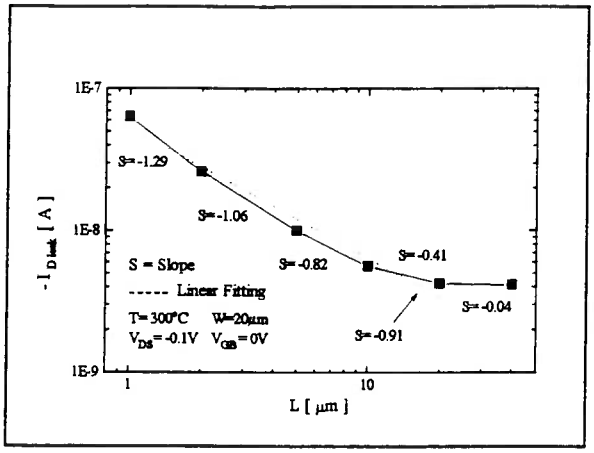

Figure 3: Variation of the leakage drain current as a function of the L (MEDICI data).

The same impact of L was experimentally observed, as shown in figure 4.

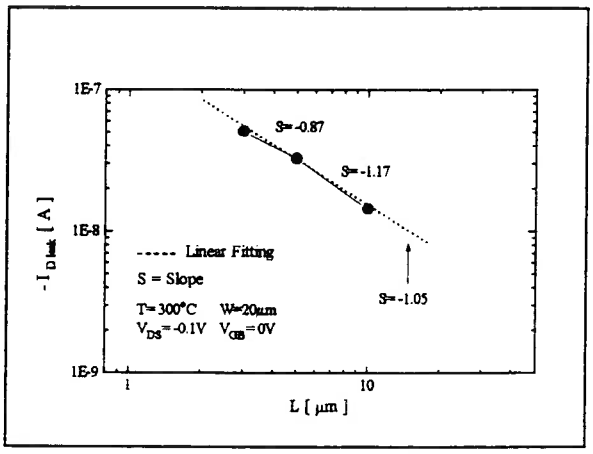

Figure 4: Variation of the leakage drain current as a function of the L (experimental data).

Thus, to model the dependence of the leakage drain current on L, we examined the slope of I_{Dleak} *vs.* L in experimental and simulation curves.

Figures 3 and 4 both show the partial slopes between two data and the global linear fitting. Table 1 shows a comparison between the slope obtained from the experimental and simulated curves presented in the figures 3 and 4.

Table 1: Comparison between the linear fitting from the experimental and simulation data.

L (µm)	Experimental	Simulation
$1 \leq L \leq 20$	-1.051	-0.914
$20 \leq L \leq 40$	----------	-0.042

As can been seen in table 1 for channel length lower than 20μm, the slope of both experimental and simulated results are around -1.0, which means that the variation of drain leakage drain current is proportional to $1/L$.

Otherwise for channel length higher than 20μm, the slope becomes lower and tends to be zero confirming the analysis presented on reference [7].

V. DRAIN LEAKAGE CURRENT MODEL WITH THE CHANNEL DIMENSIONS

So, taking into account the dependence of the drain leakage current on W and L, the basic drain model was optimized by the following expression:

$$I_{Dleak} = \frac{W}{L} \times \left[A \times 10^{\left(\frac{T - T_0}{B}\right)} \times V_D - C \times 10^{\left(\frac{T - T_0}{D}\right)} \right] \quad (7)$$

Applying this model to the experimental data, yields:

- **Region 1:** *For* $-2.5 \le V_D < -0.2V$, $L \le 20\mu m$ *and* $50 \le T \le 200°C$

$$I_{Dleak} = \frac{W}{L} \times \left[1.66 \times 10^{-13} \times 10^{\left(\frac{T - 50}{54}\right)} \times V_D - 9.7 \times 10^{-14} \times 10^{\left(\frac{T - 50}{47}\right)} \right] \quad (8)$$

- **Region 2:** *For* $-0.2 \le V_D < 0V$, $L \le 20\mu m$ *and* $50 \le T \le 200°C$

$$I_{Dleak} = \frac{W}{L} \times \left[6.4 \times 10^{-13} \times 10^{\left(\frac{T - 50}{48}\right)} \times V_D \right] \quad (9)$$

Figure 5 shows the good agreement achieved between the experimental data and the full drain leakage current model.

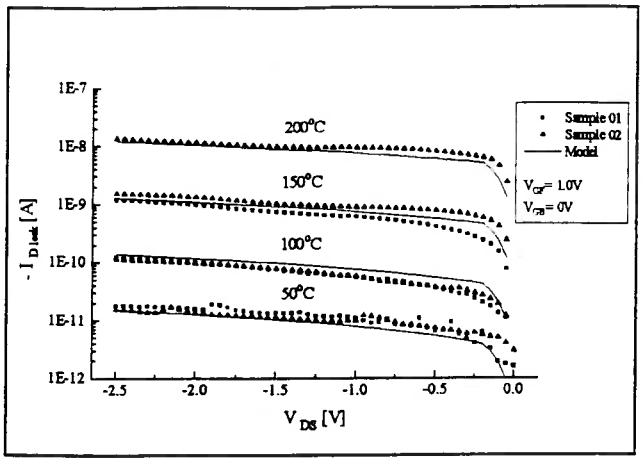

Figure 5: I_{Dleak} *vs.* V_{DS} curves for SOI pMOSFET of W= 600μm and L= 20μm, compared with the proposed model.

VI. CONCLUSIONS

In this work, a new model taking into account the dependence of the drain leakage current of accumulation-mode SOI MOSFETs, on both the width *W* and the length *L* of the channel transistor was published. Good agreement was found between model and experimental data in the temperature range studied, and for channel length lower than 20μm. For channel length higher than 20μm, the current becomes almost constant.

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REFERENCES

[1] T. Y. Chan, "Design of MOS integrated circuits at high-temperature", Ph.D. dissertation, Univ. of Arizona, Ticson, 1982.

[2] D. Flandre et al., "Demonstration of Potential of Accumulation-Mode MOS Transistors on SOI Substrates for High-Temperature Operation (150 - 300°C)", IEEE Electron Device Letters, Vol. 14, n°01, January / 1993.

[3] J. P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI", Kluwer Academic, 1991.

[4] A. J. Auberton-Hervé , J. P. Colinge and D.Flandre; "High-Temperature Applications of SIMOX Technology"; Japanese Solid-State Technology; 12-17, December 1993.

[5] M. Bellodi, J. A. Martino and D. Flandre; "New Empirical Model for Leakage Drain Current of SOI MOSFETs Valid from Room to High Temperatures"; Journal of Solid-State Devices and Circuits; Vol.04; n°.01; January 1996.

[6] TMA MEDICI: Two-Dimensional Device Simulation Program, version 2_1_2, Technology Modeling Associates Inc., Palo Alto, CA 1995.

[7] Y. Arimoto; "High-Temperature Operation of nMOSFET on Bonded SOI"; IEICE Trans. Electron.; Vol.E75-C, n°. 12; December 1992.

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