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A Design of a Redundancy-Based Cascaded Bidirectional DC-DC Converter for Improved Reliability in Energy Storage Devices

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ABSTRACT This paper proposes a redundancy-based cascaded bidirectional dc/dc converter designed to interface battery energy storage system (BESS) units. With the employment of this topology, its reliability is increased due to redundancy in power conversion, which differs from conventional structures formed by dc/dc converters that cannot process power flow when a fault occurs. Thus, the topology is provided merging the cascaded bidirectional Boost converter (CBB) and cascaded bidirectional Cuk converter (CBC). Subsequently, the coupled mathematical model of the proposed topology can be readily calculated, considering all feasible (different) sub-circuits according to the switching pattern. Therefore, small-signal analysis is applied to design the PI controllers, followed by a closed-loop performance evaluation using an infinity norm and stability analysis to assess the operation of the dc/dc converter in closed-loop for different values of load and current references. Finally, a lab-scale prototype and a hardware-in-the-loop (HIL) setup prove the effectiveness of the dc/dc converter working in various scenarios and also operating with the traditional SoC-based droop for balancing the BESS units.

INDEX TERMS battery energy storage system (BESS) units, fault-tolerant, redundancy-based, stability analysis, state-space.

I. INTRODUCTION

THE application of power electronic converters such as connecting alternative sources to the grid, flexible high-voltage direct current transmission systems, electric vehicles and the management of battery energy storage system (BESS) by absorbing or supplying power at steady-state and transitory regimes are crucial for the new tends in smart grids [1], [2]. Additionally, they can control their currents and/or voltages to match with the requirements of the distributed system and thus, the combination of them and their topologies play an important role for voltage regulation and management of the power flow for alternative sources.

Although the applications of conventional power converters, with two independent dc/dc converters tied to a common link is usual, if a fault or an operational problem such as cyberattack occur in the power device structure, the alternative source or the BESS connected to their inputs will not able to operate properly. On the other hand, the proposed redundancy-based cascaded bidirectional dc/dc converter, improves the reliability if one part of its physical structure suffers a fault or maintenance.

Regarding the reliability, it is indispensable a system that contain redundancies in telecommunication, aerospace system, military devices, medical centers and renewable energy system applications to ensure the continuity of operation during electrical faults [3], [4]. According to [2], [5], in several applications of power electronics, operational issues such as damages on semiconductors can result in repair costs

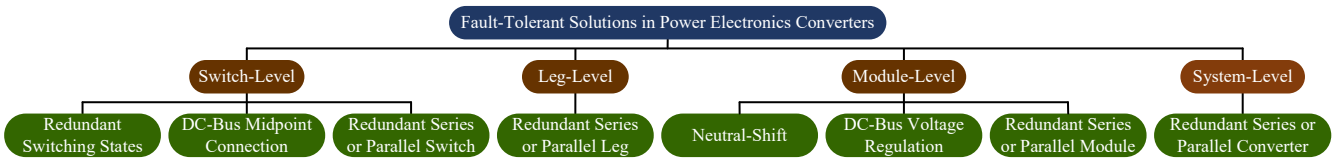

FIGURE 1. Fault-tolerant methods for Power Electronics Converters [2].

and operational expenses. Moreover, the improper operation of the power module can lead to interruption fees, further adding to the overall cost. As a result, reducing failure rate and fault-tolerant capabilities are the solutions to increase the reliability of dc/dc converters [6].

The methodologies addressed to fault-tolerant in power electronics converters are presented in Fig. 1, organized in switch-level, leg-level, module-level and system-level. Regarding switch-level, it can be applied to redundant switching states [7], [8], converters with connection to the midpoint of dc-link via extra auxiliary switch [9] and the application of redundant switches in parallel or series to the main switches [10]. Considering leg-level, redundant parallel leg is employed in [11] and [12] to mitigate the impact of electrical faults.

Additionally, cascade and modular multi-level converters are the topologies of module-level fault-tolerant which are divided in neutral-shift [13], [14], dc-bus voltage regulation [15] and redundant series or parallel module [16]–[18]. Moreover, regarding system-level, the topology presented in [19] is an example of redundant parallel converter. In reference to the dc/dc converter presented in [20], the redundant modules are designed to increase the voltage transfer ratio of the topology, while the proposed approach employs redundant modules to enhance the reliability of the BESS units.

Therefore, this paper proposes a redundancy-based cascaded bidirectional dc/dc converter composed by a combination between cascaded bidirectional Cuk converter (CBC) and cascaded bidirectional Boost converter (CBB). The proposed power device is specifically designed to interface two BESS units with a common input, offering enhanced functionality and reliability. The CBC functionalities are performed to establish the connection with the dc-link, ensuring a continuous current flow that promotes a stable dc-link voltage even in the presence of load variations, different from the dc/dc converter topologies in [21]–[24]. Furthermore, the CBB operates as an extra module, responsible for controlling the power flow during faults. Thus, the proposed redundancy-based cascaded bidirectional dc/dc converter can handle operations with sensitive loads that must operate continuously, such as in medical centers and aircraft applications, resulting in reliable performance.

According to the proposed solution, the authors evaluate its performance by employing three different tests. In the first, the experimental results and the computation simulations are performed to verify the effectiveness of the theoretical analysis in open-loop conditions (error $< 5\%$). In the second test, the ability to regulate power flow through the proposed structure is examined, while in the last, a test addressing the state of charge (SoC) balancing into the redundancy-based dc/dc converter topology by using a traditional SoC-based droop for the energy management system (EMS) is checked according to the methodology developed in [25].

In order to analyze the stability of the redundancy-based cascaded bidirectional dc/dc converter, a modeling approach is employed that takes into account the impact and interplay of the semiconductors in both the CBB and CBC via Lyapunov's indirect method [26]. Therefore, the main contribution of the paper are listed as follows.

1) Reliability with redundancy on power conversion for energy storage device applications;
2) The controllers can be designed in an independent way, which would be suitable for EMS.
3) Fault-tolerant suitable for BESS equalization;
4) The currents from the BESS are split across the inductances, allowing for a reduction in component stress.

The paper is organized as follows. The proposed topology is presented in Section II. The detailed analytical model is calculated at steady-state with state-space, input and output matrices in Section IV. Section V defines the steady-state analysis with average matrices that describe the complete model of the dc/dc converter, while Section VI evaluates the analysis of efficiency. Section VII performs the small-signal analysis to apply the proportional-integral (PI) controllers. In Section VIII, the stability analysis is checked using the infinity norm $\|H_\infty\|$ and the Lyapunov's Indirect Method, while experimental results are shown in Section IX. Finally, Section X presents conclusions and final remarks.

II. PROPOSED TOPOLOGY

The proposed redundancy-based cascaded bidirectional dc/dc converter consists of a CBC and CBB (with shared inputs, BESS1 and BESS2), as shown in Fig. 2. The CBB integrates 2 bidirectional Boost converters using capacitance C_3, while the CBC combines Cuk1 and Cuk2 with the common output capacitance C_o.

Firstly, considering Cuk1, the terminal voltage and current for BESS1 are denoted as v_{bat1} and i_{bat1}, the currents i_{L1} and i_{L2} are flowing through inductances L_1 and L_2, and the capacitance C_1 are receiving energy from BESS1

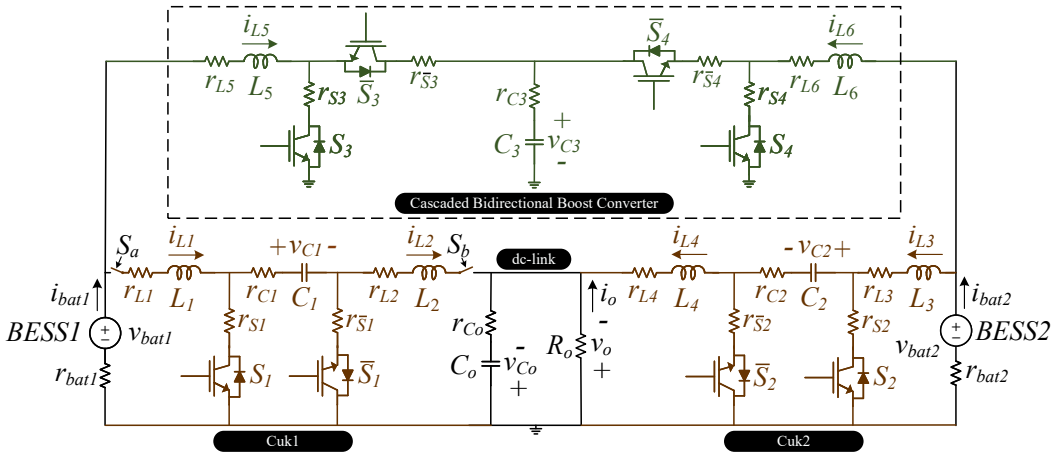

FIGURE 2. Redundancy-based cascaded bidirectional dc/dc converter.

and supplying the dc-link, respectively. In this context, the controlled semiconductors for Cuk1 are represented by S_1 with $\bar{S}_1$ receiving complementary pulse-width-modulation (PWM) signals to prevent discontinuous conduction mode.

In the case of Cuk2, the terminal voltage and current for BESS2 are v_{bat2} and i_{bat2}, with the inductances L_3 and L_4 carrying the currents i_{L3} and i_{L4} and the capacitance C_2 absorbing energy from BESS2 and delivering it to the dc-link. Similar to Cuk1, the controlled semiconductors, represented by S_2 and $\bar{S}_2$, use complementary PWM signals to avoid discontinuous conduction mode.

Regarding the CBB, current i_{L5} flows through L_5 and i_{L6} flows through L_6, the active semiconductors S_3 and $\bar{S}_3$ are placed next to v_{bat1}, while S_4 and $\bar{S}_4$ are positioned close to v_{bat2}, with the PWM signals of $\bar{S}_3$ and $\bar{S}_4$ being complementary to S_3 and S_4 also to avoid discontinuous conduction mode. In this way, the dc-link includes the common capacitance C_o, the output load R_o, the output voltage v_o, and the output current i_o.

Additionally, the main module in the power converter is the CBC. Since the proposed topology is suitable for receiving sensitive loads, the CBC should receive a continuous power on the main dc-link without any pulsed current. Therefore, a Cuk-based topology is indicated, as shown in the characteristics of Cuk converters in [27]. In contrast, the design of CBB is sufficient, because it is responsible for improving the operation of the proposed solution when no load is connected to C_3. Its role lies in managing the power flow between BESS1 and BESS2 in both directions.

The complete model incorporates internal losses of inductors (r_{L1}, r_{L2}, r_{L3}, r_{L4}, r_{L5}, and r_{L6}), capacitances (r_{C1}, r_{C2}, r_{C3}), and r_{Co}, controlled semiconductors (r_{S1}, $r_{\bar{S}1}$, r_{S2}, $r_{\bar{S}2}$, r_{S3}, $r_{\bar{S}3}$, r_{S4}, and $r_{\bar{S}4}$), and BESSs (r_{bat1} and r_{bat2}). Additionally, semiconductors S_a and S_b provide isolation for Cuk1 in the event of a detected fault, ensuring fault tolerance.

In the context of multiple BESS units under operation,

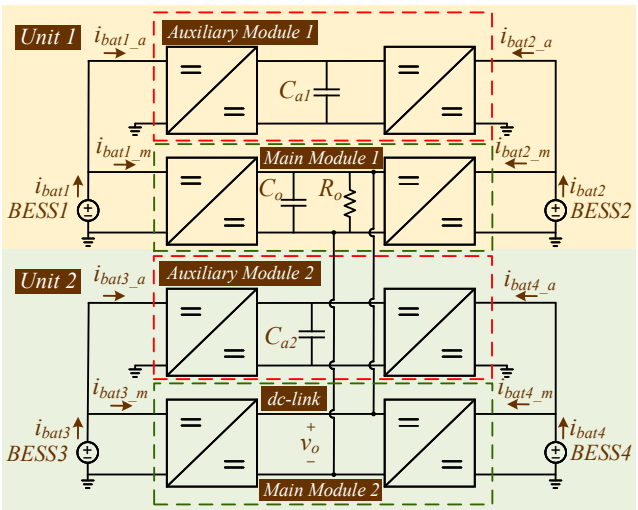

FIGURE 3. Connection of the redundancy-based cascaded bidirectional dc/dc converter to receive 4 BESS units.

the proposed topology could be connected to a similar unit through the main dc-link, for example, Fig. 3 indicates the connection of two power converters operating altogether in the dc-link. Thus, each pair of BESS units has a redundant auxiliary module, where the BESS unit current is $i_{bat\gamma}$, which is split into $i_{bat\gamma\_a}$ (auxiliary module) and $i_{bat\gamma\_m}$ (main module), with γ ranging from 1 to 4 in the case of Fig. 3.

Taking into account 4 PWM signals for driving the active semiconductors, there are 16 possible sub-circuits (2^n with n being 4) with Table 1 indicating the state (closed or opened) of each semiconductor, resulting in 16 sub-circuits denoted by ✓ for closed and χ for opened semiconductors.

III. COMPARISON WITH OTHERS TOPOLOGIES

The proposed topology features a structure with two inputs to interface BESS units and an output that can interface with

TABLE 1. Operation of the semiconductors in each sub-circuit.

Sub-circuit	S_1	S_2	S_3	S_4	Amount of semiconductors closed
1	✓	✓	✓	✓	4
2	✓	✓	✓	χ	3
3	✓	✓	χ	✓	3
4	✓	χ	✓	✓	3
5	χ	✓	✓	✓	3
6	✓	✓	χ	χ	2
7	✓	χ	✓	χ	2
8	✓	χ	χ	✓	2
9	χ	✓	✓	χ	2
10	χ	✓	χ	✓	2
11	χ	χ	✓	✓	2
12	✓	χ	χ	χ	1
13	χ	✓	χ	χ	1
14	χ	χ	✓	χ	1
15	χ	χ	χ	✓	1
16	χ	χ	χ	χ	0

a dc load. Thus, in this case, these similarities could be compared to a non-isolated three-port dc/dc converter.

In general, the proposed approach is designed to coordinate the power production of BESS units, allowing for SoC equalization. Typically, three-port dc/dc converters are designed to receive power from a system where photovoltaic (PV) units operate together with BESS to deliver power to the loads, as indicated in the review of three-port dc/dc converters in [32], [33], with a rated power ranging from 15 W to 4.5 kW and a switching frequency from 15 kHz to 100 kHz. However, they are not designed to operate with redundant modules and usually do not receive two BESS units, thereby lacking SoC equalization, as exemplified in the systematic method to construct three-port converter in [34].

Although the proposed topology and three-port converters operate with two power sources and are able to supply dc loads, their applications are different considering the reliability of designing redundant modules. In addition, when compared with redundant power converters, the proposed topology shares some similarities in maintaining power flow during unpredictable events (such as faults in semiconductors), ensuring that the power flow continues and the dc load remains unaffected. However, redundant power converters are not designed to receive two dc sources or two BESS units to facilitate SoC equalization.

As the proposed topology is more related with power converters with redundant modules, the authors perform a comparison among the proposed structure and other relevant fault-tolerant topologies based on redundancy, as shown in Table 2. The module design of the converter structure is highlighted, whether it is in series, parallel, input-parallel, or input series, with output parallel or output series configurations. Moreover, the number of elements per module is indicated: the number of active semiconductors, diodes, inductances, and capacitors.

Also in Table 2 is defined whether the configuration presents an electrical common ground among each module, which can benefit the structure implementation, and indicates if the power converter is suitable for BESS, i.e., if it is bidirectional. Finally, the comparison with other redundant power converter topologies explores their applications, such as wind farm applications and automotive applications with vehicle-to-grid (V2G) and grid-to-vehicle (G2V).

Indeed, both families of power converters (three-port dc/dc converter and fault-tolerant topologies based on redundancy) are effective in their respective applications; however, they lack the capability to balance BESS units using a redundancy-based approach.

IV. STATE-SPACE MODEL

Considering Cuk1, Cuk2, and the CBB, each pair of semiconductors "S_1 and $\bar{S}_1$", "S_2 and $\bar{S}_2$", "S_3 and $\bar{S}_3$" and "S_4 and $\bar{S}_4$" are only affected by their respective sub-circuits. Specifically, S_1 affects Cuk1, S_2 affects Cuk2, and the CBB is directly influenced by S_3 and S_4. Hence, it is possible to model each structure independently and then calculate the complete model of the proposed topology. In this context, referring to Fig. 2, the authors derive the mathematical model of the redundancy-based dc/dc converter topology in (1).

$$\begin{aligned} \boldsymbol{x} &= \left[\boldsymbol{x_{cuk1}}\ \ \boldsymbol{x_{cuk2}}\ \ \boldsymbol{x_{cbc}}\ \ v_{Co}\right]^T, \\ \boldsymbol{u} &= \begin{bmatrix} v_{bat1} & v_{bat2} \end{bmatrix}^T, \\ \boldsymbol{y} &= \begin{bmatrix} i_{L1} & i_{L3} & i_{L5} & i_{L6} & v_o \end{bmatrix}^T \end{aligned} \tag{1}$$

Where $\boldsymbol{x_{cuk1}} = \begin{bmatrix} i_{L1} & i_{L2} & v_{C1} \end{bmatrix}^T$, $\boldsymbol{x_{cuk2}} = \begin{bmatrix} i_{L3} & i_{L4} & v_{C2} \end{bmatrix}^T$ and $\boldsymbol{x_{cbc}} = \begin{bmatrix} i_{L5} & i_{L6} & v_{C3} \end{bmatrix}^T$. Additionally, it is important to address that $i_{bat1} = i_{L1} + i_{L5}$ and $i_{bat2} = i_{L3} + i_{L6}$.

A. CUK1

The model with S_1 closed is defined in (2) to obtain $\dot{\boldsymbol{x}}_{\boldsymbol{1cuk1}}$ of Cuk1.

$$\begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{L_1}\left[v_{bat1} - r_{bat1}i_{bat1} + r_{S1}(i_{L2} - i_{L1}) - r_{L1}i_{L1}\right], \\ \frac{di_{L2}}{dt} &= \frac{1}{L_2}\left[-i_{L2}(r_{L2} + r_{C1}) - v_{C1} - r_{S1}(i_{L2} - i_{L1}) - \frac{R_o\left(v_{Co} + r_{Co}(i_{L2} + i_{L4})\right)}{R_o + r_{Co}}\right], \\ \frac{dv_{C1}}{dt} &= \frac{1}{C_1}i_{L2} \end{aligned} \tag{2}$$

In (3), $\dot{\boldsymbol{x}}_{\boldsymbol{2cuk1}}$ of Cuk1 are determined with S_1 opened.

$$\begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{L_1}\left[v_{bat1} - r_{bat1}i_{bat1} + r_{\bar{S}1}(i_{L2} - i_{L1}) - i_{L1}(r_{L1} + r_{C1}) - v_{C1}\right], \\ \frac{di_{L2}}{dt} &= \frac{1}{L_2}\left[-i_{L2}r_{L2} - r_{\bar{S}1}(i_{L2} - i_{L1}) - \frac{R_o\left(v_{Co} + r_{Co}(i_{L2} + i_{L4})\right)}{R_o + r_{Co}}\right], \\ \frac{dv_{C1}}{dt} &= \frac{1}{C_1}i_{L1} \end{aligned} \tag{3}$$

B. CUK2

$\dot{\boldsymbol{x}}_{\boldsymbol{1cuk2}}$ of Cuk2 are defined with S_2 closed in (4).

TABLE 2. Comparison of fault-tolerant structures with module redundancy for improved capability.

Method	Module design	Elements per module (switch/diode/inductor/capacitor)	Electrical common ground among module	Bidirectional	Application
[20]	series	4/0/2/2	yes	yes	electric vehicle applications (V2G and G2V)
[18]	input-parallel-output-parallel	4/0/1/3	yes	yes	automotive power systems
[28]	series or parallel forward	1/3/2/2	yes (for input-parallel-output-parallel)	no	not mentioned
[29]	input-parallel-output-series / phase shifted full bridge	4/4/1/1	no	no	medium-voltage dc (MVDC)
[30]	input-parallel-output-series / phase shifted full bridge	6/8/1/3	no	no	wind farm applications
[31]	input-series-output-parallel / phase shifted full bridge	4/4/1/2	no	no	subsea power distribution
This paper	two input-parallel, one output-parallel	4/0/4/3 (for CBC) and 4/0/2/1 (for CBB)	yes	yes	SoC balancing

$$\begin{aligned}
\frac{di_{L3}}{dt} &= \frac{1}{L_3}\left[v_{bat2} - r_{bat2}i_{bat2} + r_{S2}(i_{L4} - i_{L3}) - r_{L3}i_{L3}\right],\\
\frac{di_{L4}}{dt} &= \frac{1}{L_4}\left[-i_{L2}(r_{L4} + r_{C2}) - v_{C2} - r_{S2}(i_{L4} - i_{L3}) - \frac{R_o\left(v_{Co} + r_{Co}(i_{L2} + i_{L4})\right)}{R_o + r_{Co}}\right],\\
\frac{dv_{C2}}{dt} &= \frac{1}{C_2}i_{L4}
\end{aligned} \tag{4}$$

Considering S_2 opened, the $\dot{\boldsymbol{x}}_{\mathbf{2}\boldsymbol{cuk2}}$ of Cuk2 is calculated in (5).

$$\begin{aligned}
\frac{di_{L3}}{dt} &= \frac{1}{L_3}\left[v_{bat2} - r_{bat2}i_{bat2} + r_{\bar{S}2}(i_{L4} - i_{L3}) - i_{L3}(r_{L3} + r_{C2}) - v_{C2}\right],\\
\frac{di_{L4}}{dt} &= \frac{1}{L_4}\left[-i_{L4}r_{L4} - r_{\bar{S}2}(i_{L4} - i_{L3}) - \frac{R_o\left(v_{Co} + r_{Co}(i_{L2} + i_{L4})\right)}{R_o + r_{Co}}\right],\\
\frac{dv_{C2}}{dt} &= \frac{1}{C_2}i_{L3}
\end{aligned} \tag{5}$$

C. CBB

To obtain the CBB model, the authors turned-on S_3 and S_4 to get as result $\dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cbc}}$ in (6).

$$\begin{aligned}
\frac{di_{L5}}{dt} &= \frac{1}{L_5}\left[v_{bat1} - r_{bat1}i_{bat1} - i_{L5}(r_{L5} + r_{S3})\right],\\
\frac{di_{L6}}{dt} &= \frac{1}{L_6}\left[v_{bat2} - r_{bat2}i_{bat2} - i_{L6}(r_{L6} + r_{S4})\right],\\
\frac{dv_{C3}}{dt} &= 0
\end{aligned} \tag{6}$$

When the semiconductors S_3 is closed and S_4 is opened, $\dot{\boldsymbol{x}}_{\mathbf{2}\boldsymbol{cbc}}$ is defined in (7).

$$\begin{aligned}
\frac{di_{L5}}{dt} &= \frac{1}{L_5}\left[v_{bat1} - r_{bat1}i_{bat1} - i_{L5}(r_{L5} + r_{S3})\right],\\
\frac{di_{L6}}{dt} &= \frac{1}{L_6}\left[v_{bat2} - r_{bat2}i_{bat2} - i_{L6}(r_{L6} + r_{\bar{S}4}) - r_{C3}i_{L6} - v_{C3}\right],\\
\frac{dv_{C3}}{dt} &= \frac{1}{C_3}i_{L6}
\end{aligned} \tag{7}$$

Considering S_3 opened and S_4 closed, the $\dot{\boldsymbol{x}}_{\mathbf{3}\boldsymbol{cbc}}$ for the CBB is calculated in (8).

$$\begin{aligned}
\frac{di_{L5}}{dt} &= \frac{1}{L_5}\left[v_{bat1} - r_{bat1}i_{bat1} - i_{L5}(r_{L5} + r_{\bar{S}3}) - r_{C3}i_{L5} - v_{C3}\right],\\
\frac{di_{L6}}{dt} &= \frac{1}{L_6}\left[v_{bat2} - r_{bat2}i_{bat2} - i_{L6}(r_{L6} + r_{S4})\right],\\
\frac{dv_{C3}}{dt} &= \frac{1}{C_3}i_{L5}
\end{aligned} \tag{8}$$

Finally, switching off S_3 and S_4, it is calculated the $\dot{\boldsymbol{x}}_{\mathbf{4}\boldsymbol{cbc}}$ in (9).

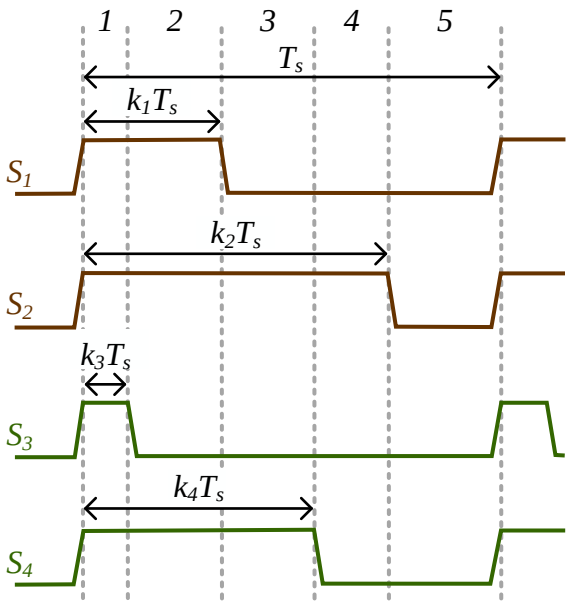

FIGURE 4. An illustrative example of switching.

$$\begin{aligned}
\frac{di_{L5}}{dt} &= \frac{1}{L_5}\left[v_{bat1} - r_{bat1}i_{bat1} - i_{L5}(r_{L5} + r_{\bar{S}3}) - r_{C3}(i_{L5} + i_{L6}) - v_{C3}\right],\\
\frac{di_{L6}}{dt} &= \frac{1}{L_6}\left[v_{bat2} - r_{bat2}i_{bat2} - i_{L6}(r_{L6} + r_{\bar{S}4}) - r_{C3}(i_{L5} + i_{L6}) - v_{C3}\right],\\
\frac{dv_{C3}}{dt} &= \frac{1}{C_3}(i_{L5} + i_{L6})
\end{aligned} \tag{9}$$

D. STATE-SPACE MATRICES FOR COUPLING THE DC/DC CONVERTERS

From the complete model, 16 sub-circuits are obtained, resulting in 16 sets of state-space matrices. The computation of $\dot{\boldsymbol{x}}$ involves combining $\dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cuk1}}$, $\dot{\boldsymbol{x}}_{\mathbf{2}\boldsymbol{cuk1}}$, $\dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cuk2}}$, $\dot{\boldsymbol{x}}_{\mathbf{2}\boldsymbol{cuk2}}$, $\dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cbc}}$, $\dot{\boldsymbol{x}}_{\mathbf{2}\boldsymbol{cbc}}$, $\dot{\boldsymbol{x}}_{\mathbf{3}\boldsymbol{cbc}}$, $\dot{\boldsymbol{x}}_{\mathbf{4}\boldsymbol{cbc}}$ and v_{Co} according to the modes of switching. Moreover, duty-cycles k_1, k_2, k_3, and k_4 are defined for S_1, S_2, S_3, and S_4, respectively.

To clarify the analysis, the authors consider an example in Fig. 4. Firstly, during sub-interval 1 (k_3T_s), all semiconductors are closed. In this scenario, $\dot{\boldsymbol{x}}_{\mathbf{1}}$ is given by $\dot{\boldsymbol{x}}_{\mathbf{1}} = \begin{bmatrix}\dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cuk1}} & \dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cuk2}} & \dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cbc}} & v_{Co}\end{bmatrix}^T$, and v_{Co} is determined by (10). Successively, evaluating sub-interval 2 with the period of $(k_1 - k_3)T_s$, sub-circuit 3 is obtained with S_1, S_2 and S_4 closed and S_3 opened to produce, therefore, $\dot{\boldsymbol{x}}_{\mathbf{3}} = \begin{bmatrix}\dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cuk1}} & \dot{\boldsymbol{x}}_{\mathbf{1}\boldsymbol{cuk2}} & \dot{\boldsymbol{x}}_{\mathbf{3}\boldsymbol{cbc}} & v_{Co}\end{bmatrix}^T$. Later, sub-circuit

10 is activated in sub-interval 3 with $(k_4 - k_1)T_s$, when S_2 and S_4 are turned on and S_1 and S_3 are off. The result of the aforementioned sequence of switching is $\dot{\boldsymbol{x}}_{\mathbf{10}} = \begin{bmatrix}\dot{\boldsymbol{x}}_{\mathbf{2cuk1}} & \dot{\boldsymbol{x}}_{\mathbf{1cuk2}} & \dot{\boldsymbol{x}}_{\mathbf{3cbc}} & v_{Co}\end{bmatrix}^T$.

$$\frac{dv_{Co}}{dt} = \frac{1}{C_o}\left[i_{L2} + i_{L4} - \frac{(v_{Co} + r_{Co}(i_{L2}+i_{L4}))}{R_o + r_{Co}}\right] \quad (10)$$

Subsequently, sub-interval 4 with the period of $(k_2 - k_4)T_s$ generates sub-circuit 13, with only S_2 activated, and $\dot{\boldsymbol{x}}_{\mathbf{13}} = \begin{bmatrix}\dot{\boldsymbol{x}}_{\mathbf{2cuk1}} & \dot{\boldsymbol{x}}_{\mathbf{1cuk2}} & \dot{\boldsymbol{x}}_{\mathbf{4cbc}} & v_{Co}\end{bmatrix}^T$. Finally, in the period $(1 - k_2)T_s$ all switches are opened (sub-interval 5), sub-circuit 16 is activated and $\dot{\boldsymbol{x}}_{\mathbf{16}} = \begin{bmatrix}\dot{\boldsymbol{x}}_{\mathbf{2cuk1}} & \dot{\boldsymbol{x}}_{\mathbf{2cuk2}} & \dot{\boldsymbol{x}}_{\mathbf{4cbc}} & v_{Co}\end{bmatrix}^T$ is obtained.

In addition, the state vectors $\dot{\boldsymbol{x}}_{\mathbf{1}}$, $\dot{\boldsymbol{x}}_{\mathbf{2}}$, ..., and $\dot{\boldsymbol{x}}_{\mathbf{16}}$ from the complete model can be obtained by combining Cuk1, Cuk2, and the CBB. This results in the state-space matrices $\boldsymbol{A_1}$, $\boldsymbol{A_2}$, ..., and $\boldsymbol{A_{16}}$, as well as the input matrices $\boldsymbol{B_1}$, $\boldsymbol{B_2}$, ..., and $\boldsymbol{B_{16}}$. Since v_{bat1} and v_{bat2} are common inputs for all sub-circuits (1 to 16), the input matrices for each sub-circuit are identical, i.e., $\boldsymbol{B} = \boldsymbol{B_1} = \boldsymbol{B_2} = \cdots = \boldsymbol{B_{16}}$.

E. OUTPUT MATRICES FOR COUPLING THE DC/DC CONVERTER

Considering the complete configuration of the redundancy-based dc/dc converter proposed, the output matrices $\boldsymbol{C}$ and $\boldsymbol{D}$ are the same for any switching mode, because the analytical model of v_o, defined in (11), does not change.

$$v_o = \frac{R_o}{(R_o + r_{Co})}\left[v_{Co} + r_{Co}(i_{L2} + i_{L4})\right] \quad (11)$$

V. STEADY-STATE ANALYSIS

Considering the switching operation, Cuk1 is directly influenced by k_1, Cuk2 by k_2 and the CBB by k_3 and k_4. In addition, as described before, the matrices $\boldsymbol{C}$ and $\boldsymbol{D}$ are the same for all switching operation. Thus, the state-space, that represent the complete model, is calculated in (12) and (13).

TABLE 3. Parameters of the redundancy-based cascaded bidirectional dc/dc converter.

Component	***Value***
Inductances from CBC (L_1, L_2, L_3, L_4)	4.8 mH
Inductances from CBB (L_5, L_6)	4.8 mH
C_1 and C_2	130 μF
C_3 and C_o	470 μF
Parasitic Losses	***Value***
$r_{L1} = r_{L2} = r_{L3} = r_{L4} = r_{L5} = r_{L6}$	150 $m\Omega$
$r_{S1} = r_{S2} = r_{S3} = r_{S4} = r_{\bar{S}1} = r_{\bar{S}2} = r_{\bar{S}3} = r_{\bar{S}4}$	30 $m\Omega$
$r_{C1} = r_{C2}$	30 $m\Omega$
$r_{C3} = r_{Co}$	150 $m\Omega$

$$\dot{\boldsymbol{x}} = \begin{bmatrix} \dot{\boldsymbol{x}}_{\mathbf{1cuk1}}k_1 + \dot{\boldsymbol{x}}_{\mathbf{2cuk1}}(1-k_1) \\ \dot{\boldsymbol{x}}_{\mathbf{2cuk2}}k_2 + \dot{\boldsymbol{x}}_{\mathbf{2cuk2}}(1-k_2) \\ \dot{\boldsymbol{x}}_{\mathbf{1cbc}}k_{cbc1} + \dot{\boldsymbol{x}}_{\mathbf{2cbc}}k_{cbc2} + \dot{\boldsymbol{x}}_{\mathbf{3cbc}}k_{cbc3} + \dot{\boldsymbol{x}}_{\mathbf{4cbc}}k_{cbc4} \\ v_{Co} \end{bmatrix} \quad (12)$$

$$\boldsymbol{y} = \boldsymbol{C}\boldsymbol{x} + \boldsymbol{D}\boldsymbol{u} \quad (13)$$

Where the coefficients k_{cbc1}, k_{cbc2}, k_{cbc3} and k_{cbc4} are calculate according to (14).

$$\begin{cases} k_{cbc1} = \dfrac{(k_3 + k_4) - |k_3 - k_4|}{2}, \\ k_{cbc2} = \dfrac{(k_3 - k_4) + |k_3 - k_4|}{2}, \\ k_{cbc3} = \dfrac{(k_4 - k_3) + |k_3 - k_4|}{2}, \\ k_{cbc4} = 1 - \dfrac{(k_3 + k_4) + |k_3 - k_4|}{2} \end{cases} \quad (14)$$

Based on the CBB switching, the duty-cycle values for S_3 and S_4 result in two situations. If $k_3 > k_4$, the following values are obtained: $k_{cbc1} = k_4$, $k_{cbc2} = k_3 - k_4$, $k_{cbc3} = 0$, and $k_{cbc4} = 1 - k_3$ (derived from (14)). Conversely, if $k_4 > k_3$, the values are: $k_{cbc1} = k_3$, $k_{cbc2} = 0$, $k_{cbc3} = k_4 - k_3$, and $k_{cbc4} = 1 - k_4$ (also derived from (14)). Using these values, (15) defines the coupled state-space model $\boldsymbol{A}$, with $A_{1,1}$, $A_{2,2}$, $A_{4,4}$, $A_{5,5}$, $A_{7,7}$, and $A_{8,8}$ presented in (16),

$$\boldsymbol{A} = \begin{bmatrix} A_{1,1} & \frac{k_1 r_{S1} + r_{\bar{S}1}(1-k_1)}{L_1} & -\frac{1-k_1}{L_1} & 0 & 0 & 0 & -\frac{r_{bat1}}{L_1} & 0 & 0 & 0 \\ \frac{k_1 r_{S1} + r_{\bar{S}1}(1-k_1)}{L_2} & A_{2,2} & -\frac{k_1}{L_2} & 0 & -\frac{R_o r_{Co}}{L_2(R_o + r_{Co})} & 0 & 0 & 0 & 0 & -\frac{R_o}{L_2(R_o + rco)} \\ \frac{1-k_1}{C_1} & \frac{k_1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & A_{4,4} & \frac{k_2 r_{S2} + r_{\bar{S}2}(1-k_2)}{L_3} & -\frac{1-k_2}{L_3} & 0 & -\frac{r_{bat2}}{L_3} & 0 & 0 \\ 0 & -\frac{R_o r_{Co}}{L_4(R_o + r_{Co})} & 0 & \frac{k_2 r_{S2} + r_{\bar{S}2}(1-k_2)}{L_4} & A_{5,5} & -\frac{k_2}{L_4} & 0 & 0 & 0 & -\frac{R_o}{L_4(R_o + r_{Co})} \\ 0 & 0 & 0 & \frac{1-k_2}{C_2} & \frac{k_2}{C_2} & 0 & 0 & 0 & 0 & 0 \\ -\frac{r_{bat1}}{L_5} & 0 & 0 & 0 & 0 & 0 & A_{7,7} & \frac{r_{C3}(k_3 + k_4 + |k_3 - k_4| - 2)}{2L_5} & -\frac{1-k_3}{L_5} & 0 \\ 0 & 0 & 0 & -\frac{r_{bat2}}{L_6} & 0 & 0 & \frac{r_{C3}(k_3 + k_4 + |k_3 - k_4| - 2)}{2L_6} & A_{8,8} & -\frac{1-k_4}{L_6} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-k_3}{C_3} & \frac{1-k_4}{C_3} & 0 & 0 \\ 0 & \frac{R_o}{C_o(R_o + r_{Co})} & 0 & 0 & \frac{R_o}{C_o(R_o + r_{Co})} & 0 & 0 & 0 & 0 & -\frac{1}{C_o(R_o + r_{Co})} \end{bmatrix} \quad (15)$$

$$\begin{aligned} A_{1,1} &= -\frac{(1-k_1)(r_{bat1} + r_{C1} + r_{L1} + r_{\bar{S}1}) + k_1(r_{bat1} + r_{L1} + r_{S1})}{L_1} \\ A_{2,2} &= -\frac{(1-k_1)}{L_2}\left(r_{L2} + r_{\bar{S}1} + \frac{R_o r_{Co}}{R_o + r_{Co}}\right) - \frac{k_1}{L_2}\left(r_{C1} + r_{L2} + r_{S1} + \frac{R_o r_{Co}}{R_o + r_{Co}}\right) \\ A_{4,4} &= -\frac{(1-k_2)(r_{bat2} + r_{C2} + r_{L3} + r_{\bar{S}2}) + k_2(r_{bat2} + r_{L3} + r_{S2})}{L_3} \\ A_{5,5} &= -\frac{(1-k_2)}{L_4}\left(r_{L4} + r_{\bar{S}2} + \frac{R_o r_{Co}}{R_o + r_{Co}}\right) - \frac{k_2}{L_4}\left(r_{C2} + r_{L4} + r_{S2} + \frac{R_o r_{Co}}{R_o + r_{Co}}\right) \\ A_{7,7} &= -\frac{r_{bat1} + r_{C3} + r_{L5} + r_{\bar{S}3} - k_3 r_{C3} + k_3 r_{S3} - k_3 r_{\bar{S}3}}{L_5} \\ A_{8,8} &= -\frac{r_{bat2} + r_{C3} + r_{L6} + r_{\bar{S}4} - k_4 r_{C3} + k_4 r_{S4} - k_4 r_{\bar{S}4}}{L_6} \end{aligned} \quad (16)$$

while the input matrix $\boldsymbol{B}$, and the output matrices $\boldsymbol{C}$ and $\boldsymbol{D}$ are defined in (17), (18) and (19), respectively.

$$\boldsymbol{B} = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{L_3} \\ 0 & 0 \\ 0 & 0 \\ \frac{1}{L_5} & 0 \\ 0 & \frac{1}{L_6} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{17}$$

$$\boldsymbol{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & \frac{R_o r_{Co}}{R_o + r_{Co}} & 0 & 0 & \frac{R_o r_{Co}}{R_o + r_{Co}} & 0 & 0 & 0 & 0 & \frac{R_o r_{Co}}{R_o + r_{Co}} \end{bmatrix} \tag{18}$$

$$\boldsymbol{D} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{19}$$

VI. EFFICIENCY ANALYSIS

In this section, the efficiency of the redundancy-based cascaded bidirectional dc/dc converter is evaluated according to the parasitic losses and parameters presented in Table 3, which include the parasitic losses $r_{L1}, r_{L2}, r_{L3}, r_{L4}, r_{L5}$, and r_{L6} representing the inductance losses; $r_{S1}, r_{\bar{S}1}, r_{S2}, r_{\bar{S}2}, r_{S3}, r_{\bar{S}3}, r_{S4}$, and $r_{\bar{S}4}$ as the semiconductor losses; and finally, r_{C1}, r_{C2}, r_{C3}, and r_{Co} representing the capacitance losses. Subsequently, the lab-scale prototype is designed using the same parameters from Table 3. To obtain the average value of the state and output vectors, the final value theorem is applied to the state-space model calculated in (12) and (13).

In this sense, according to the average voltages and currents from BESS1 and BESS2 (V_{bat1}, V_{bat2}, I_{bat1}, and I_{bat2}), the average values of the power flow through them are P_{bat1} and P_{bat2}, while the consumed power on the load is P_{load}, defined in (20).

$$\begin{cases} P_{bat1} = V_{bat1} I_{bat1} = V_{bat1}(I_{L1} + I_{L5}) \\ P_{bat2} = V_{bat2} I_{bat2} = V_{bat2}(I_{L3} + I_{L6}) \\ P_{load} = \frac{{V_o}^2}{R_o} \end{cases} \tag{20}$$

Thus, for the case where $P_{bat1} > 0$ and $P_{bat2} < 0$, the efficiency is shown in (21).

$$\eta = \frac{P_{load} - P_{bat2}}{P_{bat1}} \tag{21}$$

Assuming the case where $P_{bat1} > 0$ and $P_{bat2} > 0$, the efficiency is shown in (22).

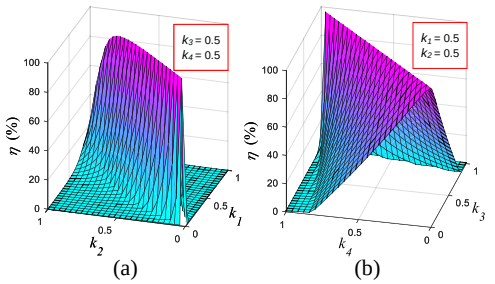

FIGURE 5. Influence of duty-cycles on the efficiency of the redundancy-based cascaded bidirectional dc/dc converter at a constant load ($R_o = 24\,\Omega$). (a) Variation applied to k_1 and k_2 with $k_3 = k_4 = 0.5$. (b) Variation applied to k_3 and k_4 with $k_1 = k_2 = 0.5$.

$$\eta = \frac{P_{load}}{P_{bat1} + P_{bat2}} \tag{22}$$

As the BESS units can deliver or receive power, as indicated by (23), P_{bat1in} and P_{bat2in} are defined for the power received by BESS1 and BESS2, respectively, while $P_{bat1out}$ and $P_{bat2out}$ represent the output power of BESS1 and BESS2, respectively.

$$\begin{cases} P_{bat1in} = 0.5(P_{bat1} + |P_{bat1}|) \\ P_{bat2in} = 0.5(P_{bat2} + |P_{bat2}|) \\ P_{bat1out} = 0.5(P_{bat1} - |P_{bat1}|) \\ P_{bat2out} = 0.5(P_{bat2} - |P_{bat2}|) \end{cases} \tag{23}$$

Thus, if P_{bat1} and $P_{bat2} > 0$, then $P_{bat1in} = P_{bat1}$ and $P_{bat2in} = P_{bat2}$, which implies that the BESS units are supplying power, and $P_{bat1out} = 0$ and $P_{bat2out} = 0$. Conversely, when the BESS units are absorbing power with P_{bat1} and $P_{bat2} < 0$, the results of (23) are $P_{bat1in} = 0$, $P_{bat2in} = 0$, $P_{bat1out} = P_{bat1}$, and $P_{bat2out} = P_{bat2}$.

Finally, the efficiency of the redundancy-based cascaded bidirectional dc/dc converter can be calculated as shown in (24), where P_{in} is the total power supplied and P_{out} is the power consumed.

$$\eta = \frac{P_{load} - 0.5(P_{bat1} - |P_{bat1}|) - 0.5(P_{bat2} - |P_{bat2}|)}{0.5(P_{bat1} + |P_{bat1}|) + 0.5(P_{bat2} + |P_{bat2}|)} = \frac{P_{out}}{P_{in}} \tag{24}$$

From (24), the efficiency is evaluated with different duty-cycles, considering the average values of the output vector $\boldsymbol{y}$. In this context, each surface in Fig. 5 and Fig. 6 is plotted as a function of two duty-cycles, while the others are maintained as constant, with the load R_o being 24 Ω.

In the case illustrated in Fig. 5(a), k_3 and k_4 are fixed at 0.5, with k_1 and k_2 varied between 0 and 1. The region of high efficiency (close to 100%) is achieved when $k_1 = k_2$. In Fig. 5(b), the high-efficiency region for the case with $k_1 = k_2 = 0.5$ is obtained with $k_3 = k_4$. The efficiency outside the high-efficiency region decreases faster in the first case than in the second.

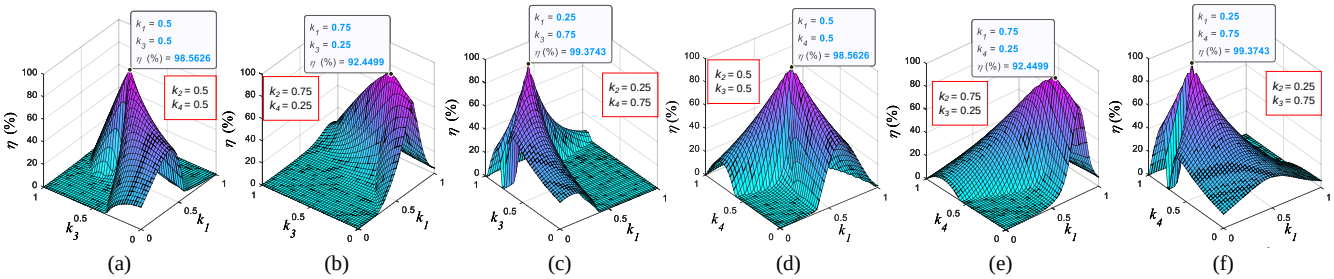

FIGURE 6. Influence of duty-cycles on the redundancy-based cascaded bidirectional dc/dc converter efficiency at a constant load ($R_o = 24\,\Omega$). (a) Variation applied to k_1 and k_3 with $k_2 = k_4 = 0.5$. (b) Variation applied to k_1 and k_3 with $k_2 = 0.75$ and $k_4 = 0.25$. (c) Variation applied to k_1 and k_3 with $k_2 = 0.25$ and $k_4 = 0.75$. (d) Variation applied to k_1 and k_4 with $k_2 = k_3 = 0.5$. (e) Variation applied to k_1 and k_4 with $k_2 = 0.75$ and $k_3 = 0.25$. (f) Variation applied to k_1 and k_4 with $k_2 = 0.25$ and $k_3 = 0.75$.

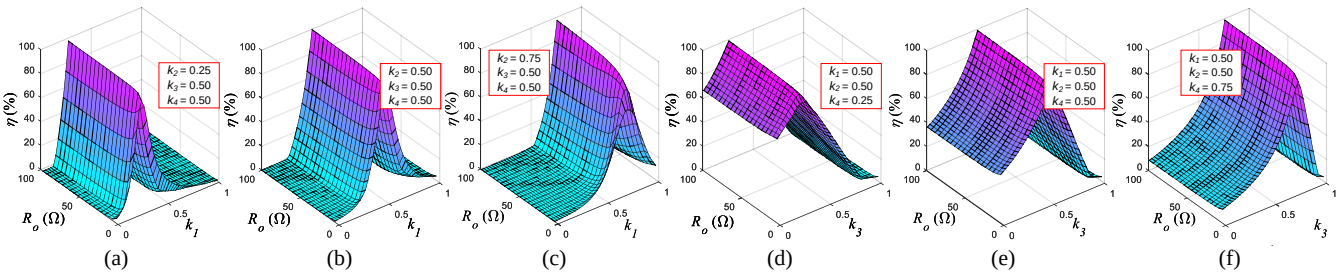

FIGURE 7. Influence of duty-cycles and the load R_o on the the redundancy-based cascaded bidirectional dc/dc converter efficiency. (a) Variation applied to k_1 and R_o with $k_2 = 0.25$ and $k_3 = k_4 = 0.5$. (b) Variation applied to k_1 and R_o with $k_2 = k_3 = k_4 = 0.5$. (c) Variation applied to k_1 and R_o with $k_2 = 0.75$ and $k_3 = k_4 = 0.5$. (d) Variation applied to k_3 and R_o with $k_1 = k_2 = 0.5$ and $k_4 = 0.25$. (e) Variation applied to k_3 and R_o with $k_1 = k_2 = k_4 = 0.5$. (f) Variation applied to k_3 and R_o with $k_1 = k_2 = 0.5$ and $k_4 = 0.75$.

In Figs. 6(a), (b), and (c), a unique point of high efficiency ($> 92\%$) is presented. To obtain the aforementioned requirements, Fig. 6(a) sets $k_2 = k_4 = 0.5$ and (24) as a function of k_1 and k_3 (between 0 and 1) to achieve the highest efficiency ($\eta = 98.56\%$) when $k_1 = k_3 = 0.5$. The same procedure is performed in Fig. 6(b), where $k_2 = 0.75$ and $k_4 = 0.25$, and k_1 and k_3 are varied between 0 and 1 to yield the highest efficiency ($\eta = 92.45\%$) at $k_1 = 0.75$ and $k_3 = 0.25$. Finally, in Fig. 6(c), $k_2 = 0.25$ and $k_4 = 0.75$, and k_1 and k_3 are varied between 0 and 1 to achieve the greatest efficiency ($\eta = 99.37\%$) at $k_1 = 0.25$ and $k_3 = 0.75$.

A similar behavior is observed in Figs. 6(d), (e), and (f). Initially, in Fig. 6(d), $k_2 = k_3 = 0.5$ is fixed, and k_1 and k_4 are modified linearly (between 0 and 1) to achieve the maximum efficiency ($\eta = 98.56\%$) when $k_1 = k_4 = 0.5$. In Fig. 6(e), where $k_2 = 0.75$ and $k_3 = 0.25$, k_1 and k_4 are varied linearly between 0 and 1 to yield the highest efficiency ($\eta = 92.45\%$) at $k_1 = 0.75$ and $k_4 = 0.25$. Finally, in Fig. 6(f), $k_2 = 0.25$ and $k_3 = 0.75$ are fixed, and k_1 and k_4 are modified linearly between 0 and 1 to achieve the greatest efficiency ($\eta = 99.37\%$) at $k_1 = 0.25$ and $k_4 = 0.75$.

As the redundancy-based cascaded bidirectional dc/dc converter has a symmetrical configuration, the efficiency surfaces as functions of the pairs "k_1 and k_3" and "k_1 and k_4" should be similar to those of "k_2 and k_4" and "k_2 and k_3", respectively. As noted, the efficiency of the redundancy-based cascaded bidirectional dc/dc converter is higher with duty-cycles from the CBC, presenting similar values for k_1 and k_2, while the CBB should have k_3 similar to k_4.

Finally, the influence of the load R_o on the efficiency of the redundancy-based cascaded bidirectional dc/dc converter is studied. Fig. 7 shows each surface as a function of R_o and one duty-cycle, with the others set as constant. By analyzing the surfaces, the load variation does not imply any changes in the redundancy-based cascaded bidirectional dc/dc converter efficiency.

VII. CONTROL DESIGN AND SMALL-SIGNAL ANALYSIS

This section focuses on the small-signal analysis of the proposed dc/dc converter, which is crucial for evaluating its transfer function and designing closed-loop controllers. Although the converter is composed of classical topologies, it is necessary to develop a model that captures the complete interplay among them.

The small-signal model of the dc/dc converter is derived using the state-space matrices. Starting from the average model of the matrices $\boldsymbol{A}$ in (15) (with the parameters $A_{1,1}$, $A_{2,2}$, $A_{4,4}$, $A_{5,5}$, $A_{7,7}$, and $A_{8,8}$ in (16)), and the matrices $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ defined in (17), (18) and (19), it is obtained (25) by applying small-signal analysis with the second-order ($\hat{k}\hat{\boldsymbol{x}} << 1$) and dc terms ($\boldsymbol{AX} + \boldsymbol{BU} = 0$) neglected.

It is assumed that $k_3 > k_4$ to simplify $|k_3 - k_4|$ in the matrix $\boldsymbol{A}$, which does not impact on the system because the dc/dc converter is engineered to be symmetrical and the

controllers are designed without load on C_3. Therefore, the current i_{L5} is similar to $-i_{L6}$ (disregarding the power losses) and consequently k_3 tends to present the same value of k_4 and then, $|k_3 - k_4|$ would not have a significant impact in the final result of the state-space average calculated in (25).

$$\begin{aligned}\dot{\hat{\boldsymbol{x}}} =&(\boldsymbol{A_0} + \boldsymbol{A_{k_1}}K_1 + \boldsymbol{A_{k_2}}K_2 + \boldsymbol{A_{k_3}}K_3 + \boldsymbol{A_{k_4}}K_4)\hat{\boldsymbol{x}}+\\ &\boldsymbol{B\hat{u}} + \boldsymbol{A_{k_1}X}\hat{k}_1 + \boldsymbol{A_{k_2}X}\hat{k}_2 + \boldsymbol{A_{k_3}X}\hat{k}_3 + \boldsymbol{A_{k_4}X}\hat{k}_4,\\ \hat{\boldsymbol{y}} =&\boldsymbol{C}\hat{x} + \boldsymbol{D\hat{u}}\end{aligned} \tag{25}$$

From (25), $\boldsymbol{A_0}$ is the constant matrix of $\boldsymbol{A}$ with all duty-cycles set to zero, while $\boldsymbol{A_{k_1}}$, $\boldsymbol{A_{k_2}}$, $\boldsymbol{A_{k_3}}$ and $\boldsymbol{A_{k_4}}$ consider only the influence of k_1, k_2, k_3, k_4, respectively, as indicated in (26) .

$$\begin{aligned}&\lim_{(k_1,k_2,k_3,k_4)\to(0,0,0,0)} \boldsymbol{A} = \boldsymbol{A_0},\\ &\lim_{(k_1,k_2,k_3,k_4)\to(1,0,0,0)} \boldsymbol{A} = \boldsymbol{A_{k_1}},\\ &\lim_{(k_1,k_2,k_3,k_4)\to(0,1,0,0)} \boldsymbol{A} = \boldsymbol{A_{k_2}},\\ &\lim_{(k_1,k_2,k_3,k_4)\to(0,0,1,0)} \boldsymbol{A} = \boldsymbol{A_{k_3}},\\ &\lim_{(k_1,k_2,k_3,k_4)\to(0,0,0,1)} \boldsymbol{A} = \boldsymbol{A_{k_4}}\end{aligned} \tag{26}$$

Thus, after applying Laplace's transform on (25), the output $\hat{\boldsymbol{y}}(s)$ is defined in (27).

$$\begin{aligned}\hat{\boldsymbol{y}}(s) =&\boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}[\boldsymbol{B\hat{u}}(s) + \boldsymbol{F_1}\hat{k}_1(s) + \boldsymbol{F_2}\hat{k}_2(s) + \boldsymbol{F_3}\hat{k}_3(s) + \boldsymbol{F_4}\hat{k}_4(s)]\\ &+ \boldsymbol{D\hat{u}}(s)\end{aligned} \tag{27}$$

From (27), $\boldsymbol{F_i} = \boldsymbol{A_{k_i}}K_i$ with $i = 1, 2, 3$ and 4 then, the control-to-output transfer functions $\boldsymbol{G_{i_{L1}}}(s)$, $\boldsymbol{G_{i_{L3}}}(s)$, $\boldsymbol{G_{i_{L5}}}(s)$ and $\boldsymbol{G_{i_{L6}}}(s)$ are obtained from the small-signal model and defined in (28).

$$\begin{bmatrix}\boldsymbol{G_{i_{L1}}}(s)\\ \boldsymbol{G_{i_{L3}}}(s)\\ \boldsymbol{G_{i_{L5}}}(s)\\ \boldsymbol{G_{i_{L6}}}(s)\end{bmatrix} = \begin{bmatrix}\boldsymbol{C_{i_{L1}}}\\ \boldsymbol{C_{i_{L3}}}\\ \boldsymbol{C_{i_{L5}}}\\ \boldsymbol{C_{i_{L6}}}\end{bmatrix} \boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1} \begin{bmatrix}\boldsymbol{F_1}(s)\\ \boldsymbol{F_2}(s)\\ \boldsymbol{F_3}(s)\\ \boldsymbol{F_4}(s)\end{bmatrix} \tag{28}$$

Where,

$$\begin{bmatrix}\boldsymbol{C_{i_{L1}}} & \boldsymbol{C_{i_{L3}}} & \boldsymbol{C_{i_{L5}}} & \boldsymbol{C_{i_{L6}}}\end{bmatrix}^T = \begin{bmatrix}1 & 0 & 0 & 0 & 0\\ 0 & 1 & 0 & 0 & 0\\ 0 & 0 & 1 & 0 & 0\\ 0 & 0 & 0 & 1 & 0\end{bmatrix}.$$

A. ANALYSIS IN THE FREQUENCY DOMAIN

Additionally, later than calculating the control-to-output transfer function, the PI controllers are determined by tuning each control loop, individually. As the switching frequency is set to 10 kHz, the bandwidths for the controllers are adjusted at 1 kHz with a phase margin of 60.2° for $\boldsymbol{G_{i_{L1}}}(s)$ and $\boldsymbol{G_{i_{L3}}}(s)$ and 49.9° for $\boldsymbol{G_{i_{L5}}}(s)$ and $\boldsymbol{G_{i_{L6}}}(s)$. Therefore, Fig. 8 and Fig. 9 illustrate the frequency response at open-loop of the control-to-output transfer functions $\boldsymbol{G_{i_{L1}}}(s)$ and $\boldsymbol{G_{i_{L5}}}(s)$ along with their corresponding PI controllers $\left(\boldsymbol{G_{i_{L1}}}(s)P_{i_{L1}}(s)\right.$ and $\left.\boldsymbol{G_{i_{L5}}}(s)P_{i_{L5}}(s)\right)$.

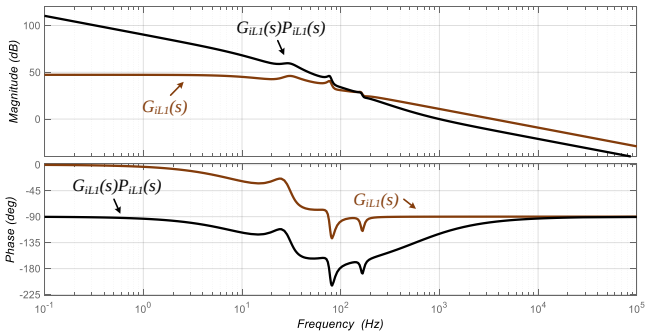

FIGURE 8. Open-loop frequency response for $\boldsymbol{G_{i_{L1}}}$ and $\boldsymbol{G_{i_{L1}}}(s)P_{i_{L1}}(s)$.

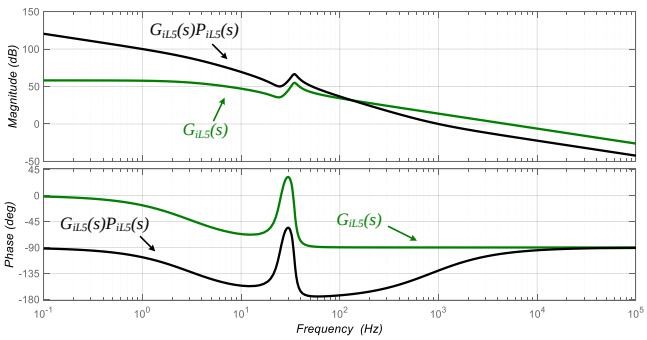

FIGURE 9. Open-loop frequency response for $\boldsymbol{G_{i_{L5}}}$ and $\boldsymbol{G_{i_{L5}}}(s)P_{i_{L5}}(s)$.

Considering Fig. 8, $\boldsymbol{G_{i_{L1}}}(s)$ shows gain of 50 dB and a phase displacement between 0° and -45° for frequencies lower than 30 Hz. However, when the frequency is increased (from 20 Hz up to 10 kHz) the authors visualize a resonance at 25 Hz, a decrement of -20 dB in the gain and a phase displacement that tends to 90°. In terms of $\boldsymbol{G_{i_{L1}}}(s)PI_{iL1}$, the gain is decreased at -20 dB in the entire range of frequency, while the phase starts from -90° at frequencies lower than 10 Hz, it goes to -225° between 10 Hz and 100 Hz and returns to -90° from 100 Hz up to 2 kHz.

In the analysis performed on Fig. 9, the authors consider $\boldsymbol{G_{i_{L5}}}(s)$ and $\boldsymbol{G_{i_{L5}}}(s)PI_{iL5}$, respectively. In general the behavior in the frequency domain is quite similar to the statements mentioned previously. The main difference is regarding the level of resonance, i.e., it is around 2 times higher in terms of gain and phase deviation when compared with Fig. 9, and observed at 35 Hz.

Additionally, as the PI controller for each PWM is designed by neglecting the other duty-cycles, the authors also propose stability analysis using infinity norm $\|H_\infty\|$ and Lyapunov's indirect method, as demonstrated in the next section.

VIII. STABILITY ANALYSIS

After the control design, it is necessary to evaluate the performance to ensure that the interaction among PI controllers for each inductance current i_{L1}, i_{L3}, i_{L5}, and i_{L6} remains stable during the operation of the redundancy-based

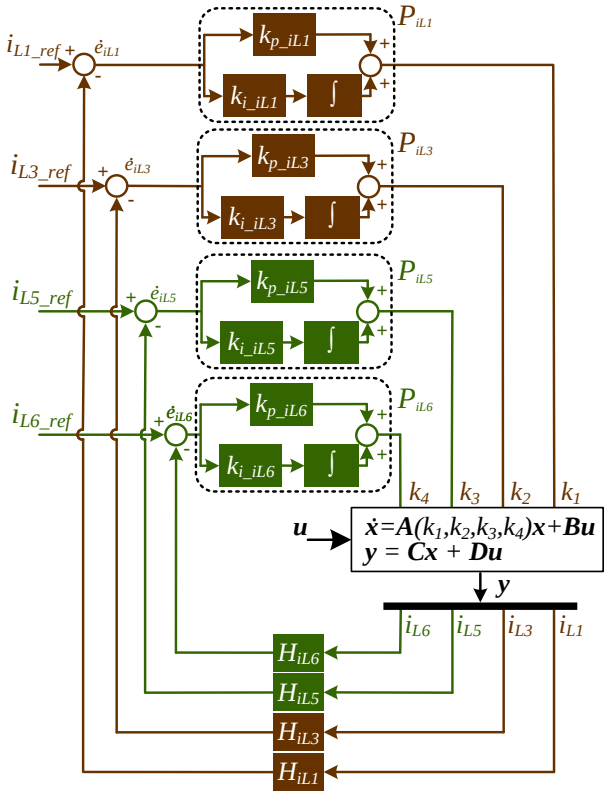

FIGURE 10. Diagram representing the interaction among the PI controllers in the average model.

bidirectional dc/dc converter. Thus, the interaction among CBC and CBB from the average model is indicated in (29), while Fig. 10 shows the complete diagram considering the closed-loop with k_{p_iLj} and k_{i_iLj} representing the proportional and integral gains for the PI_{iLj} controller, H_{iLj} the current sensor gains, $\dot{e}_{iLj}$ the errors of current and i_{Lj_ref} the current references calculated by a higher level of control with $j \in \Psi = \{1, 3, 5 \text{ and } 6\}$. In this context, subsection VIII-A defines the evaluation of closed-loop performance for each inductance current i_{L1}, i_{L3}, i_{L5}, and i_{L6} and the dc-link voltage v_o response over the load current disturbances i_o. Later, the eigenvalue movements derived from the Jacobian's matrix solution in (29) is evaluated in subsection VIII-B.

$$\begin{bmatrix} \dot{\boldsymbol{x}} \\ \dot{e}_{iL1} \\ \dot{e}_{iL3} \\ \dot{e}_{iL5} \\ \dot{e}_{iL6} \end{bmatrix} = \begin{bmatrix} \boldsymbol{A}(k_1,k_2,k_3,k_4)\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \\ i_{L1\_ref} - H_{iL1} i_{L1} \\ i_{L3\_ref} - H_{iL3} i_{L3} \\ i_{L5\_ref} - H_{iL5} i_{L5} \\ i_{L6\_ref} - H_{iL6} i_{L6} \end{bmatrix} \tag{29}$$

A. EVALUATION OF CLOSED-LOOP PERFORMANCE

Since the control design neglects the interaction among PI controllers in the redundancy-based bidirectional dc/dc converter, the authors applied the infinity norm $\|H_\infty\|$ to evaluate the closed-loop performance in the complete average model. To begin, the state-space representation considering the closed-loop performance $\boldsymbol{x}_{CL}$ is defined in (30).

$$\boldsymbol{x}_{CL} = [\boldsymbol{x}, e_{iL1}, e_{iL3}, e_{iL5}, e_{iL6}] \tag{30}$$

Subsequently, the closed-loop state-space model matrix $\boldsymbol{A}_{CL}$ is obtained in (31) from the Jacobian's matrix of the average model (29) over the state vector $\boldsymbol{x}_{CL}$.

$$\boldsymbol{A}_{CL} = \begin{bmatrix} \frac{\partial f1_x}{\partial x_1} & \frac{\partial f1_x}{\partial x_2} & \cdots & \frac{\partial f1_x}{\partial x_m} \\ \frac{\partial f2_x}{\partial x_1} & \frac{\partial f2_x}{\partial x_2} & \cdots & \frac{\partial f2_x}{\partial x_m} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial fn_x}{\partial x_1} & \frac{\partial fn_x}{\partial x_2} & \cdots & \frac{\partial fn_x}{\partial x_m} \end{bmatrix} \tag{31}$$

where m is the number of state-space variables. In sequence, the closed-loop input matrix $\boldsymbol{B}_{CL}$ is obtained in (32) from the Jacobian's matrix over the input vector $\boldsymbol{u}_{CL} = [v_{bat1}, v_{bat2}, i_o]$.

$$\boldsymbol{B}_{CL} = \begin{bmatrix} \frac{\partial f1_x}{\partial u_1} & \frac{\partial f1_x}{\partial u_2} & \cdots & \frac{\partial f1_x}{\partial u_k} \\ \frac{\partial f2_x}{\partial u_1} & \frac{\partial f2_x}{\partial u_2} & \cdots & \frac{\partial f2_x}{\partial u_k} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial fn_x}{\partial u_1} & \frac{\partial fn_x}{\partial u_2} & \cdots & \frac{\partial fn_x}{\partial u_k} \end{bmatrix} \tag{32}$$

with k being the total number of system inputs. Furthermore, the closed-loop output vector is defined in (33).

$$\boldsymbol{y}_{CL} = [i_{L1}, i_{L3}, i_{L5}, i_{L6}, v_o] \tag{33}$$

which can be represented as the model in (34).

$$\boldsymbol{y}_{CL} = \boldsymbol{C}_{CL}\boldsymbol{x}_{CL} + \boldsymbol{D}_{CL}\boldsymbol{u}_{CL} \tag{34}$$

The closed-loop output matrix $\boldsymbol{C}_{CL}$ has most elements as zero, except for those selecting the state-space variables that define the closed-loop output vector $\boldsymbol{y}_{CL}$. In sequence, the closed-loop feedforward matrix $\boldsymbol{D}_{CL}$ is a zero matrix with dimensions $k \times j$, where j represents the number of outputs.

Finally, a matrix of transfer functions can be obtained to represent the complete redundancy-based cascaded bidirectional dc/dc converter. The response $H(s)$ of the inductance currents i_{L1}, i_{L3}, i_{L5} and i_{L6} and dc-link voltage v_o over the load current i_o can then be used to evaluate the closed-loop performance.

Thus, the infinity norm $\|H_\infty\|$ is obtained according to

$$\|H(s)\|_\infty = \sup_{\omega \in \mathbb{R}} \|H(j\omega)\| \tag{35}$$

where $H(j\omega)$ denotes the frequency response of the system at frequency ω, and $\|\cdot\|$ represents the magnitude, with the *supremum* being the maximum magnitude of the transfer function's frequency response across all possible frequencies.

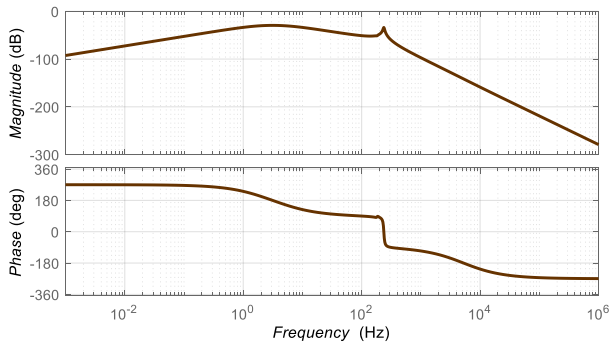

FIGURE 11. Bode diagram: closed-loop performance from the i_{L1} over the load current i_o.

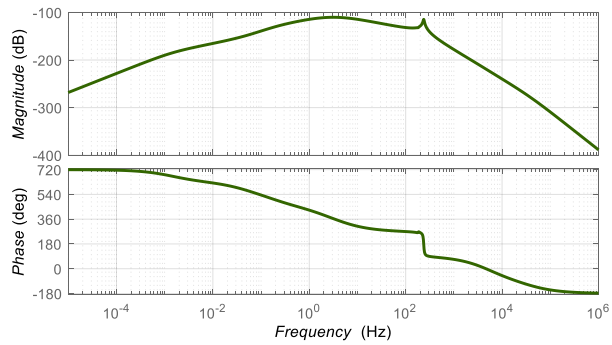

FIGURE 12. Bode diagram: closed-loop performance from the i_{L5} over the load current i_o.

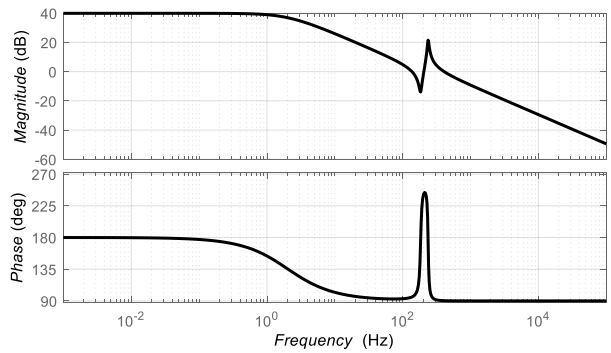

FIGURE 13. Bode diagram: closed-loop performance from the v_o over the load current i_o.

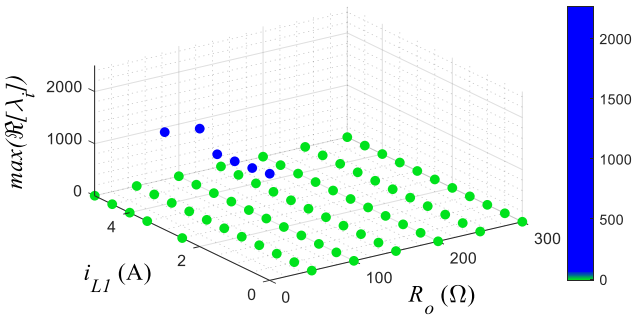

FIGURE 14. Maximum real part of the eigenvalues, $max(\Re[\lambda_i])$, considering i_{L1_ref} and R_o changing from 0 to 5 A and from 1 Ω to 300 Ω, while $i_{L5\_ref} = 5$ A.

1) Evaluation of i_{L1} and i_{L3} in the closed-loop

First of all, the frequency response $\frac{i_{L1}(s)}{i_o(s)}$ is shown in Fig. 11, with infinity norm $\left\| \frac{i_{L1}(s)}{i_o(s)} \right\|_\infty = 0.0338$. This is identical to the frequency response $\frac{i_{L3}(s)}{i_o(s)}$ due to the symmetry in the redundancy-based cascaded bidirectional dc/dc converter. Additionally, a generic system is stable when the infinity norm $\|H(s)\|_\infty < 1$, i.e., considering the proposed solution, the authors concluded that the PI controllers for i_{L1} and i_{L3} do not impact the output current i_o stability.

2) Evaluation of i_{L5} and i_{L6} in the closed-loop

In Fig. 12 is performed the frequency response $\frac{i_{L5}(s)}{i_o(s)}$ to evaluate the PI controller from i_{L5} over the output current i_o. In this type of analysis, the authors do not observe impact on the level of stability because its infinity norm is smaller than one, i.e., $\left\| \frac{i_{L5}(s)}{i_o(s)} \right\|_\infty = 3.0730 \times 10^{-6}$. Taking into account the frequency response $\frac{i_{L6}(s)}{i_o(s)}$, the result is identical as shown in Fig. 12, indicating that i_{L6} also exhibits stable performance with its infinity norm smaller than one.

3) Evaluation of v_o in the closed-loop

Fig. 13 shows the frequency response $\frac{v_o(s)}{i_o(s)}$ with the infinity norm greater than 1, as indicated by $\left\| \frac{v_o(s)}{i_o(s)} \right\|_\infty = 98.65$. Thus, the proposed solution maintains the stability, though the robustness is not guaranteed because v_o is affected by the R_o connected to the dc-link, which may exceed the rated power supported by the BESS units. Consequently, subsection VIII-B evaluates the stability analysis considering the R_o and the maximum inductance currents that the BESS units can support.

B. LYAPUNOV'S INDIRECT METHOD

This subsection evaluates the closed-loop stability of the proposed dc/dc converter via Lyapunov's Indirect Method. First of all, the equilibrium point is calculated from the solution of the complete average model in (29) which considers the effect of all PI controllers and the matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ defined in (15) and (17), respectively. In sequence, the eigenvalues are calculated from the Jacobian's matrix of the model shifted to the equilibrium point [26].

1) Movement of the Eigenvalues

The stability analyzes deviations in the current references i_{L1_ref} and i_{L5_ref} as well as in the load R_o connected to the dc-link. Thus, Fig. 14 shows that $R_o \leq 1\ \Omega$ may cause instability in the redundancy-based cascaded bidirectional dc/dc converter because the maximum real part of the eigenvalues, denoted as $max(\Re[\lambda_i])$, is positive. However, for $R_o > 1\ \Omega$, Fig. 14 indicates stable performance under load resistance and i_{L1} variation. Moreover, Fig. 15 shows

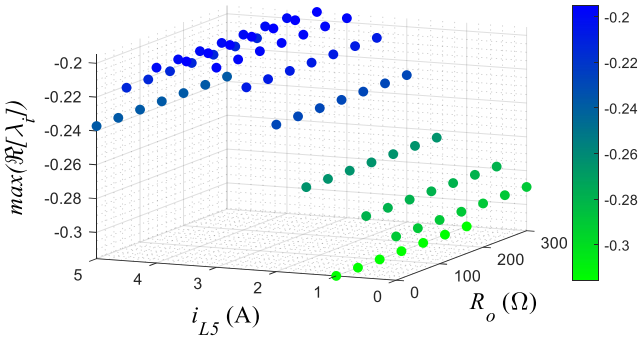

FIGURE 15. Maximum real part of the eigenvalues, $max(\Re[\lambda_i])$, performing i_{L5_ref} and R_o change from 0 to 5 A and 1 Ω to 300 Ω, while $i_{L1\_ref} = 5$ A.

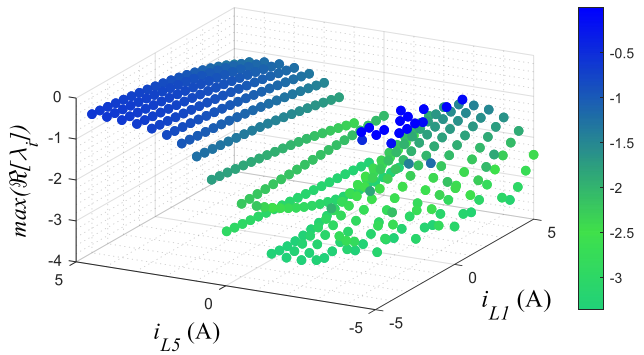

FIGURE 16. Maximum real part of the eigenvalues, $max(\Re[\lambda_i])$, making i_{L1_ref} and i_{L5_ref} move from 0 to -5 A and 0 to 5 A with $R_o = 200\ \Omega$.

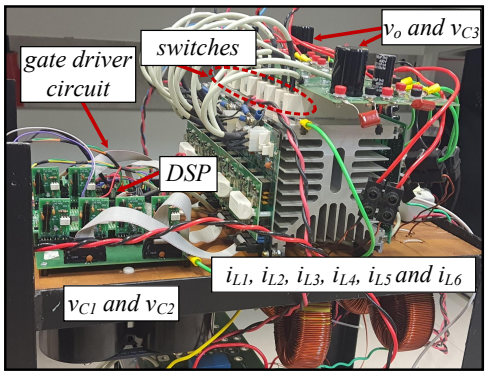

FIGURE 17. Lab-scale prototype.

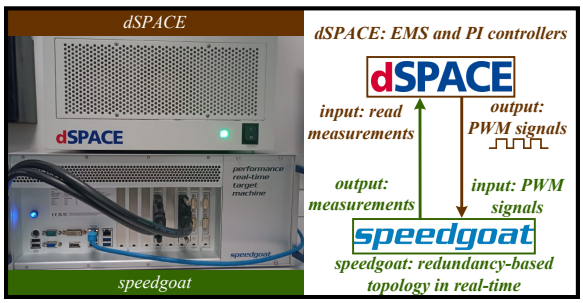

FIGURE 18. Interaction between Speedgoat platform and dSPACE system.

that modifying the resistance R_o together with i_{L5} does not impact the stability performance.

Additionally, when i_{L1} and i_{L5} tend to -5 A, the $max(\Re[\lambda_i])$ moves closer to the right side of the imaginary axis, reducing the stability margin as illustrated in Fig. 16. In this scenario, as there is a sweep involving the inductance currents i_{L1} and i_{L5} from -5 A to 5 A, the redundancy-based cascaded bidirectional dc/dc converter operates with the BESS1 ($i_{bat1} = i_{L1} + i_{L5}$) ranging from -10 A to 10 A and the fixed load of 200 Ω. Because of symmetry, the evaluation would present similar results considering the BESS2 unit and the inductance currents i_{L3} and i_{L6}. Thus, with $max(\Re[\lambda_i])$ being negative, it is concluded that this topology can operate with the fixed load (200 Ω), considering the maximum supplied/absorbed current (10 A) from the BESS units as defined in the experimental results. Using Lyapunov's Indirect Method, the authors conclude that the proposed dc/dc converter is stable for $R_o > 1\ \Omega$, i.e., this condition results in negative values for $max(\Re[\lambda_i])$.

IX. EXPERIMENTAL RESULTS

A laboratory-scale prototype was built to analyze the redundancy-based dc/dc converter shown in Fig. 2, using the parameters presented in Table 3 from Section VI. The setup is depicted in Fig. 17, where each converter input is connected to a battery pack with a rated capacity of 60 Ah. The maximum voltage reached is 36 V, and the maximum current supplied/absorbed is set as 10 A. The switching frequency is 10 kHz performed by STM32F407VG microcontroller with 32-bit core from STMicroelectronics. The authors also present a group of results achieved through the real-time hardware-in-the-loop (HIL) testing, which involved the interaction between the speedgoat platform (where the dc/dc converter is implemented) and the dSPACE system (where the control algorithms are integrated), as shown in Fig. 18. Additionally, the parameters used in the HIL as those applied to the lab-scale prototype, ensuring the feasibility of the tests.

A. COMPARISON BETWEEN EXPERIMENTAL RESULTS AND COMPUTATIONAL SIMULATIONS

For this analysis, the experimental results were obtained from the lab-scale prototype. In the first case, the waveforms are shown in Fig. 19 with the average values of $V_{bat1} = 26$ V, $V_{bat2} = 26$ V, $k_1 = 0.576$, $k_2 = 0.547$, $k_3 = 0.507$, $k_4 = 0.430$, and $R_o = 24\ \Omega$. In addition, there is a minimum error (less than 5%) in the variables i_{bat1}, i_{bat2}, i_{L1}, i_{L2}, i_{L3}, i_{L4}, i_{L5}, i_{L6}, v_{C1}, v_{C2}, v_{C3}, and v_o when compared with the computational simulation in Matlab/Simulink, as indicated in Fig. 20. In this result, it is observed that BESS1 ($i_{bat1} > 0$) is supplying power to BESS2 ($i_{bat2} < 0$), while i_{L1} and i_{L5} are positive and i_{L2} and i_{L6} are negative. Moreover, the power flow through Cuk2 is almost null because both i_{L3}

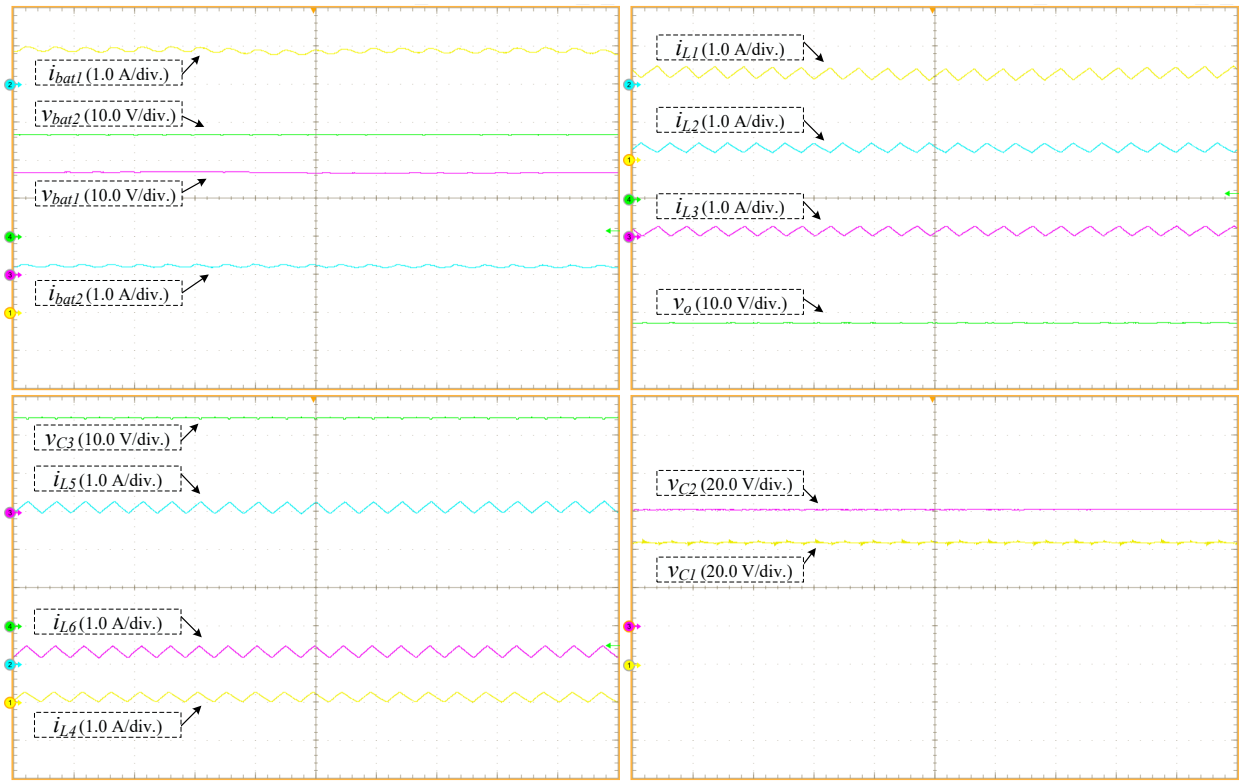

FIGURE 19. First case: experimental results with $k_1 = 0.576$, $k_2 = 0.547$, $k_3 = 0.507$, $k_4 = 0.430$ and $R_o = 24\ \Omega$. Time scale: 200 μs/div.

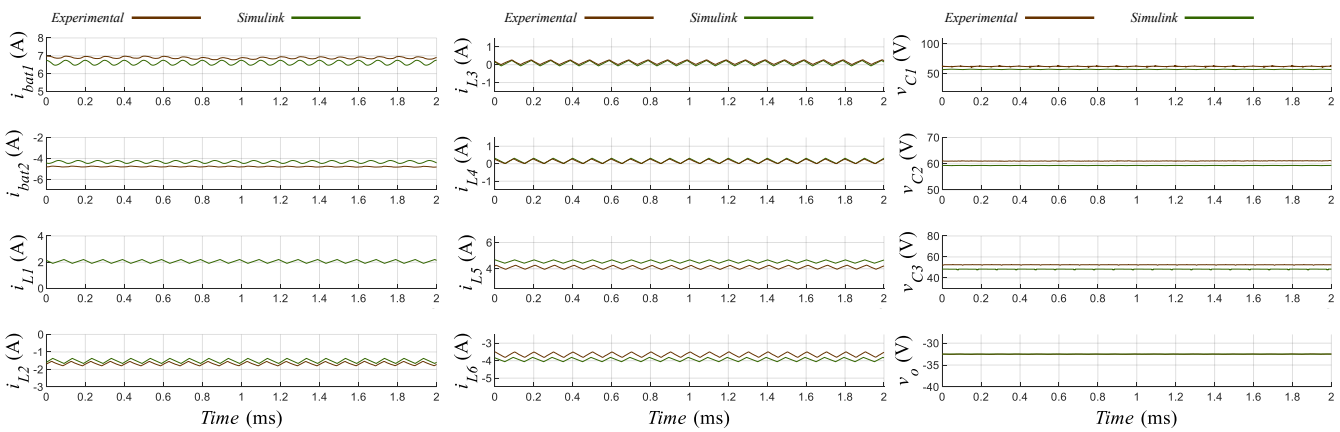

FIGURE 20. First case: experimental results versus computational simulations with $k_1 = 0.576$, $k_2 = 0.547$, $k_3 = 0.507$, $k_4 = 0.430$ and $R_o = 24\ \Omega$.

and i_{L4} are near of zero, i.e., Cuk1 supplies the load, while the bidirectional Boost converter supplies BESS2. On the capacitances C_o, C_1, C_2 and C_3, the voltages show low level of ripple, and $v_o < 0$ because of the main characteristic of Cuk converters.

Considering the second case, the experimental results are indicated in Fig. 21, with the same variables evaluated previously. The duty-cycles are set to $k_1 = 0.542$, $k_2 = 0.455$, $k_3 = 0.331$ and $k_4 = 0.280$, the sources V_{bat1} = 27.6V, V_{bat2} = 26.7V and the load $R_o = 24\ \Omega$. Furthermore, the comparison between the experimental results and computational simulations is shown in Fig. 22, where the tests also result in a minimum error (<5%). In this analysis, BESS1 ($i_{bat1} > 0$) is charging BESS2 ($i_{bat2} < 0$), while i_{L1} and i_{L4} are positive, i_{L2} and i_{L3} are negative and i_{L5} and i_{L6} are close to 0. Therefore, the CBB is only supplying its losses, Cuk1 is providing power for BESS2 and the load, while Cuk2 delivers power to BESS2. On the capacitances C_o, C_1, C_2 and C_3, the voltages show low level of ripple, with the first of them providing $v_o < 0$ because of the main characteristic of Cuk converters. Finally, the efficiency η for the first and second cases is indicated in Table 4.

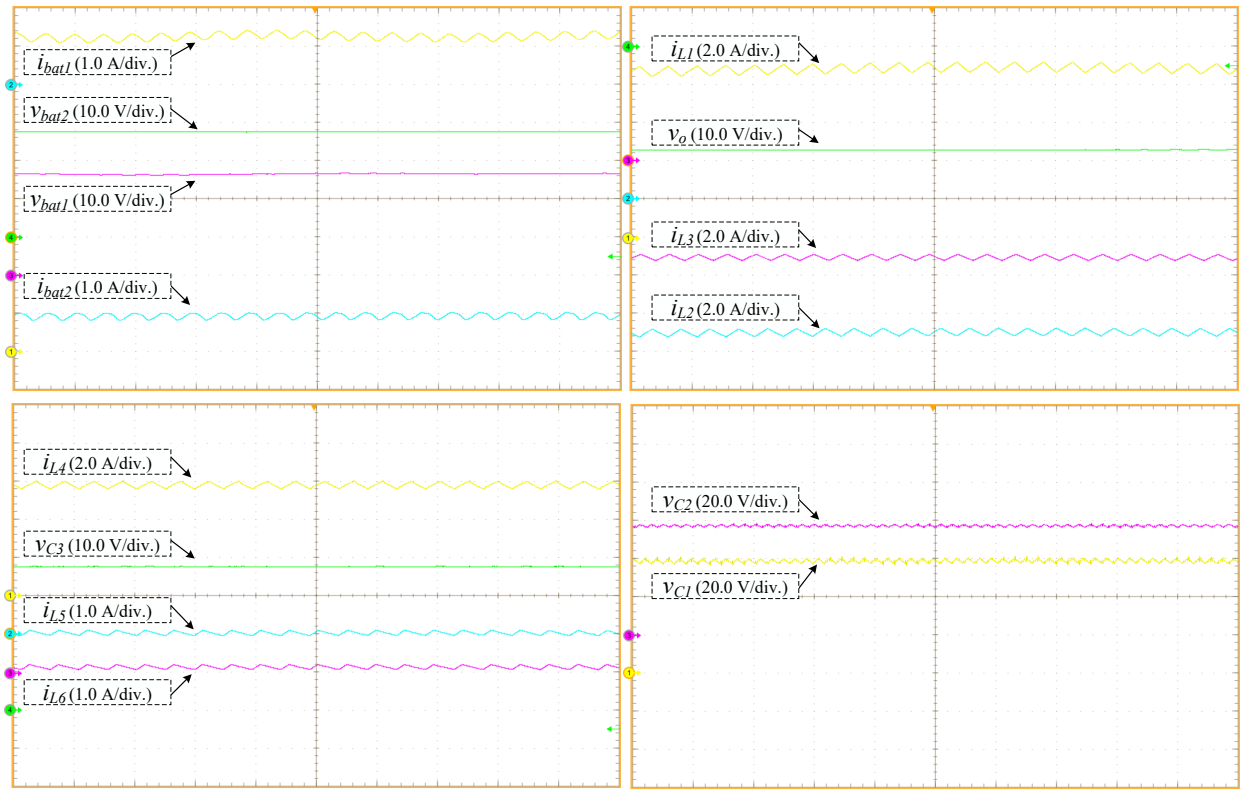

FIGURE 21. Second case: experimental results with $k_1 = 0.542$, $k_2 = 0.455$, $k_3 = 0.331$, $k_4 = 0.280$, $R_o = 24$. Time scale: 200 μs/div.

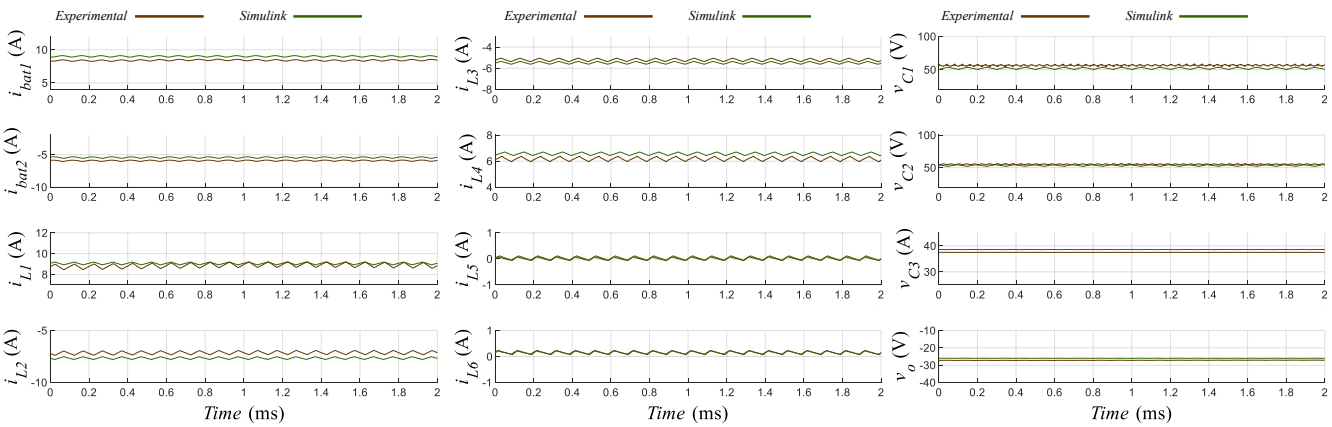

FIGURE 22. Second case: experimental results versus computational simulations with $k_1 = 0.542$, $k_2 = 0.455$, $k_3 = 0.331$, $k_4 = 0.280$ and $R_o = 24\ \Omega$.

TABLE 4. Efficiency of the experimental results in open-loop conditions.

	First Case	***Second Case***
P_{in}	172.38 W	221.74 W
P_{out}	155.50 W	195.31 W
η	90.21%	88.08%

B. CURRENT CONTROL AT CLOSED-LOOP

To evaluate the performance of the PI controllers at closed-loop, a set of current steps were performed on the current references as shown in Fig. 23, in the lab-scale prototype. Considering the first of them, named interval I, $i_{L1} = i_{L3} = i_{L5} = 5$ A and $i_{L6} = -5$ A. Later, during interval II, i_{L1} and i_{L3} were reduced from 5 A to 4 A and from 5 A to 3 A, while i_{L5} and i_{L6} remained at the same value. Finally, in interval III, i_{L1} and i_{L3} were not modified, while i_{L5} was decreased from 5 A to 3 A and the magnitude of i_{L6} from -5 A to -3 A.

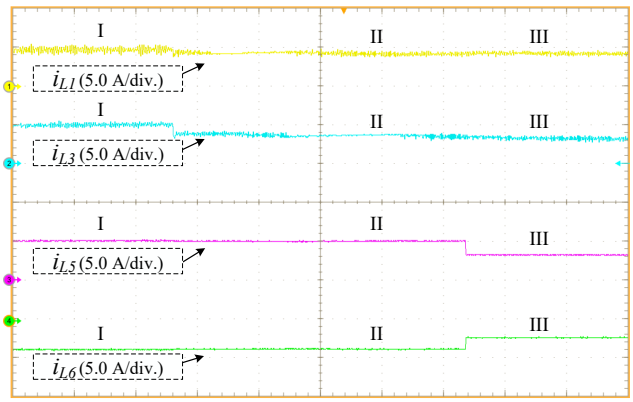

FIGURE 23. Redundancy-based dc/dc converter under current steps from top to bottom. Time scale: 1 s/div.

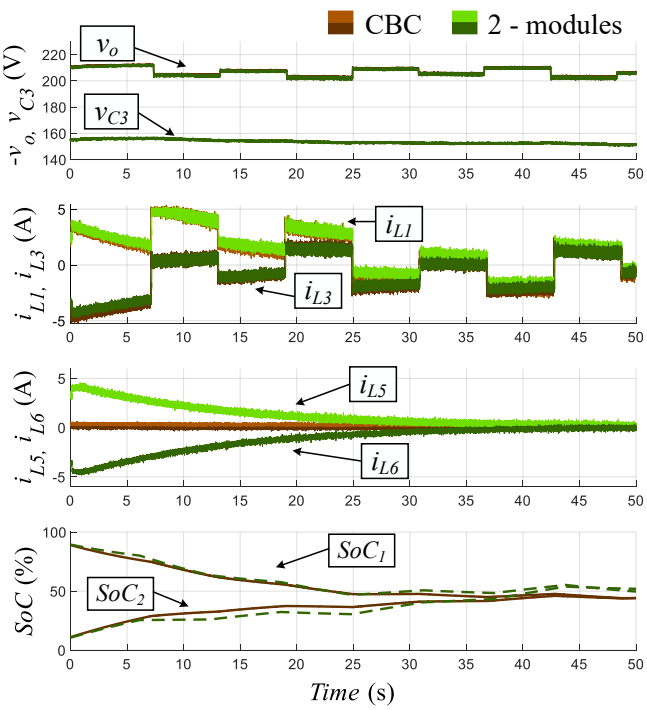

FIGURE 24. Incorporating the SoC-based droop from [25] to validate redundancy-based operation from top to bottom: dc-link voltage v_o, v_{C3}, current inductances i_{L1}, i_{L3}, i_{L5} and i_{L6} and the SoC balancing process, starting with SoC_1 = 90% and SoC_2 = 10%.

C. SOC-BASED DROOP APPLIED TO THE PROPOSED TOPOLOGY

This scenario, obtained in the HIL performance, evaluates the traditional SoC-based approach proposed by [25] to verify the SoC balancing in the redundancy-based dc/dc cascaded bidirectional converter with load steps of approximately 200 W. In this scenario, a utility grid is also connected to the proposed topology to deliver power when both BESS units require power for charging. The inductance current reference (i_{Lref}) is indicated in (36).

$$i_{L\_ref} = I_{max}\left[\frac{-v_{link} + v_{link\_ref} + \Delta v(\text{SoC} - 1)}{\Delta v}\right] \tag{36}$$

with $I_{max} = 5$ A being the maximum supported current in the inductance, v_{link} being the dc-link voltage (v_o for CBC and v_{C3} for CBB), v_{link_ref} being the rated voltage (220 V for CBC and 170 V for CBB), Δv being the voltage deviation for the SoC-based droop equalization (20 V), and SoC being SoC_1 for BESS1 and SoC_2 for BESS2.

Although for some applications the CBC without load can have bidirectional operation with the PWM signals from S_3 being complementary to $\bar{S}_4$ and $\bar{S}_3$ being complementary to S_4, the proposed topology is designed with different PWM signals for each pair of semiconductor. This is because the current reference will reach an equilibrium point according to v_{C3} and the SoCs of the BESS units, as per (37), with each reference being obtained from (36).

$$i_{L5\_ref}(SoC_1, v_{C3}) = -i_{L6\_ref}(SoC_2, v_{C3}) \tag{37}$$

1) Reliability of SoC equalization through both modules

In this scenario, Fig. 24 indicates the waveforms of the dc-link voltage v_o, v_{C3}, current inductances i_{L1}, i_{L3}, i_{L5}, and i_{L6} and the SoC balancing process, with the initial values of SoC_1 and SoC_2 being 90% and 10%, respectively. In this context, two equalization processes were evaluated: the first considers only the CBC operation, where the inductance currents i_{L5} and i_{L6} are 0 A, while the second method performs the equalization through both the CBB and CBC power modules. To become the analysis as fast as possible, the BESS capacities were reduced by a factor of 500 for the first method, and by 250 for the second analysis.

According to Fig. 24, the equalization process is improved with the CBB topology, as i_{L5} and i_{L6} operate without supplying a load. This allows for better equalization, resulting in SoC_1 and SoC_2 having slightly higher values compared to the situation with only CBC operation. As a result, the reliability of SoC balancing is enhanced, allowing the system to continue operating even if a module undergoes maintenance or experiences a fault.

2) Reliability of SoC equalization under power flow redirection to auxiliary module: stable dc-link voltage

In this case, the auxiliary module is responsible for redirecting the power flow from Cuk1 to CBB during the SoC equalization. Thus, Fig. 25 shows the SoC equalization process with initial SoCs from the BESS units being SoC_1 = 90% and SoC_2 = 60% under load steps of 200 W, with i_{L1} going to zero and the CBB (immediately) receiving the additional power flow, i.e., i_{L5} and i_{L6} transport the power flow from BESS1 to Cuk2, which then goes to the load. Additionally, i_{L3} is modified after the power flow redirection, receiving power not only from BESS2 but also from the CBB (BESS1). Furthermore, the dc-link voltage is affected by the load steps;

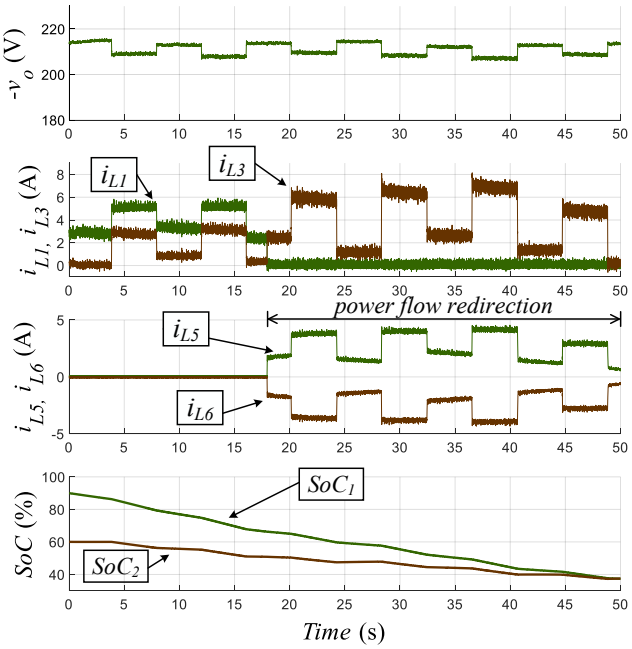

FIGURE 25. SoC equalization in the redundancy-based dc/dc converter with power flow redirection from Cuk1 to CBC, starting with SoC_1 = 90% and SoC_2 = 60%. From top to bottom: dc-link voltage v_o, current inductances i_{L1}, i_{L3}, i_{L5} and i_{L6} and the SoC balancing process (SoC_1 and SoC_2).

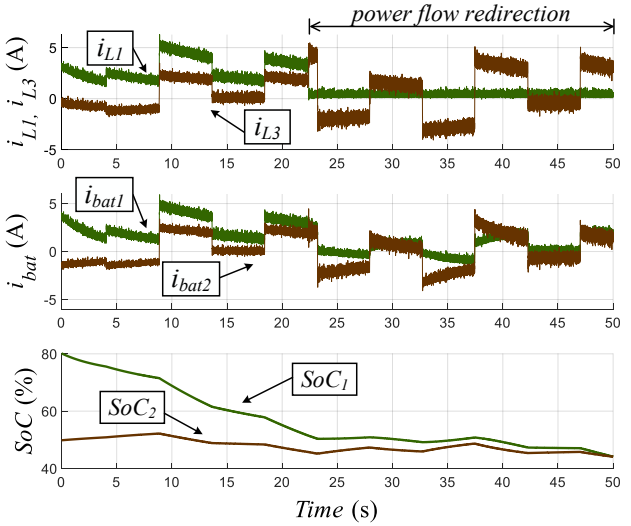

FIGURE 26. SoC equalization in the redundancy-based dc/dc converter with power flow redirection from Cuk1 to CBC, starting with SoC_1 = 80% and SoC_2 = 50%. From top to bottom: current inductances i_{L1} and i_{L3}, BESS units currents i_{bat1} and i_{bat2} and the SoC balancing process (SoC_1 and SoC_2).

however, it remains stable and is not modified by the power flow redirection at 18 s of elapsed time, as indicated in Fig. 25.

3) Reliability of SoC equalization under power flow redirection to auxiliary module: stable BESS units currents

For this scenario, Fig. 26 indicates that the power flow is redirected from Cuk1 to the CBB module at 22.5 s of elapsed time. In this mode of operation, i_{L1} goes to zero, while the power demand flows into the inductances L_5 and L_6. Later, the transport of the total power demanded goes to L_3 until it reaches the dc load. The BESS units' currents under load steps of 200 W remain stable and do not suffer a significant impact from the power flow redirection. Thus, the SoC equalization, which starts with SoC_1 = 80% and SoC_2 = 50%, is enhanced. Finally, the power flow redirection could be due to a fault in the Cuk1 or maintenance that requires the disconnection of this power converter.

X. CONCLUSION

This paper presented a redundancy-based cascaded bidirectional dc/dc converter which increase the reliability to interface BESS units. The proposed topology is a combination between CBC and CBB converters. Therefore, it is possible to model the complete system by considering each dc/dc converter separately. As result, the complete closed-loop state-space model can be derived from the set of equations that are interconnected. Additionally, the classical PI controllers are evaluated, and the infinity norm proves the stability among them, while Lyapunov's Indirect Method defines the limits of stability under different scenarios of load and power production.

The redundancy-based in the proposed topology is suitable for applications in shipboard, medical centers and aerospace system. As a result, the performance of a SoC equalization approach becomes more prominent in the event of a fault occurrence, enhancing overall reliability with a power flow redirection. Thus, the SoC balancing process can be enhanced with the auxiliary module operating with the SoC-based droop methodology, or it can be used as a standby module to redirect the power flow from the main module without affecting the BESS currents or the main dc-link voltage.

In this context, the experimental setup as well as, HIL analysis were carried out to validate the effectiveness of the proposed procedure. Finally, in potential future studies, the proposed topology will be developed with a methodology to detect faults in the operation of SoC equalization, and it will be integrated with other power converters to operate in a redundancy-based dc microgrid.

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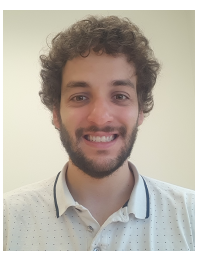

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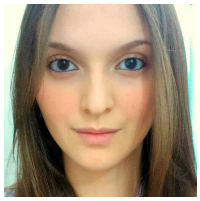

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