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Majorana-based transistor

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One of the most promising avenues to scalable fault-tolerant quantum computation is based on topological superconductors. (1-2) In such devices, logical operations are performed by exploring the non-Abelian statistics of its zero-energy excitations called Majorana bound states (MBSs). Interestingly, MBSs always come in pairs, due to parity conservation, and are localized at opposite sides of the superconductor, which provides remarkably robustness against local noise. In this work, we propose a Majorana-based transistor by exploring this (Majorana) nonlocality. To this end, we couple a Majorana wire to a quantum dot (QD), which is connected to two metallic leads (3), source and drain, and to a third lead at the other end of the wire, acting as the gate of the transistor. We calculate the density of states (DOS) on the dot and the transversal source-drain (across the QD) current, by calculating the retarded Green's function and the s-matrix, respectively. Our results show that the coupling to the "gate" lead, tunable with an electrostatic potential, controls the DOS on the dot and, consequently, the conductance. The mechanism that allows this control is the nonlocal nature of the MBSs wavefunctions and the hybridization between them. Our work provides a new direction to the control of edge states in multi-terminal devices via asymmetric coupling to metallic leads.

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