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A Comprehensive Non-Ideal Steady-State Analysis of a Threefold Operation Mode Interleaved-Based DC–DC Converter

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ABSTRACT Formerly in the literature, a new interleaved-based boost converter was devised for multiple input voltage sources purposes. Nevertheless, when only a single input voltage source is connected to the 2-phase version of this converter, it can be seen as a compact interleaved boost with voltage multiplier (cIBVM). A brief description of cIBVM operation as well as the ideal modeling are already discussed in the literature for one specific range of duty-cycle. In this paper, we provide further analysis by considering the conduction and dynamic losses on the analytical model with a single voltage source. Moreover, we also obtained the analytical model considering the entire duty-cycle range showing that the converter can perform either a quadratic, a double or even a symmetric voltage gain depending solely on the switching strategy adopted. The analytical model was obtained using state-space representation and both its accuracy and the effectiveness of the results were validated from a Simulink-based cross validation and a complete sequence of experimental tests.

INDEX TERMS DC–DC converters, high step-up conversion ratio, multiple operation modes.

I. INTRODUCTION

The DC–DC converters are devices that play a fundamental role in the proper operation of microgrids [1]–[3], electric vehicles [4], [5] and satellite applications [6], [7]. For this reason, many advanced studies that are entirely focused on either presenting a new topology or even better describing and exploring an existing topology in terms of modeling and non-ideal analyses have been appearing from the beginning of power electronics research [8], [9]. Within this frame of reference, it is important to state that the voltage gain and efficiency of the DC–DC converter under analysis are usually the performance relations that concentrate the most of the technological improvement effort and thus motivate the study [10].

Additionally, one of the most promising DC–DC converter topology reported in the literature is based on the well-known interleaved technique which ensures a large conversion ratio while providing high efficiency for components with reduced dimensions without compromising the DC–DC converter overall performance [11]–[13]. Moreover, interleaved-based DC–DC converters are more reliable when compared to non-interleaved types rated for the same power level owing to the increased number of power stages [14], reason why they are attractive for photovoltaic and fuel cells [15], [16].

The interleaved technique has been applied in many applications and can be used to supply voltage from low to medium/high power capabilities. In the low power end, for example, it has been seen the use of the interleaved technique in works such as [17], where the authors devised a converter rated for 7.7 W to be used in integrated circuits, and [18], where a step-down interleaved converter rated for 12.15 W was proposed for mobile low-power applications. Considering now the medium/high power end, other examples are the step-down interleaved converter rated for 500 W proposed

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in [19] as well as the work presented in [20] where the authors devised a 30 kW step-up interleaved converter for hybrid electric vehicles applications.

Apart from that, the interleaved technique can also be combined with other design strategies as was shown in the high step-up interleaved converter proposed by [21] which explores coupled-inductor and switched-capacitor techniques to improve performance for distribution generation systems.

In this context, in [22] and [23] Gules, Pfitscher and Franco integrated the idea of voltage multiplier cells with the interleaved technique and devised a new DC–DC converter topology, which was named as interleaved boost with voltage multiplier (IBVM), that is capable of delivering a conversion ratio reasonably larger than that of the conventional interleaved boost. In this way, the IBVM became a very attractive DC–DC converter solution to high-power applications, although a complete description was still missing in the literature. For this reason, in [16] Fuzato and his collegues elaborated a detailed work exploring the IBVM operation and non-ideal behavior from an extensive state-space model which enabled the authors to report more realistic static voltage gain and efficiency performances and also validate the modeling approach against a sequence of experimental results.

Following the same implementation concept, the DC–DC converter for multiple input voltage sources proposed in [24] by Zhou, Zhu and Luo can be seen as a reduced version of the IBVM, or else a compact IBVM (cIBVM). In terms of performance, the cIBVM develops the same conversion ratio, but on the other hand, in terms of topology it has the advantage of requiring three less components, thus being a better alternative to microgrid applications owing to the reduced manufacturing cost. In addition, cIBVM is an interleaved converter and it is naturally more reliable than single-phase converters.

For this reason, the cIBVM constitutes a more attractive DC–DC converter solution when compared to the conventional IBVM, and yet a complete description is not deeply explored in the literature, since the work initially presented by Zhou, Zhu and Luo addresses only an idealized modeling approach that does not provide a more complex and detailed evaluation of the non-ideal static voltage gain, the efficiency or even the effects of parasitic losses in the overall performance. Additionally, no analysis is given when the cIBVM is operating in a duty-cycle range lower than 50% ($0 \leq K < 0.5$), that is, the authors limit the study for high duty-cycle ($0.5 \leq K \leq 1$).

Differently from the study presented in [24], which is entirely based on ideal assumptions, in this paper we report a complete description of the 2-phase cIBVM operation and non-ideal behavior that is valid for both $0 \leq K < 0.5$ and $0.5 \leq K \leq 1$, configuring operation modes 1 and 2, respectively. In addition, we lay aside the interleaved technique and go further to also analyze even a third operation mode (operation mode 3) which is obtained by simply changing the switching strategy to a complementary switching that is valid for all K, in which case a different DC–DC converter with symmetric static voltage gain and high-efficiency is described.

The entire study is performed considering the three aforementioned operation modes which lead to three different non-ideal state-space models that include all the components parasitic conduction, switching and inductor core losses in continuous conduction mode (CCM). From these models, a detailed non-ideal analysis is performed to evaluate the parasitic resistive losses effects on the static voltage gain and the efficiency for each operation mode. The analytical model done is useful to design the converter. The accuracy of the obtained models and the effectiveness of the results are verified considering four test scenarios in which a Simulink-based cross validation and a complete sequence of experimental tests are performed.

In Section II, the ideal circuit description of the DC–DC converter presented in [24] and its basic operation are presented. The corresponding switching maps of both interleaved technique and complementary switching are given. In Section III, the non-ideal circuit description is presented and the state-space models of all feasible sub-circuits are obtained. In Section IV, these models are used to calculate the average models of the corresponding operation modes and in Section V an efficiency estimation is obtained based on conduction and dynamic power losses. A Simulink-based cross validation to verify the state-space models accuracy against a reference circuit is then presented in Section VI. In the sequence, a complete steady-state analysis in terms of static voltage gain is performed in Section VII. The experimental results are given in Section VIII. Finally, the conclusion of our work is presented in Section IX.

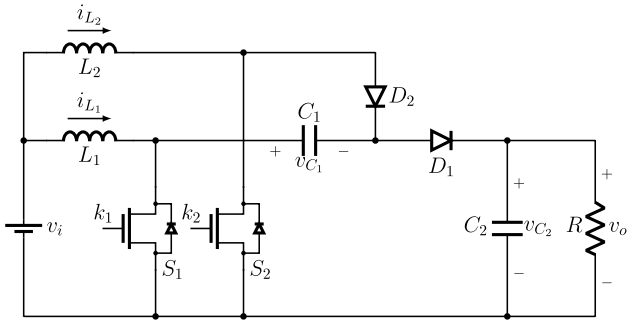

FIGURE 1. Compact IBVM proposed in [24].

II. CIRCUIT DESCRIPTION AND OPERATION MODES

The converter topology evaluated in this paper is a compact solution of the IBVM converter as is shown in Fig. 1. Considering the same illustration and according to [24], i_{L1} and i_{L2} represent the currents flowing through the inductors, L_1 and L_2, v_{C_1} and v_{C_2} are the voltages on the capacitors, C_1 and C_2, v_i and v_o are the input and output voltages, and R is the equivalent load placed on the converter terminals, respectively.

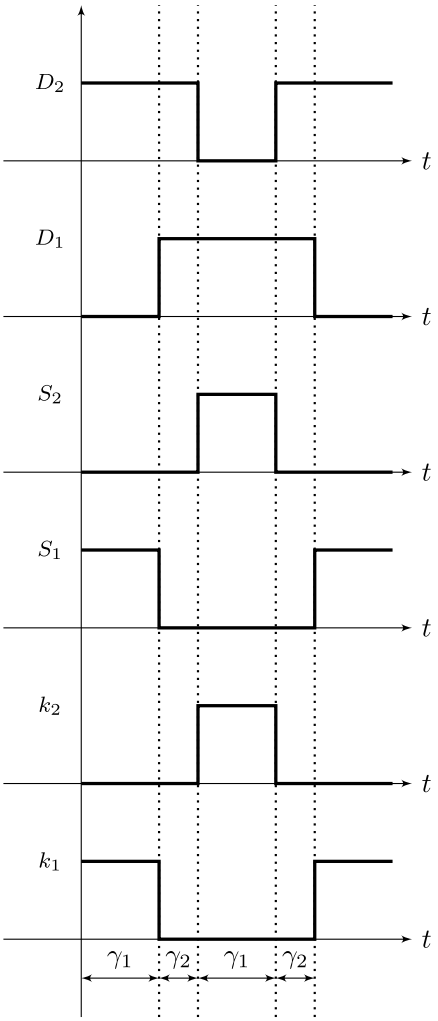

FIGURE 2. Switching map for $0 \leq K < 0.5$.

From Fig. 1, it can be noted that the cIBVM has a reduced number of components (semiconductors and storage devices), that is one capacitor and two diodes lesser than the conventional IBVM. Additionally, the topology requires four semiconductors, two controlled switches, S_1 and S_2, activated by the driving signals k_1 and k_2, and two diodes (non-active semiconductors), D_1 and D_2, respectively.

A. INTERLEAVED TECHNIQUE

In this converter, the interleaved technique can be employed by generating k_1 and k_2 with 180° of displacement and applying the same duty-cycle at steady-state regime (K) to both driving signals. Considering that the switching period is T_s and the switching frequency $f_s = 1/T_s$, let

$$\gamma_1 = KT_s, \ \gamma_2 = \left(\frac{1}{2} - K\right) T_s,$$
$$\gamma_3 = \left(K - \frac{1}{2}\right) T_s \text{ and } \gamma_4 = (1-K)T_s$$

then, the switching maps for sub-intervals $0 \leq K < 0.5$ and $0.5 \leq K \leq 1$ are showed in Figs. 2 and 3, respectively.

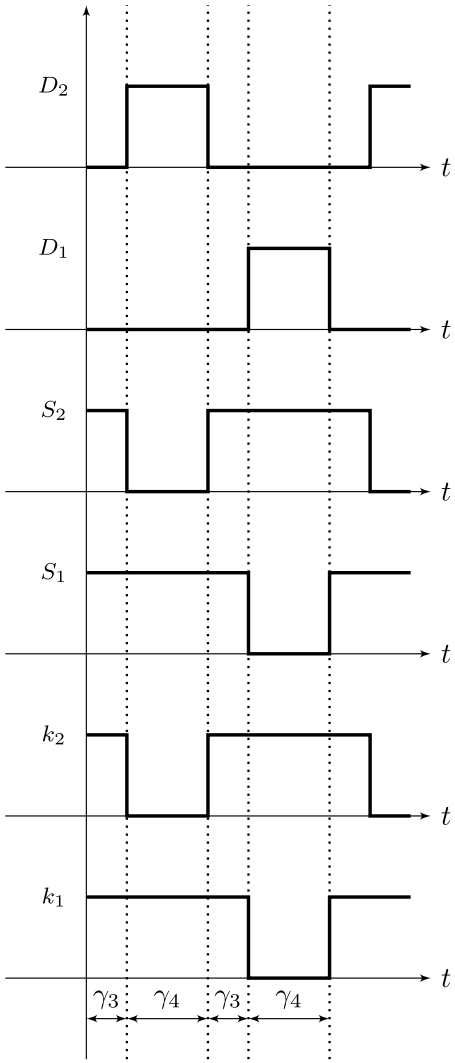

FIGURE 3. Interleaved technique switching map for $0.5 \leq K \leq 1$.

B. COMPLEMENTARY SWITCHING

In addition, the converter can also operate with the complementary switching. In this strategy, a duty-cycle K is applied to k_1, while the complement $1 - K$ is used in k_2, thus producing the switching map illustrated in Fig. 4.

C. FINAL REMARKS FOR THE SWITCHING PATTERN

Based on the waveform pattern demonstrated in Figs. 2, 3 and 4, it is possible to conclude that the DC–DC converter analyzed in this paper can be completely described according to only four sub-circuits regardless the switching strategy that is used. That being said, Table 1 presents the switch configuration that must be observed to represent each possible sub-circuit.

Taking into account the aforementioned arguments, in the next section the state-space model related to each sub-circuit is obtained.

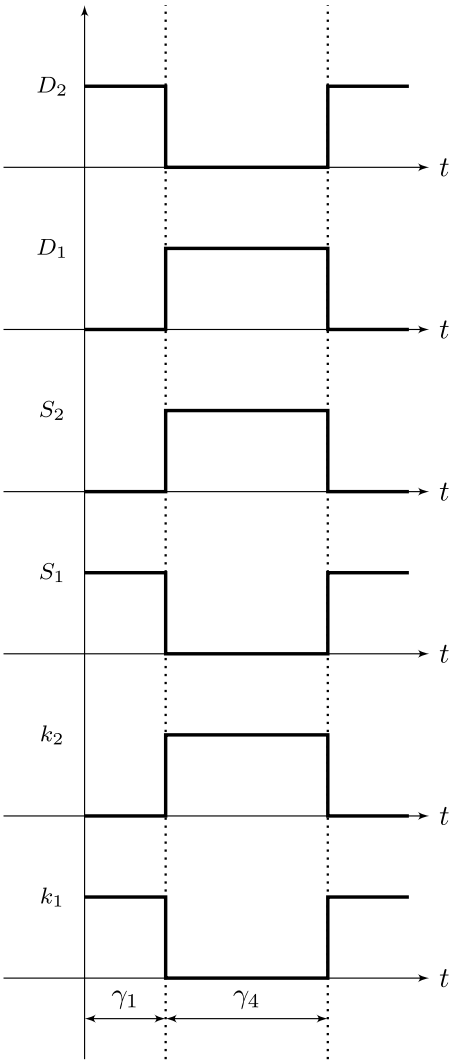

FIGURE 4. Switching map for the complementary operation mode.

TABLE 1. Switching pattern.

Sub-circuit	S_1	S_2	D_1	D_2
1	OFF	OFF	ON	ON
2	ON	OFF	OFF	ON
3	OFF	ON	ON	OFF
4	ON	ON	OFF	OFF

III. STATE-SPACE MODELING APPROACH

In order to analyze the converter efficiency as well as the non-ideal static voltage gain at steady-state regime, all the components parasitic conduction losses are included. Therefore, in the non-ideal circuit shown in Fig. 5, r_{L_1} and r_{L_2} are the conduction losses through inductors L_1 and L_2, r_{S_1}, r_{S_2}, r_{D_1} and r_{D_2} are the intrinsic resistances of semiconductors S_1, S_2, D_1 and D_2, and r_{C_1} and r_{C_2} are the equivalent series resistances (ESR) in capacitors C_1 and C_2, respectively. Moreover, v_{D_1} and v_{D_2} are the forward voltage drops in D_1 and D_2, respectively.

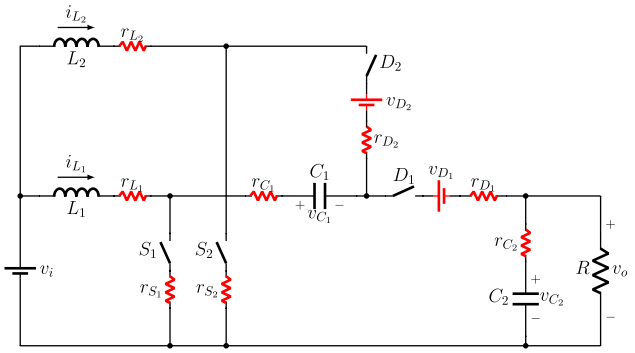

FIGURE 5. Non-ideal cIBVM converter.

In order to obtain the state-space representation for each possible sub-circuit in the next subsections, let us define the state vector ($\boldsymbol{x}$), the input vector ($\boldsymbol{u}$) and the output vector (y) as

$$\boldsymbol{x} = \begin{bmatrix} i_{L_1} & i_{L_2} & v_{C_1} & v_{C_2} \end{bmatrix}^T,$$
$$\boldsymbol{u} = \begin{bmatrix} v_i & v_{D_1} & v_{D_2} \end{bmatrix}^T, \quad y = v_o \text{ and } \dot{\boldsymbol{x}} = \frac{d\boldsymbol{x}}{dt}.$$

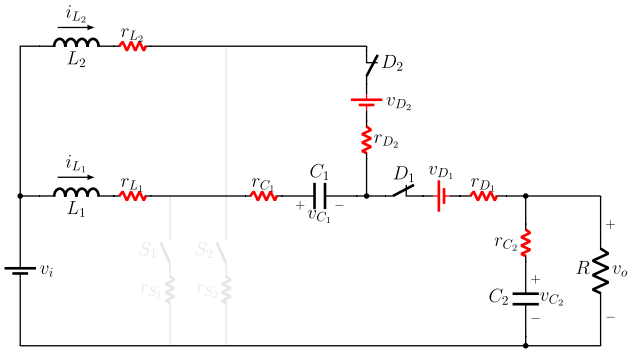

FIGURE 6. Sub-circuit 1.

A. SUB-CIRCUIT 1

Applying the Kirchhoff's laws in the sub-circuit of Fig. 6, we obtain

$$\dot{\boldsymbol{x}} = \boldsymbol{A_1}\boldsymbol{x} + \boldsymbol{B_1}\boldsymbol{u} \text{ and}$$
$$y = \boldsymbol{E_1}\boldsymbol{x},$$

where

$$\boldsymbol{A_1} = \begin{bmatrix} a_{1_1} & a_{1_2} & a_{1_3} & a_{1_4} \\ a_{1_5} & a_{1_6} & a_{1_7} & a_{1_8} \\ a_{1_9} & a_{1_{10}} & a_{1_{11}} & a_{1_{12}} \\ a_{1_{13}} & a_{1_{14}} & a_{1_{15}} & a_{1_{16}} \end{bmatrix},$$

$$\boldsymbol{B_1} = \begin{bmatrix} \frac{1}{L_1} & -\frac{1}{L_1} & 0 \\ \frac{1}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{ and}$$

$$\boldsymbol{E_1} = \begin{bmatrix} \frac{R\,r_{C_2}}{R+r_{C_2}} & \frac{R\,r_{C_2}}{R+r_{C_2}} & 0 & \frac{R}{R+r_{C_2}} \end{bmatrix}$$

with

$$a_{1_1} = \frac{R^2}{L_1\,(R+r_{C_2})} - \frac{R+r_{C_1}+r_{D_1}+r_{L_1}}{L_1},$$
$$a_{1_2} = \frac{R^2}{L_1\,(R+r_{C_2})} - \frac{R+r_{D_1}}{L_1},$$
$$a_{1_3} = -\frac{1}{L_1},\ a_{1_4} = -\frac{R}{L_1\,(R+r_{C_2})},$$
$$a_{1_5} = \frac{R^2}{L_2\,(R+r_{C_2})} - \frac{R+r_{D_1}}{L_2},$$
$$a_{1_6} = \frac{R^2}{L_2\,(R+r_{C_2})} - \frac{R+r_{D_1}+r_{D_2}+r_{L_2}}{L_2},$$
$$a_{1_8} = -\frac{R}{L_2\,(R+r_{C_2})},\ a_{1_9} = \frac{1}{C_1},$$
$$a_{1_{13}} = a_{1_{14}} = \frac{R}{C_2\,(R+r_{C_2})},\ a_{1_{16}} = -\frac{1}{C_2\,(R+r_{C_2})} \text{ and}$$
$$a_{1_7} = a_{1_{10}} = a_{1_{11}} = a_{1_{12}} = a_{1_{15}} = 0.$$

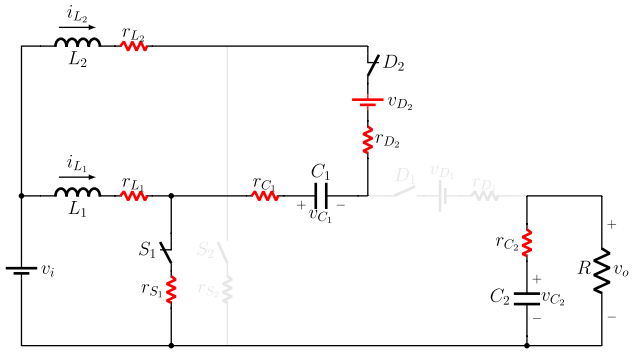

FIGURE 7. Sub-circuit 2.

B. SUB-CIRCUIT 2

Applying the Kirchhoff's laws in the sub-circuit of Fig. 7 yields to

$$\dot{\boldsymbol{x}} = \boldsymbol{A_2}\boldsymbol{x} + \boldsymbol{B_2}\boldsymbol{u} \text{ and}$$
$$y = \boldsymbol{E_2}\boldsymbol{x},$$

where

$$\boldsymbol{A_2} = \begin{bmatrix} -\frac{r_{L_1}+r_{S_1}}{L_1} & -\frac{r_{S_1}}{L_1} & 0 & 0 \\ -\frac{r_{S_1}}{L_2} & a_{2_6} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2\,(R+r_{C_2})} \end{bmatrix},$$

$$\boldsymbol{B_2} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ \frac{1}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{ and}$$

$$\boldsymbol{E_2} = \begin{bmatrix} 0\ 0\ 0 & \frac{R}{R+r_{C_2}} \end{bmatrix}.$$

with

$$a_{2_6} = -\frac{r_{C_1}+r_{D_2}+r_{L_2}+r_{S_1}}{L_2}.$$

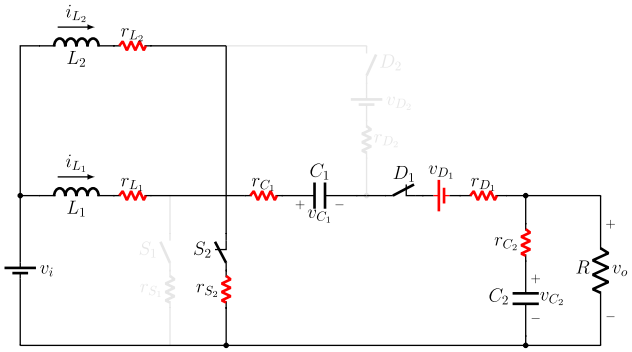

FIGURE 8. Sub-circuit 3.

C. SUB-CIRCUIT 3

In the third switching pattern, the corresponding sub-circuit is as illustrated in Fig. 8. Applying the Kirchhoff's laws results in

$$\dot{\boldsymbol{x}} = \boldsymbol{A_3}\boldsymbol{x} + \boldsymbol{B_3}\boldsymbol{u} \text{ and}$$
$$y = \boldsymbol{E_3}\boldsymbol{x},$$

where

$$\boldsymbol{A_3} = \begin{bmatrix} a_{3_1} & 0 & -\frac{1}{L_1} & -\frac{R}{L_1\,(R+r_{C_2})} \\ 0 & -\frac{r_{L_2}+r_{S_2}}{L_2} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{R}{C_2\,(R+r_{C_2})} & 0 & 0 & -\frac{1}{C_2\,(R+r_{C_2})} \end{bmatrix},$$

$$\boldsymbol{B_3} = \begin{bmatrix} \frac{1}{L_1} & -\frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{ and}$$

$$\boldsymbol{E_3} = \begin{bmatrix} \frac{R\,r_{C_2}}{R+r_{C_2}} & 0 & 0 & \frac{R}{R+r_{C_2}} \end{bmatrix}$$

with

$$a_{3_1} = \frac{R^2}{L_1\,(R+r_{C_2})} - \frac{R+r_{C_1}+r_{D_1}+r_{L_1}}{L_1}.$$

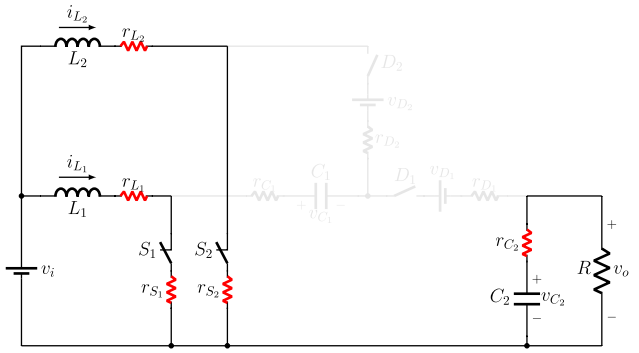

FIGURE 9. Sub-circuit 4.

D. SUB-CIRCUIT 4

Finally, applying the Kirchhoff's laws in the sub-circuit shown in Fig. 9, we obtain as result

$$\dot{\boldsymbol{x}} = \boldsymbol{A_4}\boldsymbol{x} + \boldsymbol{B_4}\boldsymbol{u} \text{ and}$$
$$y = \boldsymbol{E_4}\boldsymbol{x},$$

where

$$\boldsymbol{A_4} = \begin{bmatrix} -\dfrac{r_{L_1}+r_{S_1}}{L_1} & 0 & 0 & 0 \\ 0 & -\dfrac{r_{L_2}+r_{S_2}}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\dfrac{1}{C_2\left(R+r_{C_2}\right)} \end{bmatrix},$$

$$\boldsymbol{B_4} = \begin{bmatrix} \dfrac{1}{L_1} & 0 & 0 \\ \dfrac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{ and}$$

$$\boldsymbol{E_4} = \begin{bmatrix} 0 & 0 & 0 & \dfrac{R}{R+r_{C_2}} \end{bmatrix}.$$

With the complete state-space model for each switching sub-interval, it is possible to calculate the average models to obtain the static voltage gain and the efficiency for all considered operation modes.

IV. AVERAGE VOLTAGE GAIN MODELING

The converter has 3 different operation modes, which are:

1) Interleaved switching for $0 \leq K < 0.5$ (mode 1),
2) Interleaved switching for $0.5 \leq K \leq 1$ (mode 2),
3) Complementary switching (mode 3).

Let $q \in \{1, 2, 3\}$. Assuming $\bar{\boldsymbol{A}}_q$, $\bar{\boldsymbol{B}}_q$ and $\bar{\boldsymbol{E}}_q$ as average state-space matrices, for a generic operation mode q, we have an algebraic system as

$$0 = \bar{\boldsymbol{A}}_q\boldsymbol{X} + \bar{\boldsymbol{B}}_q\boldsymbol{U} \text{ and}$$
$$Y = \bar{\boldsymbol{E}}_q\boldsymbol{X}$$

such that the average value of the state variables ($\boldsymbol{X}$) and output ($Y = V_o$), as a function of average value of the input ($\boldsymbol{U} = \begin{bmatrix} V_i & V_{D_1} & V_{D_2} \end{bmatrix}^T$), are given by

$$\boldsymbol{X} = -\bar{\boldsymbol{A}}_q^{-1}\bar{\boldsymbol{B}}_q\boldsymbol{U} \text{ and} \quad (1)$$
$$Y = -\bar{\boldsymbol{E}}_q\bar{\boldsymbol{A}}_q^{-1}\bar{\boldsymbol{B}}_q\boldsymbol{U}. \quad (2)$$

Moreover, from (2), the static voltage gain (M_q) can be calculated as

$$M_q =: \frac{V_o}{V_i} = -\bar{\boldsymbol{E}}_q\bar{\boldsymbol{A}}_q^{-1}\bar{\boldsymbol{B}}_q\boldsymbol{U}V_i^{-1} \quad (3)$$

and the ideal static voltage gain is obtained by setting

$$r_{L_1} = r_{L_2} = r_{C_1} = r_{C_2} = r_{D_1} = r_{D_2} = r_{S_1} = r_{S_2} = 0$$

and

$$V_{D_1} = V_{D_2} = 0$$

in (3).

A. MODE 1

For this operation mode, from Section II, we have

$$\bar{\boldsymbol{A}}_1 = \boldsymbol{A}_1(1-2K) + \boldsymbol{A}_2K + \boldsymbol{A}_3K,$$
$$\bar{\boldsymbol{B}}_1 = \boldsymbol{B}_1(1-2K) + \boldsymbol{B}_2K + \boldsymbol{B}_3K \text{ and}$$
$$\bar{\boldsymbol{E}}_1 = \boldsymbol{E}_1(1-2K) + \boldsymbol{E}_2K + \boldsymbol{E}_3K.$$

1) NON-IDEAL GAIN

The ideal static voltage gain is

$$M_1 = \frac{m_{1_1}K^4 + m_{1_2}K^3 + m_{1_3}K^2 + m_{1_4}K + m_{1_5}}{m_{1_6}K^4 + m_{1_7}K^3 + m_{1_8}K^2 + m_{1_9}K + m_{1_{10}}} \quad (4)$$

where its coefficients are in Table 2.

2) IDEAL GAIN

Considering null the losses, the ideal voltage gain is given by

$$M_1 = \frac{1}{(1-K)^2},$$

i.e. the cIBVM converter operates with a quadratic voltage gain.

B. MODE 2

For this operation mode, from Section II, we have

$$\bar{\boldsymbol{A}}_2 = \boldsymbol{A_4}(2K-1) + \boldsymbol{A_2}(1-K) + \boldsymbol{A_3}(1-K),$$
$$\bar{\boldsymbol{B}}_2 = \boldsymbol{B_4}(2K-1) + \boldsymbol{B_2}(1-K) + \boldsymbol{B_3}(1-K) \text{ and}$$
$$\bar{\boldsymbol{E}}_2 = \boldsymbol{E_4}(2K-1) + \boldsymbol{E_2}(1-K) + \boldsymbol{E_3}(1-K).$$

1) NON-IDEAL GAIN

The non-ideal static voltage gain is

$$M_2 = \frac{m_{2_1}K^2 + m_{2_2}K + m_{2_3}}{m_{2_4}K^2 + m_{2_5}K + m_{2_6}} \quad (5)$$

and its coefficients are in Table 3.

TABLE 2. Coefficients of (4).

m_{1_1}	$-R^2 V_{D_1} - R^2 V_{D_2} - R r_{C_2} V_{D_1} - R r_{C_2} V_{D_2}$
m_{1_2}	$4R^2 V_{D_1} + 4R^2 V_{D_2} + 4R r_{C_2} V_{D_1} + 4R r_{C_2} V_{D_2}$
m_{1_3}	$R^2 V_i - 6R^2 V_{D_2} - 6R^2 V_{D_1} - 6R r_{C_2} V_{D_1} - 6R r_{C_2} V_{D_2} + R r_{C_2} V_i$
m_{1_4}	$4R^2 V_{D_1} + 4R^2 V_{D_2} - 2R^2 V_i + 4R r_{C_2} V_{D_1} + 4R r_{C_2} V_{D_2} - 2R r_{C_2} V_i$
m_{1_5}	$R^2 V_i - R^2 V_{D_2} - R^2 V_{D_1} - R r_{C_2} V_{D_1} - R r_{C_2} V_{D_2} + R r_{C_2} V_i$
m_{1_6}	$R^2 V_i$
m_{1_7}	$R r_{C_2} V_i - 4R^2 V_i + R r_{D_1} V_i - R r_{D_2} V_i + R r_{S_2} V_i + r_{C_2} r_{D_1} V_i - r_{C_2} r_{D_2} V_i + r_{C_2} r_{S_2} V_i$
m_{1_8}	$6R^2 V_i - R r_{C_1} V_i + 3R r_{D_2} V_i + R r_{L_1} V_i + R r_{L_2} V_i - 2R r_{S_2} V_i - r_{C_1} r_{C_2} V_i + 3 r_{C_2} r_{D_2} V_i + r_{C_2} r_{L_1} V_i + r_{C_2} r_{L_2} V_i - 2 r_{C_2} r_{S_2} V_i$
m_{1_9}	$R r_{C_1} V_i - 4R^2 V_i - 2R r_{C_2} V_i - 2R r_{D_1} V_i - 3R r_{D_2} V_i - 2R r_{L_2} V_i + R r_{S_1} V_i + R r_{S_2} V_i + r_{C_1} r_{C_2} V_i - 2 r_{C_2} r_{D_1} V_i - 3 r_{C_2} r_{D_2} V_i - 2 r_{C_2} r_{L_2} V_i + r_{C_2} r_{S_1} V_i + r_{C_2} r_{S_2} V_i$
$m_{1_{10}}$	$R^2 V_i + R r_{C_2} V_i + R r_{D_1} V_i + R r_{D_2} V_i + R r_{L_2} V_i + r_{C_2} r_{D_1} V_i + r_{C_2} r_{D_2} V_i + r_{C_2} r_{L_2} V_i$

TABLE 3. Coefficients of (5).

m_{2_1}	$-R^2 V_{D_1} - R^2 V_{D_2} - R r_{C_2} V_{D_1} - R r_{C_2} V_{D_2}$
m_{2_2}	$2R^2 V_{D_1} + 2R^2 V_{D_2} - 2R^2 V_i + 2R r_{C_2} V_{D_1} + 2R r_{C_2} V_{D_2} - 2R r_{C_2} V_i$
m_{2_3}	$2R^2 V_i - R^2 V_{D_2} - R^2 V_{D_1} - R r_{C_2} V_{D_1} - R r_{C_2} V_{D_2} + 2R r_{C_2} V_i$
m_{2_4}	$R^2 V_i$
m_{2_5}	$R r_{S_2} V_i - 2R r_{C_1} V_i - R r_{C_2} V_i - R r_{D_1} V_i - R r_{D_2} V_i - 2R r_{S_1} V_i - 2R^2 V_i - 2 r_{C_1} r_{C_2} V_i - r_{C_2} r_{D_1} V_i - r_{C_2} r_{D_2} V_i - 2 r_{C_2} r_{S_1} V_i + r_{C_2} r_{S_2} V_i$
m_{2_6}	$R^2 V_i + 2R r_{C_1} V_i + R r_{C_2} V_i + R r_{D_1} V_i + R r_{D_2} V_i + R r_{L_1} V_i + R r_{L_2} V_i + 3R r_{S_1} V_i + 2 r_{C_1} r_{C_2} V_i + r_{C_2} r_{D_1} V_i + r_{C_2} r_{D_2} V_i + r_{C_2} r_{L_1} V_i + r_{C_2} r_{L_2} V_i + 3 r_{C_2} r_{S_1} V_i$

2) IDEAL GAIN

The ideal voltage gain is given by

$$M_2 = \frac{2}{(1-K)},$$

i.e. the cIBVM converter has double voltage gain as the classical IBVM converter.

C. MODE 3

In this case, from Section II, we have

$$\begin{aligned}\bar{\boldsymbol{A}}_3 &= \boldsymbol{A_2}K + \boldsymbol{A_3}(1-K),\\ \bar{\boldsymbol{B}}_3 &= \boldsymbol{B_2}K + \boldsymbol{B_3}(1-K) \text{ and}\\ \bar{\boldsymbol{E}}_3 &= \boldsymbol{E_2}K + \boldsymbol{E_3}(1-K).\end{aligned}$$

1) NON-IDEAL GAIN

The ideal static voltage gain is

$$M_3 = \frac{m_{3_1}K^4 + m_{3_2}K^3 + m_{3_3}K^2 + m_{3_4}K}{m_{3_5}K^4 + m_{3_6}K^3 + m_{3_7}K^2 + m_{3_8}K + m_{3_9}} \tag{6}$$

and its coefficients are in Table 4.

TABLE 4. Coefficients of (6).

m_{3_1}	$-R^2 V_{D_1} - R^2 V_{D_2} - R r_{C_2} V_{D_1} - R r_{C_2} V_{D_2}$
m_{3_2}	$2R^2 V_{D_1} + 2R^2 V_{D_2} + 2R r_{C_2} V_{D_1} + 2R r_{C_2} V_{D_2}$
m_{3_3}	$-R^2 V_{D_1} - R^2 V_{D_2} - R^2 V_i - R r_{C_2} V_{D_1} - R r_{C_2} V_{D_2} - R r_{C_2} V_i$
m_{3_4}	$V_i R^2 + r_{C_2} V_i R$
m_{3_5}	$R^2 V_i$
m_{3_6}	$R r_{D_2} V_i - R r_{C_2} V_i - R r_{D_1} V_i - 2R^2 V_i - R r_{S_2} V_i - r_{C_2} r_{D_1} V_i + r_{C_2} r_{D_2} V_i - r_{C_2} r_{S_2} V_i$
m_{3_7}	$R^2 V_i - R r_{C_1} V_i + R r_{C_2} V_i + R r_{D_1} V_i - 2R r_{D_2} V_i + R r_{L_1} V_i + R r_{L_2} V_i + 3R r_{S_2} V_i - r_{C_1} r_{C_2} V_i + r_{C_2} r_{D_1} V_i - 2 r_{C_2} r_{D_2} V_i + r_{C_2} r_{L_1} V_i + r_{C_2} r_{L_2} V_i + 3 r_{C_2} r_{S_2} V_i$
m_{3_8}	$R r_{C_1} V_i + R r_{D_2} V_i - 2R r_{L_2} V_i + R r_{S_1} V_i - 3R r_{S_2} V_i + r_{C_1} r_{C_2} V_i + r_{C_2} r_{D_2} V_i - 2 r_{C_2} r_{L_2} V_i + r_{C_2} r_{S_1} V_i - 3 r_{C_2} r_{S_2} V_i$
m_{3_9}	$R r_{L_2} V_i + R r_{S_2} V_i + r_{C_2} r_{L_2} V_i + r_{C_2} r_{S_2} V_i$

2) IDEAL GAIN

The ideal voltage gain is given by

$$M_3 = \frac{1}{K(1-K)}.$$

In this operation mode, it is easy to observe that the converter has a symmetric voltage gain, i.e. high gain at low and high values of duty-cycle.

V. EFFICIENCY ESTIMATION

Unlike was done to obtain an explicit analytical solution for the average voltage gain, the explicit analytical solution for efficiency is not suitable to be displayed, since it results in a rational function with extensive coefficients. Nevertheless, the efficiency can be defined and then evaluated numerically as in [19], [21].

In this section, the efficiency efficiency of the converter is defined considering conduction, switching and inductor

core losses, i.e. the efficiency in any operation mode is rated as a function of power input, power output and the power losses.

A. INPUT POWER

Let i_i be the input current. Then, i_i is given by

$$i_i = i_{L_1} + i_{L_2}. \tag{7}$$

Assuming $v_i = V_i$ as constant, the input power in steady-state is written as

$$P_i = \lim_{t\to\infty} \frac{1}{T_s} \int_t^{t+T_s} V_i i_i \mathrm{d}t = V_i I_i \tag{8}$$

where I_i the average current of the input voltage source. Then, let $\boldsymbol{J} =: \begin{bmatrix}1 & 1 & 0 & 0\end{bmatrix}$, for any operation mode, I_i can be expressed as

$$I_i = \boldsymbol{JX}, \tag{9}$$

which leads to

$$I_i = I_{L_1} + I_{L_2}, \tag{10}$$

where I_{L_1} and I_{L_2} are the average currents flowing through inductors L_1 and L_2, respectively. Therefore,

$$P_i = V_i \boldsymbol{JX}. \tag{11}$$

B. LOAD POWER

For a constant load R, the instantaneous load power (p_R) is given by

$$p_R = \frac{v_o^2}{R} \tag{12}$$

then, the load power consumption in steady-state is given by

$$P_R = \lim_{t\to\infty} \frac{1}{RT_s} \int_t^{t+T_s} v_o^2 \mathrm{d}t$$

yielding to

$$P_R = \frac{V_{o_{rms}}^2}{R} \tag{13}$$

where

$$V_{o_{rms}} = \lim_{t\to\infty} \sqrt{\frac{1}{T_s} \int_t^{t+T_s} v_o^2 \mathrm{d}t}.$$

Moreover, assuming the C_2 large enough, $V_{o_{rms}} \to V_o$ and

$$P_R = \frac{V_o^2}{R}, \tag{14}$$

which simplifies the efficiency estimation.

C. POWER LOSSES

The most relevant power losses can be separated as conduction and dynamic losses, where the last is essentially composed by switching and inductor core losses.

The conduction power loss is obtained by the power dissipated through the conduction parasitic resistances of the devices as well as the diodes forward voltage drops. The dynamic power loss depends on the switching frequency and is equal to the sum of power losses by virtue of switching transition and inductor core. The switching power losses occur during semiconductors transitions and is present in active switches and diodes [25].

Note that the load power already computes the device's conduction power losses which include the power dissipated as a result of the direct voltage drops of the diodes and the resistances of the switches and storage devices. However, it must be said that the dynamic power losse is relevant for efficiency analyses and therefore must be considered [19], [21], [26], [27]. Next we breakdown the power losses derivation.

1) CONDUCTION POWER LOSS

The conduction power loss (P_τ) portion for any operation mode is straightforward to be obtained in our modeling and it is given by

$$P_\tau \triangleq P_i - P_R.$$

Next we estimate the switching power losses.

2) SWITCHING POWER LOSSES

The estimation of the switching losses on the active semiconductors and diodes can be performed as shown in [25], [28]. In this case, we consider the turn-off loss on the diodes, the rise/fall time, and the output capacitance on active switches.

Let t_{r_1} and t_{r_2} be the rise time, t_{f_1} and t_{f_2} be the fall time of the semiconductors S_1 and S_2, and Q_{r_1} and Q_{r_2} represent the reverse recovery charge of the diodes D_1 and D_2, respectively.

Additionally, V_{C_1} is the average voltage on C_1, while $P_{sw_{D_1}}, P_{sw_{D_2}}, P_{sw_{S_1}}$ and $P_{sw_{S_2}}$ are the switching losses through D_1, D_2, S_1 and S_2, respectively.

The switching power losses are estimated by

$$\begin{aligned}
P_{sw_{D_1}} &= |\Phi_1| Q_{r_1} f_s, \\
P_{sw_{D_2}} &= |\Phi_2| Q_{r_2} f_s, \\
P_{sw_{S_1}} &= \frac{1}{2}(t_{r_1} + t_{f_1})|\Phi_3| f_s, \\
P_{sw_{S_2}} &= \frac{1}{2}(t_{r_2} + t_{f_2})|\Phi_4| f_s
\end{aligned}$$

where Φ_1, Φ_2, Φ_3, Φ_4, Φ_5 and Φ_6 are given in Table 5 for each operation mode.

Remark 1: Let C_{oss_1} and C_{oss_2} be the output capacitance of switches S_1 and S_2. Accordingly with [29], the power loss due

TABLE 5. Coefficients Φ_1, Φ_2, Φ_3 and Φ_4 for switching power loss estimation of each operation mode.

	Mode1	Mode 2	Mode 3
Φ_1	$V_o + V_{C_1}$	$V_o + V_{C_1}$	$V_o + V_{C_1}$
Φ_2	V_o	$V_o + V_{C_1}$	V_o
Φ_3	$(V_o + V_{C_1})(I_{L_1} + I_{L_2})$	$V_{C_1}(I_{L_1} + I_{L_2})$	$(V_o + V_{C_1})(I_{L_1} + I_{L_2})$
Φ_4	$V_o I_{L_2}$	$(V_o + V_{C_1})I_{L_2}$	$V_{C_1} I_{L_2}$

C_{oss_1} and C_{oss_2} is already computed in the parameters $P_{sw_{S_1}}$ and $P_{sw_{S_2}}$.

Let P_{ISS_1} and P_{ISS_2} be the power losses in the switch gate, Q_{g_1} and Q_{g_2} be the total gate charge and $V_{C_{G_1}}$ and $V_{C_{G_2}}$ represent the supply voltage of gate control circuit of S_1 and S_2, respectively, then

$$P_{ISS_1} = Q_{g_1} V_{C_{G_1}} f_s,$$
$$P_{ISS_2} = Q_{g_2} V_{C_{G_2}} f_s.$$

3) CORE INDUCTOR POWER LOSS

The major contribution of the inductor core losses are by virtue of hysteresis and eddy current. Let $P_{sw_{L_1}}$ and $P_{sw_{L_2}}$ be the inductor core loss through L_1 and L_2, respectively, then accordingly with [25], the inductor core power loss may be estimated by the Steinmetz's equation

$$P_{sw_{L_1}} = \lambda_1 f_s^{\alpha_1} \Delta B_1^{\beta_1} \hat{v_1},$$
$$P_{sw_{L_2}} = \lambda_2 f_s^{\alpha_2} \Delta B_2^{\beta_2} \hat{v_2},$$

where $\hat{v_1}, \hat{v_2}$ are the volume of the inductor core, $\lambda_1, \lambda_2, \alpha_1, \alpha_2, \beta_1$ and β_2 are constant depending on the core material which can be found in technical specifications of core manufacturers, and ΔB_1, ΔB_2 are the maximum induction on core given by

$$\Delta B_1 == \frac{\Delta i_{L_1} L_1}{2\hat{S_1} N_1}, \quad \Delta B_2 = \frac{\Delta i_{L_2} L_2}{2\hat{S_2} N_2}$$

where Δi_{L_1} and Δi_{L_2} are the change in inductor current, $\hat{S_1}$ and $\hat{S_2}$ are the cross-section area, and N_1 and N_2 are the number of turns in L_1 and L_2, respectively [25].

4) DYNAMIC POWER LOSS

The total dynamic power loss (P_v) is calculated as the sum of the switching power losses and is obtained by doing

$$P_v \triangleq P_{sw_{D_1}} + P_{sw_{D_2}} + P_{sw_{S_1}} + P_{sw_{S_2}} + P_{sw_{L_1}} + P_{sw_{L_2}} + P_{ISS_1} + P_{ISS_2} \quad (15)$$

D. OUTPUT POWER

The output power (P_o) is thus given by

$$P_o = P_i - P_\tau - P_v$$

and the efficiency is estimated by

$$\eta = \frac{P_o}{P_i}. \quad (16)$$

Note that as the output power depends on the power losses, which are different for each operation mode, then the efficiency depends on the operation mode. In the next section we perform a simulation to validate the modeling approach.

VI. SWITCHED MODEL VALIDATION

To validate the cIBVM models, a set of time-domain simulations are performed in which the switched model responses are compared to those of the switched circuit assembled in the Matlab/Simulink environment. In the analysis, we evaluated the interleaved and the complementary operation modes by observing states i_{L_1} and i_{L_2}, the cIBVM terminal voltage v_o, and the duty-cycles k_1 and k_2, respectively.

In this context, four different scenarios are considered in order to evaluate the cIBVM converter performance when it is processing approximately 100 W. In Table 8, the scenarios are given in terms of the corresponding operation mode, duty-cycle at steady-state regime, and 100 W resistance load value. The considered nominal parameters of the converter are rated in Table 6. As for the dynamic power loss estimation, the parameters that were used are given in Table 7.

TABLE 6. Nominal parameters.

Parameter	Value	Parameter	Value
r_{L_1}	98 mΩ	L_1	1.3 mH
r_{L_2}	98 mΩ	L_2	1.3 mH
r_{C_1}	25 mΩ	C_1	100 μF
r_{C_2}	30 mΩ	C_2	470 μF
r_{S_1}	8 mΩ	f_s	10 kHz
r_{S_2}	8 mΩ	v_i	30 V
r_{D_1}	7.1 mΩ	V_{D_1}	1.01 V
r_{D_2}	7.1 mΩ	V_{D_2}	1.01 V

The steady-state condition of the scenarios in Table 8 are shown in Figs. 11, 12, 13 and 14, respectively. As can be seen, the results show that the analytical models derived in this paper match precisely with the switched circuit.

In Table 9, the average currents (I_{L_1} and I_{L_2}) and voltages (V_o and V_i) are evaluated, while in Table 10 the analyzes are performed in terms of the input and output

TABLE 7. Parameters for dynamic power losses estimation.

Parameter	Value	Parameter	Value
Q_{r_1},Q_{r_2}	0.9 μC	t_{r_1},t_{r_2}	105 ns
t_{f_1},t_{f_2}	74 ns	λ_1,λ_2	17.26
N_1,N_2	150	$\hat{S}_1$,$\hat{S}_2$	6 cm^2
α_1,α_2	1.31	β_1,β_1	2.9
$\hat{v_1}$,$\hat{v_2}$	151cm^3	Q_{g_1},Q_{g_2}	161 nC
$V_{C_{G_1}}$,$V_{C_{G_2}}$	15 V	–	–

TABLE 8. Test scenarios.

Scenario	Mode	K	R (Ω)
1	1	0.3604	50
2	2	0.6080	225
3	3	0.2670	225
4	3	0.7331	225

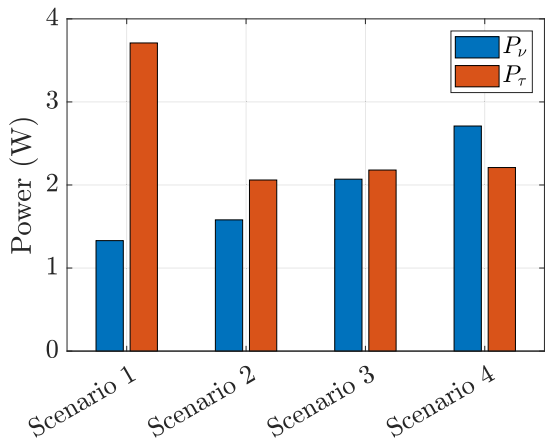

FIGURE 10. Power losses breakdown of simulated scenarios. The blue bar is the dynamic power loss and the red bar the conduction power loss.

TABLE 9. Average values of the state currents, input and output voltages - simulated scenarios.

Scenario	I_{L_1} (A)	I_{L_2} (A)	V_o	V_i
1	1.24	2.21	70.7	30.00
2	1.70	1.70	149.9	30.00
3	0.91	2.49	149.9	30.00
4	2.49	0.91	149.9	30.00

powers (P_i and P_o), the voltage gain and the converter efficiency. In addition, the power losses breakdown is shown in Fig. 10.

From Fig. 10, it is possible to conclude that the conduction power loss (P_τ) is dominant in scenarios 1 and 2, equivalent to dynamic power loss (P_ν) in scenario 3 and lightly inferior in scenario 4, respectively.

TABLE 10. Voltage gain and efficiency-simulated scenarios.

Scenario	P_i (W)	P_o (W)	Voltage Gain	η (%)
1	103.71	98.27	2.35	94.75
2	102.06	98.42	5.00	96.43
3	102.17	97.92	5.00	95.83
4	102.22	97.28	5.00	95.17

VII. RESISTIVE LOSSES EFFECT ON THE VOLTAGE GAIN

A set of waveforms were computed for each operation mode to evaluate the effects of the duty-cycle at steady-state regime (K), the parasitic resistances and load demanded on the voltage gain. To perform the tests, we considered $R = 225\ \Omega$ and the values presented in Table 6.

From Fig. 15, it is possible to see that in mode 3 a high voltage gain is achieved at both low and high K values, that is, the converter operates with a symmetric voltage gain relation. For modes 1 and 2, on the other hand, a discontinuity is observed when $K = 0.5$ which is where the converter moves from a quadratic to a double voltage gain relation.

A. INTERLEAVED MODE

To evaluate the voltage gain, we perform a sweep of the parasitic resistances in the interval [0 0.6] Ω, the duty-cycle at steady-state regime (K) in the range [0 1], and the load connected to the converter terminals in the interval [112.5 500] Ω. According to the results, we observed two different group of effects on the voltage gain in Fig. 16.

The first group, it can be seen that the highest voltage gain is achieved when the losses r_{L_1}, r_{L_2}, r_{S_1} and r_{S_2} are negligible, the load demand ($1/R$) is low and K is around of 90%, however increasing the losses, moving K far from 90% or reducing the load demand the voltage gain is reduced. Otherwise, on second group, the voltage gain is not much affected when the losses r_{C_1}, r_{C_2}, r_{D_1} and r_{D_2} are in the aforementioned range. In other words, for this case, the duty-cycle K impacts much more the voltage gain than the losses on the capacitors and diodes (r_{C_1}, r_{C_2} r_{D_1} and r_{D_2}).

B. COMPLEMENTARY OPERATION MODE

To evaluate the voltage gain for the complementary mode, we followed the same procedure described in the previous section for the interleaved mode. However, the load sweep is now performed according to the interval [112.5 500] Ω.

The results obtained for the complementary mode are presented in Fig. 17, and now three different group of effects were observed.

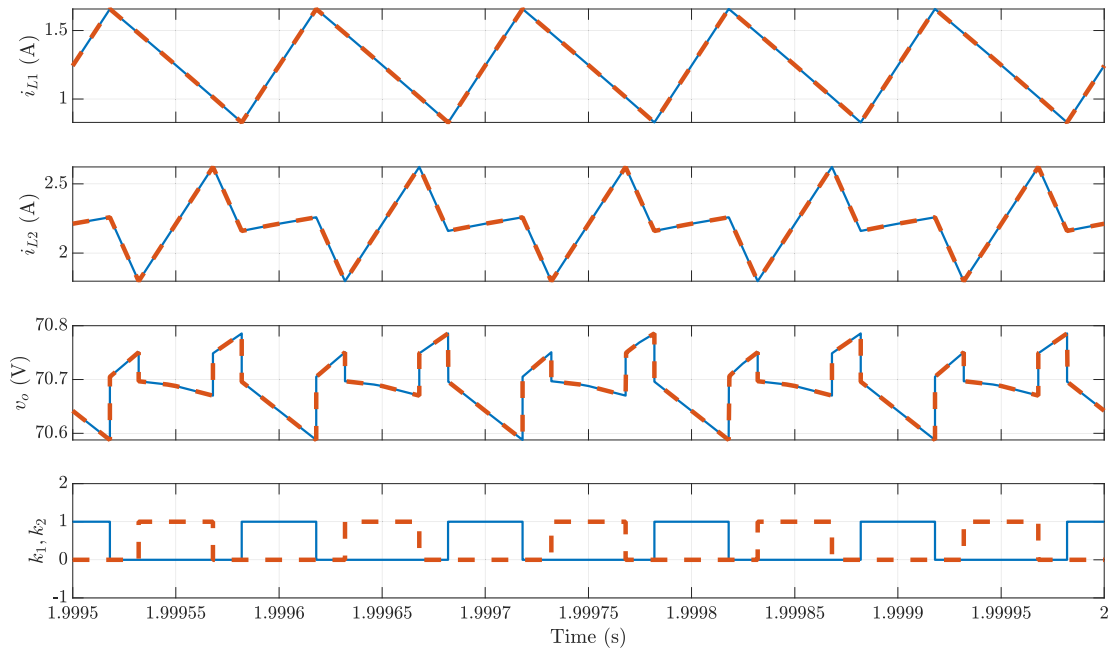

FIGURE 11. Scenario 1-The inductors current i_{L_1}, i_{L_2} and voltage output v_o under steady-state condition. The solid blue line is the model response, while the red dashed line is the switched simulation. The solid blue and red dashed lines are the driving signals k_1 and k_2, respectively.

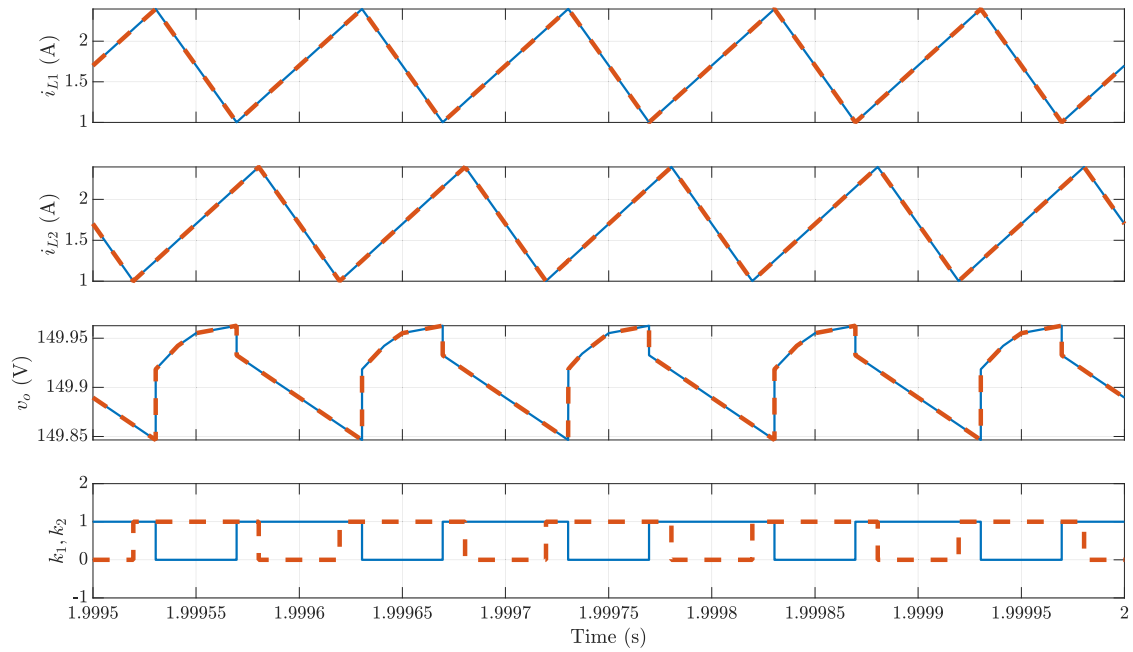

FIGURE 12. Scenario 2-The inductors current i_{L_1}, i_{L_2} and voltage output v_o under steady-state condition. The solid blue line is the model response, while the red dashed line is the switched simulation. The solid blue and red dashed lines are the driving signals k_1 and k_2, respectively.

In the first group, a high voltage gain is achieved by either reducing r_{L_1} and r_{S_1} or moving the duty-cycle K to approximately 5% or 95%, however the highest voltage gain is obtained when K is close to 95%. In the second group, the effect is similar. The highest voltage gain is obtained by either reducing r_{L_2} and r_{S_2} or moving the duty-cycle K to approximately 5% or 95%, however now the maximum gain is achieved when K is close to 5%. On the other hand, a third

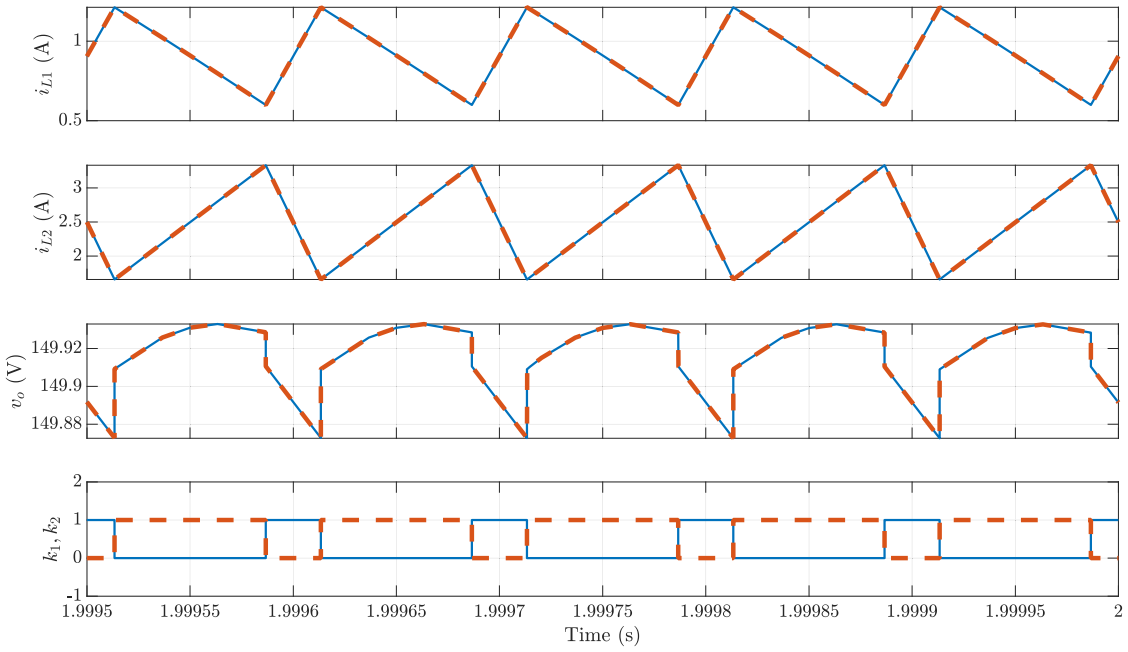

FIGURE 13. Scenario 3-The inductors current i_{L_1}, i_{L_2} and voltage output v_o under steady-state condition. The solid blue line is the model response, while the red dashed line is the switched simulation. The solid blue and red dashed lines are the driving signals k_1 and k_2, respectively.

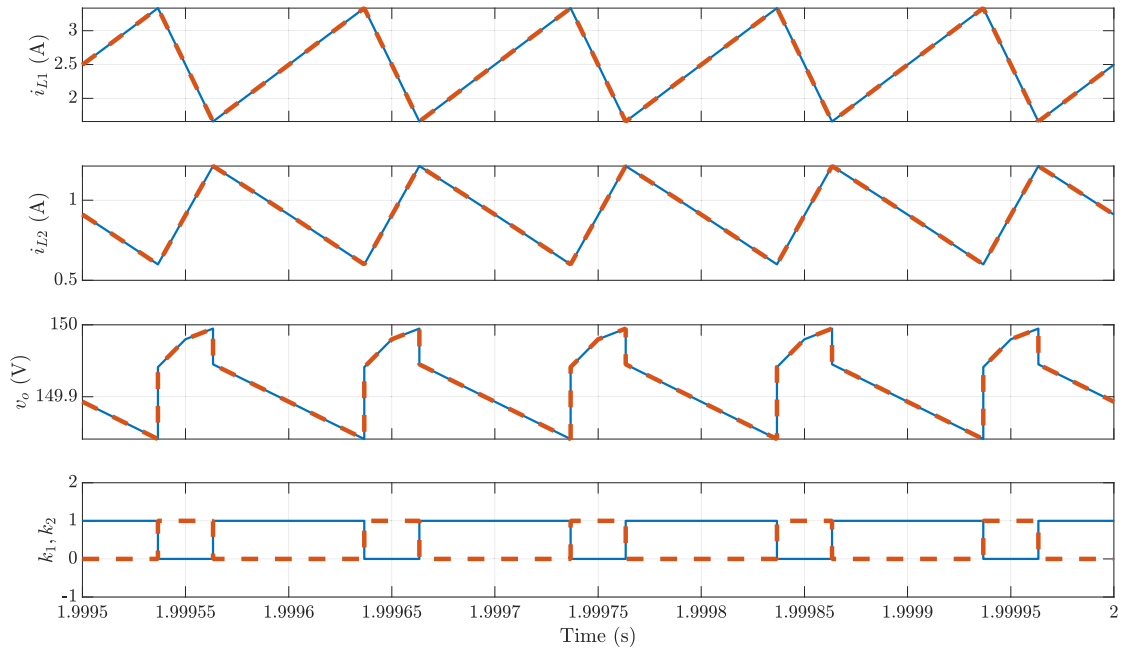

FIGURE 14. Scenario 4-The inductors current i_{L_1}, i_{L_2} and voltage output v_o under steady-state condition. The solid blue line is the model response, while the red dashed line is the switched simulation. The solid blue and red dashed lines are the driving signals k_1 and k_2, respectively.

group is observed, in which the maximum gain is achieved by reducing either r_{C_1}, r_{C_2}, r_{D_1} or r_{D_2}, or even by choosing K as either 5% or 95%. In this type of procedure, the highest voltage gain is quite similar in both operating points (5% and 95%).

In the latest group of effects, it can be seen that a high load demand $(1/R)$ reduces the voltage gain, while changing K leads to two equivalent maximum points at 5% and 95%, respectively.

VIII. EXPERIMENTAL RESULTS

A prototype converter from Fig. 1 was built with the devices shown in Table 11 and parameters shown

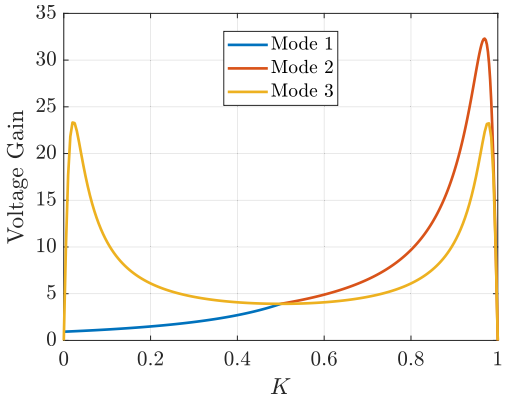

FIGURE 15. Behavior of the voltage gain.

in Table 12. The switching frequency was set to 10 kHz and the voltage input to 30 V. A picture of the experimental setup used to verify the effectiveness of the obtained non-ideal voltage gain and efficiency is presented in Fig. 18.

A series of experimental tests were performed to verify the effectiveness of the analytical models presented previously. The results are given in Figs. 19, 20, 21 and 22 for the same scenarios that were simulated in the Matlab/Simulink environment. It is easy to see that the experimental results match precisely in terms of behavior (shaping, level, distortion, etc) with the simulation results in Figs. 11, 12, 13 and 14.

Additionally, Table 13 shows the average current (I_{L_1} and I_{L_2}) through the inductors L_1 and L_2, the input (V_i) and output (V_o) voltages in all scenarios, while Table 14 shows the input (P_i) and output (P_o) power, voltage gain and efficiency (η).

Other important result is achieved when Tables 9 and 10 are compared to Tables 13 and 14. Considering the output (V_o) average voltages, the maximum relative error between the experimental and simulation results is 1.16%. Furthermore, evaluating the efficiency and the voltage gain, the greatest relative error is 0.77%.

To obtain the experimental voltage gain, we performed a duty-cycle (K) sweep in all operation modes 1, 2 and 3. The results are shown in Figs. 23 and 24. As can be noted, the limit of operation occurs when the current reaches approximately 11 A, which is the current level that leads

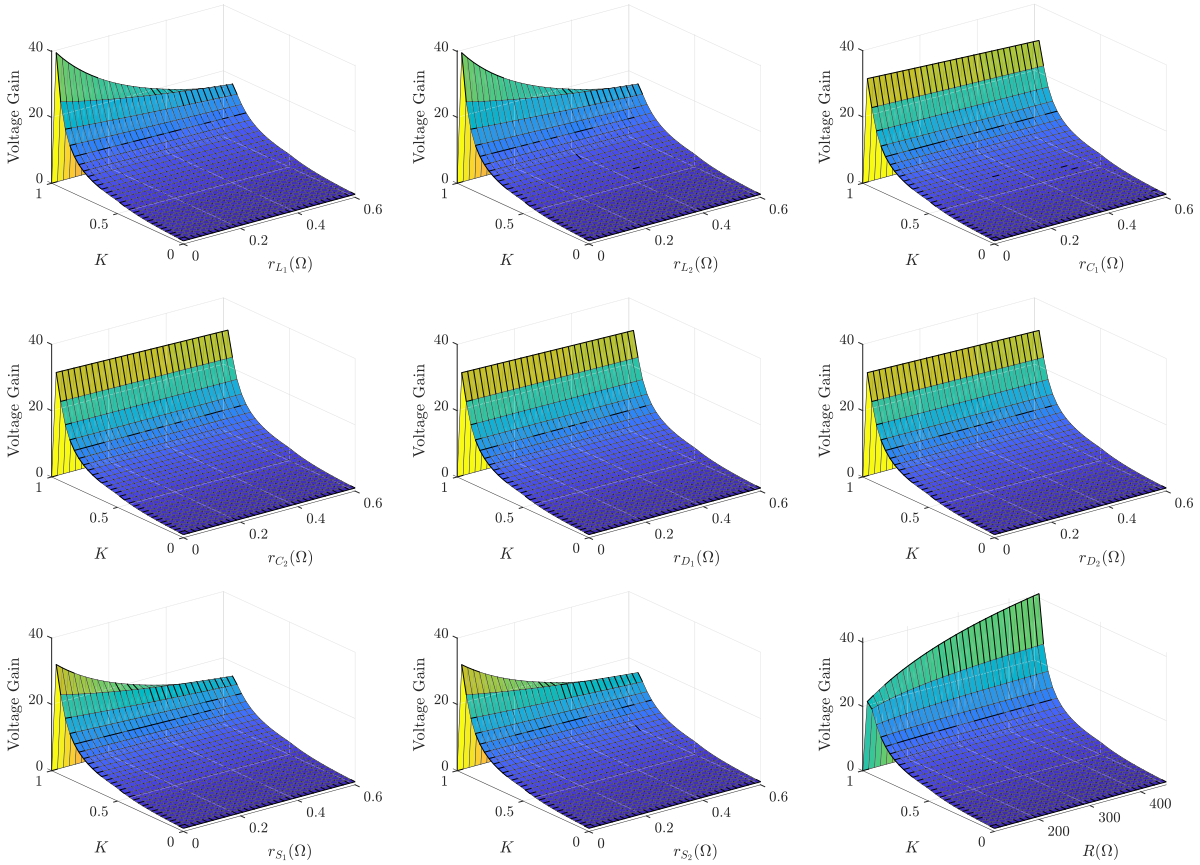

FIGURE 16. Evaluation of the voltage gain and efficiency in terms of parasitic resistances, load demand and duty-cycle for modes 1 and 2 (Interleaved mode).

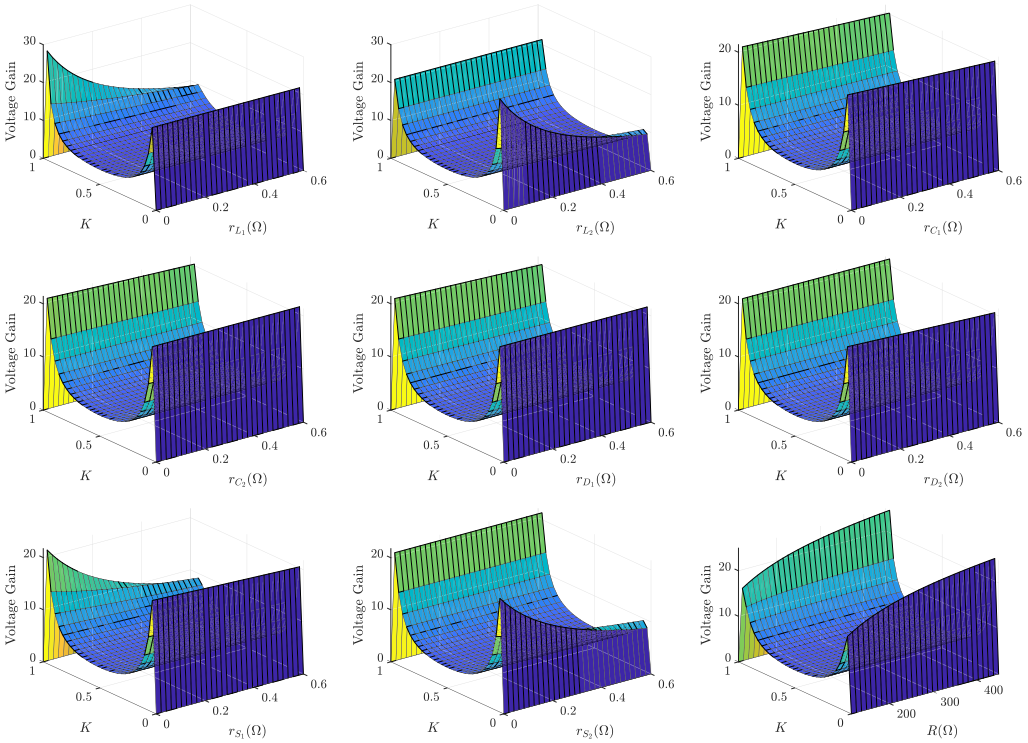

FIGURE 17. Evaluation of the voltage gain and efficiency in terms of parasitic resistances, load and duty-cycle for mode 3 (complementary switching mode).

TABLE 11. Description of the commercial devices used in the cIBVM converter prototype.

Device	Description
S_1,S_2	MOSFET IRF4668PbF
D_1,D_2	DSEI 2X31-06C
L_1,L_2	3F3 ferrite grade, 18 AWG
C_1,C_2	Electrolytic capacitors

TABLE 12. Parameters of the commercial devices used in the cIBVM converter prototype.

Parameter	Value	Parameter	Value
N_1,N_2	150	$\hat{S}_1$,$\hat{S}_2$	6 cm^2
α_1,α_2	1.31	β_1,β_1	2.9
$\hat{v_1}$,$\hat{v_2}$	151cm^3	λ_1,λ_2	17.26
r_{S_1},r_{S_2}	8 mΩ	Q_{g_1},Q_{g_2}	161 nC
t_{r_1},t_{r_2}	105 ns	t_{f_1},t_{f_2}	74 ns
r_{D_1},r_{D_2}	7.1 mΩ	V_{D_1}, V_{D_2}	1.01 V
Q_{r_1},Q_{r_2}	0.9 μC	V_{CG_1},V_{CG_2}	15 V
L_1,L_2	1.3 mH	r_{L_1},r_{L_2}	98 mΩ
C_1	100 μF	r_{C_1}	25 mΩ
C_2	470 μF	r_{C_2}	30 mΩ

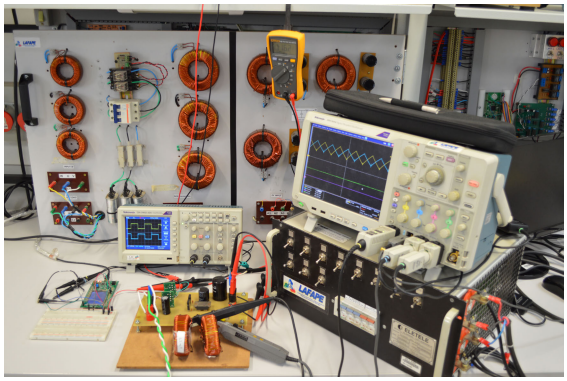

FIGURE 18. Experimental setup.

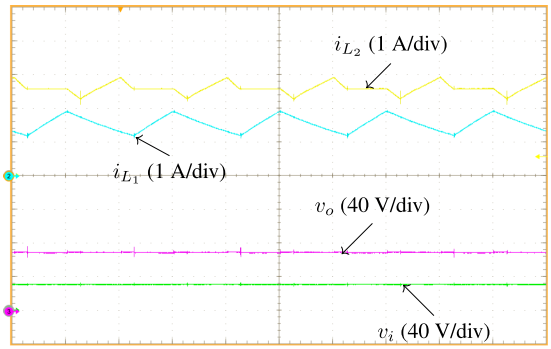

FIGURE 19. Scenario 1–Experimental analysis at steady-state regime considering i_{L_1}, i_{L_2}, v_i and v_o. Time-scale is 50 μs/div.

the DC voltage source to operate under its over current protection. In Fig. 23, it is possible to see the discontinuity between operation modes 1 and 2 when $K = 0.5$. In Fig. 24, the symmetric voltage gain relation of operation

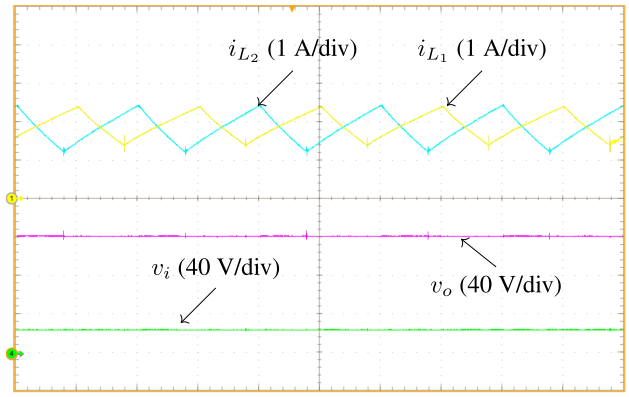

FIGURE 20. Scenario 2–Experimental analysis at steady-state regime considering i_{L_1}, i_{L_2}, v_i and v_o. Time-scale is 50 μs/div.

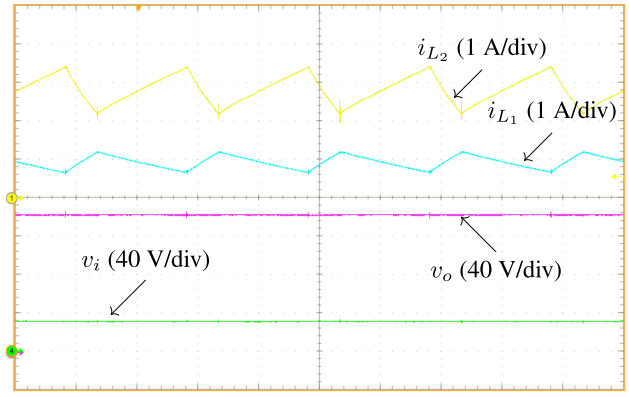

FIGURE 21. Scenario 3–Experimental analysis at steady-state regime considering i_{L_1}, i_{L_2}, v_i and v_o. Time-scale is 50 μs/div.

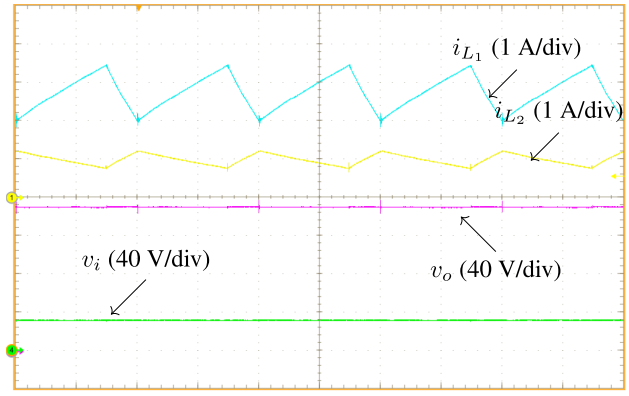

FIGURE 22. Scenario 4–Experimental analysis at steady-state regime considering i_{L_1}, i_{L_2}, v_i and v_o. Time-scale is 50 μs/div.

TABLE 13. Average values of the states currents, input and output voltages-experimental scenarios.

Scenario	I_{L_1} (A)	I_{L_2} (A)	V_o (V)	V_i (V)
1	1.34	2.48	71.44	28.41
2	1.72	1.78	151.48	29.99
3	0.92	2.72	151.66	29.53
4	2.68	0.91	151.32	29.69

mode 3 is confirmed when performing the duty-cycle (K) sweep.

TABLE 14. Voltage gain and efficiency-experimental scenarios.

Scenario	P_i (W)	P_o (W)	Voltage Gain	η (%)
1	108.53	102.07	2.51	94.05
2	104.97	101.98	5.05	97.16
3	107.49	102.23	5.13	95.10
4	106.59	101.77	5.09	95.48

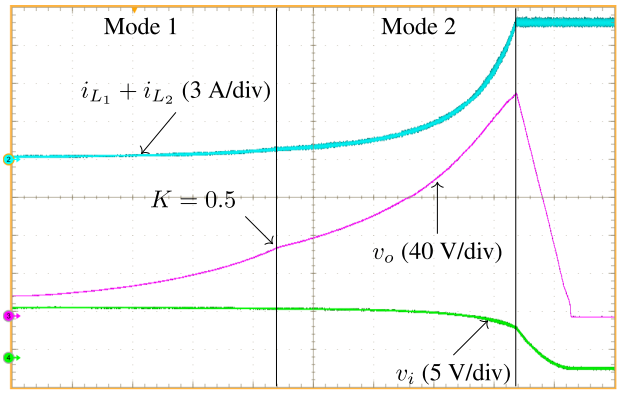

FIGURE 23. Interleaved technique–Effect of the duty-cycle sweeping on the terminal voltage (v_o) and input current ($i_i = i_{L_1} + i_{L_2}$) when the load demand is constant ($R = 225\ \Omega$). Time-scale is 20 s/div and the power supply had overcurrent protection.

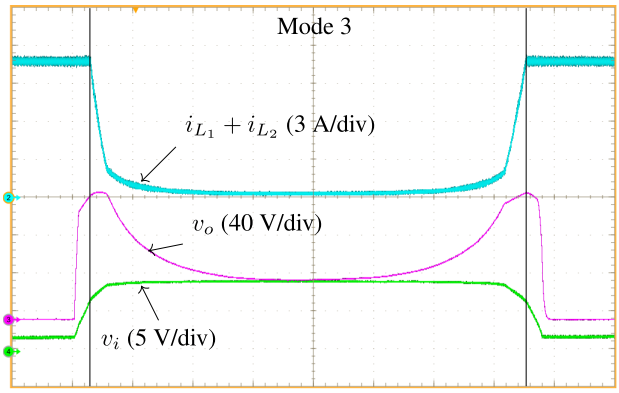

FIGURE 24. Complementary switching–Effect of the duty-cycle sweeping on the terminal voltage (v_o) and input current ($i_i = i_{L_1} + i_{L_2}$) when the load demand is constant ($R = 225\ \Omega$). Time-scale is 20 s/div and the power supply had overcurrent protection.

IX. CONCLUSION

In this paper, a complete non-ideal steady-state analysis of a threefold operation mode interleaved-based DC–DC converter was performed. Although the converter topology has been firstly proposed in [24], a complete description of the non-ideal performance was not deeply explored in the literature. As was previously discussed, it is possible to successfully implement three different operation modes depending solely on the switching strategy that is used. In this case, operation modes 1 and 2 are obtained when adopting the interleaved switching strategy across intervals $0 \leq K < 0.5$ and $0.5 \leq K \leq 1$, thus yielding a quadratic and a double static voltage gain relation, respectively. Operation mode 3, on the other hand, is obtained upon considering a complementary

switching strategy, which leads to a high symmetric static voltage gain relation on the converter terminals.

As an inherent drawback, it was shown that both the complementary mode and the interleaved mode with $K < 0.5$ the inductor currents are imbalanced. On the other hand, in such regions the converter exhibits unique characteristics as symmetric and quadratic voltage gain, which results in a trade-off to be faced and dealt with by designers.

The performed non-ideal analyzes were entirely based on the state-space models, with conduction and dynamic losses, which were calculated for each specific operation mode, besides presenting a complete evaluation of the static voltage gain and efficiency relations. It was also presented a detailed description of each resistive loss impact in terms of overall performance.

Finally, a Simulink-based cross validation and a sequence of experimental tests were carried out to validate the obtained models. The results showed that the calculated analytical models are effective, since it is possible to observe that the plotted and experimental waveforms match precisely in terms of shape, level and distortion. Nevertheless, it is important to state that when the experimental results are confronted against the simulation, a overall mean relative error of 1.78% is observed, which is a reasonable approximation.

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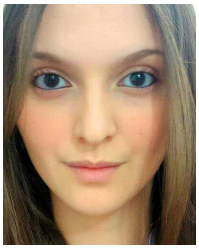

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