Boletim Técnico da Escola Politécnica da USP
Departamento de Engenharia de Sistemas Eletrônicos

ISSN 1517-3542

BT/PSI/0210

A New Technique to Extract the Oxide Charge Density at Front and Back Interfaces of SOI nMOSFETs Devices

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São Paulo – 2002

O presente trabalho é um resumo da tese de doutorado apresentada por Aparecido Sirley Nicolett, sob orientação do Prof. Dr. João Antonio Martino.: "Estudo do Comportamento da Resistência Série e Desenvolvimento de Novos Métodos de Caracterização Elétrica em Dispositivos SOI MOSFET", defendida em 27/04/01, na Escola Politécnica.

A íntegra da tese encontra-se à disposição com o autor e na Biblioteca de Engenharia de Eletricidade da Escola Politécnica/USP.

FICHA CATALOGRÁFICA

Nicolett, Aparecido Sirley
A new technique to extract the oxide charge density at front and back interfaces of SOI nMOSFETs devices / A.S. Nicolett, J.A. Martino. – São Paulo : EPUSP, 2002.
10 p. – (Boletim Técnico da Escola Politécnica da USP, Departamento de Engenharia de Sistemas Eletrônicos, BT/PSI/0210)

1. Transistores 2. Baixa temperatura [Efeitos] I. Martino, João Antonio II. Universidade de São Paulo. Escola Politécnica. Departamento de Engenharia de Sistemas Eletrônicos III. Título
IV. Série
ISSN 1517-3542 CDD 621.381528
620.11216

A New Technique to Extract the Oxide Charge Density at Front and Back Interfaces of SOI nMOSFETs Devices

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Abstract

This work presents a new method to extract the oxide charge densities at front (Q_{ox1}) and back (Q_{ox2}) interfaces of fully depleted SOI nMOSFETs. The proposed method exploits the influence of the front and back gate voltages on the back and front channel current regime respectively. To extract Q_{ox2}, the drain current curve is measured as a function of the back gate voltage V_{GB} with the front interface inverted. When the back interface condition changes due to the back gate voltage, kinks occur in the front drain current for specific V_{GB} biases and these are used by the method. Similarly, the back drain current as a function of the front gate voltage V_{GF} with the back interface inverted shows some kinks at specific V_{GF} which are used by the method to extract Q_{ox1}. MEDICI simulations were used to support the analysis and the method was applied experimentally.

1. Introduction

Silicon-On-Insulator (SOI) technology has grown rapidly during the past years, mainly because this technology has many advantages over bulk technology [1 - 6]. However, not all SOI MOSFETs have the same behavior because they are dependent on the silicon film thickness and the channel doping concentration. Three different types of devices exist: thick-film, medium thickness and thin-film devices. In a thin-film device, the silicon film (transistor channel) can be fully depleted and in this case there is an interaction between the front- and back-interface. Special interest has been paid to fully depleted SOI MOSFETs which have superior behavior compared to partially depleted ones, like for example a high transconductance and low electrical fields [7]. Figure 1 shows a cross section of an SOI nMOSFET illustrating some of the notations used.

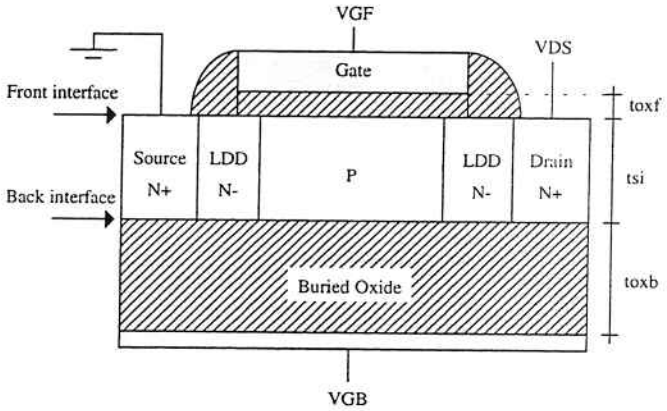


Figure 1: Cross-section of the LDD SOI nMOSFET illustrating some of the notations used.

In fully depleted SOI devices, the behavior of the front interface (between the gate oxide and the silicon film) is modified by the back interface condition (between the silicon film and the buried oxide) which can be inverted, depleted or accumulated. Similarly, the conditions of the front interface also modify the characteristics of the back interface [8]. Equations (1) and (2) are the relations that describe the charge coupling between the front and back gates in a fully depleted SOI MOSFET [8, 9].

$$V_{GF} = \phi_{MS1} - \frac{Q_{ox1}}{C_{oxf}} + \left(1 + \frac{C_{Si}}{C_{oxf}}\right)\phi_{SF} - \frac{C_{Si}}{C_{oxf}}\phi_{SB} + \frac{qN_{af}t_{Si}}{2C_{oxf}} - \frac{Q_{S1}}{C_{oxf}} \quad (1)$$

$$V_{GB} = \phi_{MS2} - \frac{Q_{ox2}}{C_{oxb}} + \left(1 + \frac{C_{Si}}{C_{oxb}}\right)\phi_{SB} - \frac{C_{Si}}{C_{oxb}}\phi_{SF} + \frac{qN_{af}t_{Si}}{2C_{oxb}} - \frac{Q_{S2}}{C_{oxb}} \quad (2)$$

2. Proposed Method

To determine the back oxide charge density Q_{ox2}, the I_{DS} vs. V_{GB} curve is obtained for a constant V_{GF} larger than Vth_{Facc2}. Figure 2 shows the I_{DS}, $\delta I_{DS}/\delta V_{GB}$ and $\delta^2 I_{DS}/\delta V_{GB}^2$ curves as a function of the V_{GB}.

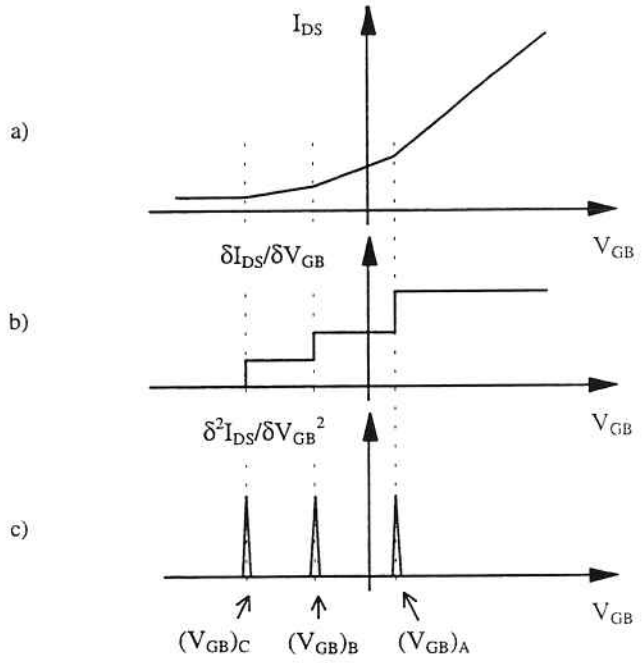


Figure 2: I_{DS}, $\delta I_{DS}/\delta V_{GB}$ and $\delta^2 I_{DS}/\delta V_{GB}^2$ curves as a function of the V_{GB}.

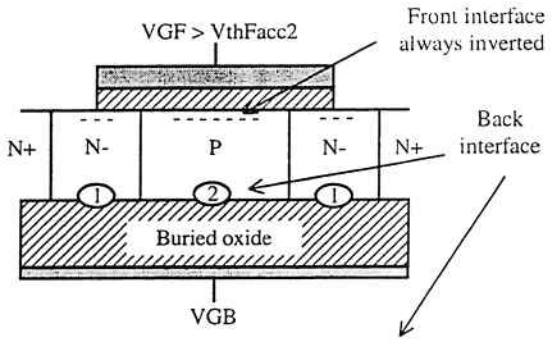
Figure 2a shows the I_{DS} behavior when the back gate voltage changes from positive to negative values. For high positive bias, the back interface below the channel is inverted. For this condition, the front threshold voltage $Vth_{F,inv2}$ is lowest, taking into account that the front threshold voltage in thin-film SOI devices depends on the back bias condition [3]. For high negative bias, the back

interface underneath the channel becomes accumulated. For this condition, the front threshold voltage $Vth_{F,acc2}$ is largest. The I_{DS} curve must be measured using a front voltage V_{GF} larger than $Vth_{F,acc2}$. This ensures that the front interface is always in inversion, enabling current flow from source to drain using different V_{GB}, for a positive V_{DS}.

Figures 2b and 2c show the first and second derivatives of the I_{DS} vs. V_{GB} curve, respectively. In figure 2c, three important points (maximum points) can be seen. For $V_{GB} > (V_{GB})_A$, the back interface is inverted under the channel and accumulated under the LDD regions. The point $(V_{GB})_A$ represents the voltage where the back interface under the channel becomes inverted.

For $(V_{GB})_B < V_{GB} < (V_{GB})_A$, the back interface under the channel is depleted, while the back interface for the LDD region remains accumulated. The point $(V_{GB})_B$ represents the condition where the back interface under the channel changes from depletion to accumulation, while the back interface for the LDD regions is changing from accumulation to depletion. In fact, the voltages corresponding to these two effects do not occur in the same point, but they are very close, due to the concentrations used for the channel and LDD regions. Therefore, one transition point is hidden by the other.

For $(V_{GB})_C < V_{GB} < (V_{GB})_B$, the back interface on the channel can be considered accumulated, while the LDD back interface can be considered depleted. The point $(V_{GB})_C$ represents the back voltage where the LDD regions become inverted at the back interface and it can be used to estimate the LDD doping concentration [10]. Figure 3 shows the back gate voltage influence on the back interface conditions.



V_{GB}	Regions	
	①	②
$V_{GB} > (V_{GB})_A$	Accumulated	Inverted
$(V_{GB})_B < V_{GB} < (V_{GB})_A$	Accumulated	Depleted
$(V_{GB})_C < V_{GB} < (V_{GB})_B$	Depleted	Accumulated
$V_{GB} < (V_{GB})_C$	Inverted	Accumulated

Figure 3: Back gate voltage influence on the back interface conditions of an LDD SOI nMOSFET.

Applying the conditions of the points $(V_{GB})_A$ and $(V_{GB})_B$ in the equation (2), where the front interface is always inverted ($\phi_{SF} = \phi_{SF,inv1}$, because $V_{GF} > Vth_{F,acc2}$) and the back interface is inverted ($\phi_{SB} = \phi_{SB,inv2}$, $Q_{S2} = 0$) or accumulated ($\phi_{SB} = 0$, $Q_{S2} = 0$), equations (3) e (4) are defined. Q_{ox2} can be obtained by the sum of (3) and (4).

$$(V_{GB})_A = \phi_{MS2} - \frac{Q_{ox2}}{C_{oxb}} + \left(1 + \frac{C_{Si}}{C_{oxb}}\right)\phi_{SB,inv2} - \frac{C_{Si}}{C_{oxb}}\phi_{SF,inv1} + \frac{qN_{af}t_{Si}}{2C_{oxb}} \quad (3)$$

$$(V_{GB})_B = \phi_{MS2} - \frac{Q_{ox2}}{C_{oxb}} - \frac{C_{Si}}{C_{oxb}}\phi_{SF,inv1} + \frac{qN_{af}t_{Si}}{2C_{oxb}} \quad (4)$$

$$Q_{ox2} = \frac{\varepsilon_{ox}}{t_{oxb}}\left(\phi_{MS2} + \frac{\phi_{SB,inv2}}{2} - \frac{(V_{GB})_A + (V_{GB})_B}{2}\right) + \frac{\varepsilon_{Si}}{t_{Si}}\left(\frac{\phi_{SB,inv2}}{2} - \phi_{SF,inv1}\right) + \frac{qN_{af}t_{Si}}{2} \quad (5)$$

Similarly, to determine the front oxide charge density Q_{ox1}, the I_{DS} versus V_{GF} curve is determined for a constant V_{GB} larger than $Vth_{B,acc1}$, where $Vth_{B,acc1}$ is the back threshold voltage with the front interface accumulated. For these conditions, two maximum points can be also observed in $\delta^2 I_{DS}/\delta V_{GF}^2$. Figure 4 shows the I_{DS} and $\delta^2 I_{DS}/\delta V_{GF}^2$ curves as a function of the V_{GF}.

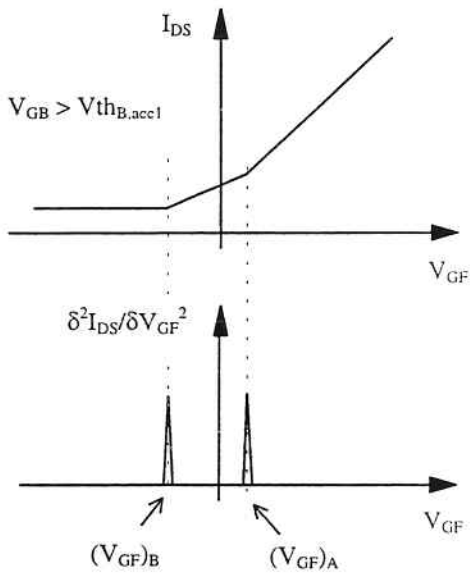


Figure 4: I_{DS} and $\delta^2 I_{DS}/\delta V_{GF}^2$ curves as a function of the V_{GF}.

The point $(V_{GF})_A$ represents the voltage where the front interface becomes inverted. The point $(V_{GF})_B$ represents the voltage where the front interface becomes accumulated. Applying the conditions of the points $(V_{GF})_A$ and $(V_{GF})_B$ in the equation (1), where the back interface is always inverted ($\phi_{SB} = \phi_{SB,inv2}$, because $V_{GB} > Vth_{B,acc1}$) and the front interface is inverted ($\phi_{SF} = \phi_{SF,inv1}$, $Q_{S1} = 0$) or accumulated ($\phi_{SF} = 0$, $Q_{S1} = 0$), Q_{ox1} can be obtained from equation (6).

$$Q_{ox1} = \frac{\varepsilon_{ox}}{t_{oxf}}\left(\phi_{MS1} + \frac{\phi_{SF,inv1}}{2} - \frac{(V_{GF})_A + (V_{GF})_B}{2}\right) + \frac{\varepsilon_{Si}}{t_{Si}}\left(\frac{\phi_{SF,inv1}}{2} - \phi_{SB,inv2}\right) + \frac{qN_{af}t_{Si}}{2} \quad (6)$$

In this proposed technique, the approximation used for the surface potential at the strong inversion ($\phi_{SF} = \phi_{SF,inv1}$ or $\phi_{SB} = \phi_{SB,inv2}$) is based on the model proposed by Lindner [11], equation (7), who suggested that the band bending is closer to the value at which minority carrier pin the surface band bending in inversion.

$$\phi_{SF,inv1} = \phi_{SB,inv2} = \frac{KT}{q}\left(2.1\ln\frac{N_{af}}{ni} + 2.08\right) \tag{7}$$

3. Simulation Details and Results

The SOI nMOSFETs studied have a drawn channel length L_m = 1.0 μm and channel doping concentration N_{af} = $1x10^{17}$ cm^{-3}. A gate oxide thickness t_{oxf} = 20 nm, buried oxide thickness t_{oxb} = 80 nm and a silicon film thickness t_{Si} = 80 nm were used as input parameter for the bidimensional numerical simulator MEDICI [12]. For the simulations, different front and back oxide charge densities, Q_{ox1} and Q_{ox2} respectively, were used and the interface trap densities were assumed negligible. Figure 5 shows the I_{DS} and $\delta^2 I_{DS}/\delta V_{GB}^2$ curves as a function of the V_{GB}.

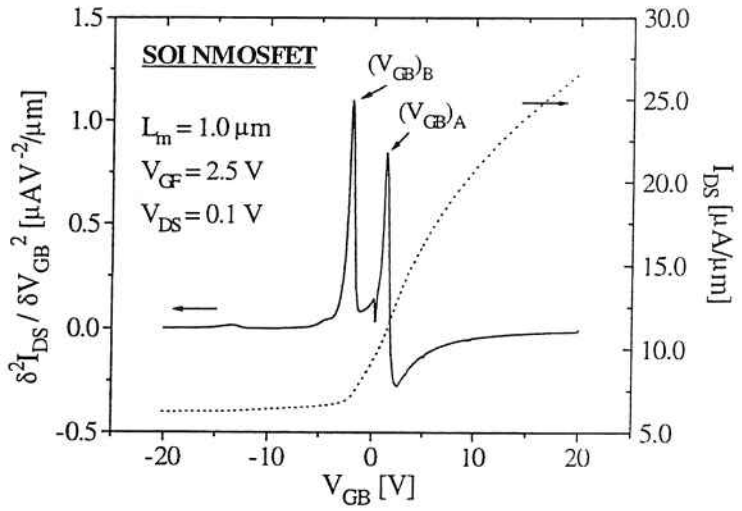


Figure 5: Simulated I_{DS} and $\delta^2 I_{DS}/\delta V_{GB}^2$ versus V_{GB} curves for a constant V_{GF} of an SOI nMOSFET, where $(V_{GB})_A$ = 1.35 V and $(V_{GB})_B$ = - 1.95 V.

Figure 6 shows the front surface potential variation as a function of depth in the film for the $(V_{GB})_A$ and $(V_{GB})_B$ voltages. Due to the charge coupling between the front and back interfaces on the fully depleted SOI device, it is not possible to derive ϕ_{SF}, because there is no neutral region between the interfaces as a reference.

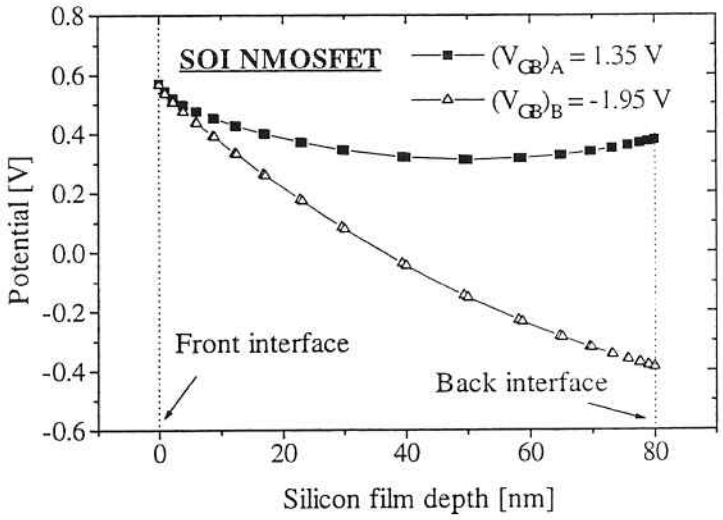


Figure 6: Front and back surfaces potential variation for a fully depleted SOI nMOSFET as a function of depth for the two different back gate voltages.

To determine ϕ_{SF}, a thick-film SOI nMOSFET was simulated by MEDICI using t_{Si} = 300 nm. Figure 7 shows the front surface potential variation with depth for the $(V_{GB})_A$ and $(V_{GB})_B$ voltages. Now there is not a coupling between the interfaces and it is possible to extract ϕ_{SF}.

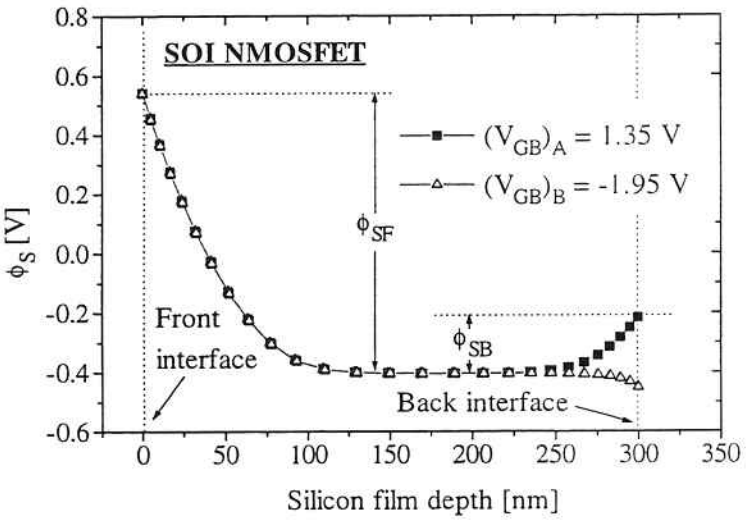


Figure 7: Front and back surface potential variation for a thick-film LDD SOI nMOSFET as a function of depth in the film for the two different back gate voltages.

Figure 8 shows the values of ϕ_{SF} and ϕ_{SF}/ϕ_{Ff} as a function of the overdrive voltage $(V_{GF} - Vth_F)$. One can see that for $(V_{GF} - Vth_F) > 1.0$ V, $\phi_{SF} \approx 0.94$ V and $\phi_{SF}/\phi_{Ff} \approx 2.3$. These results are very close to the results expected by the Lindner's model, when strong inversion is used.

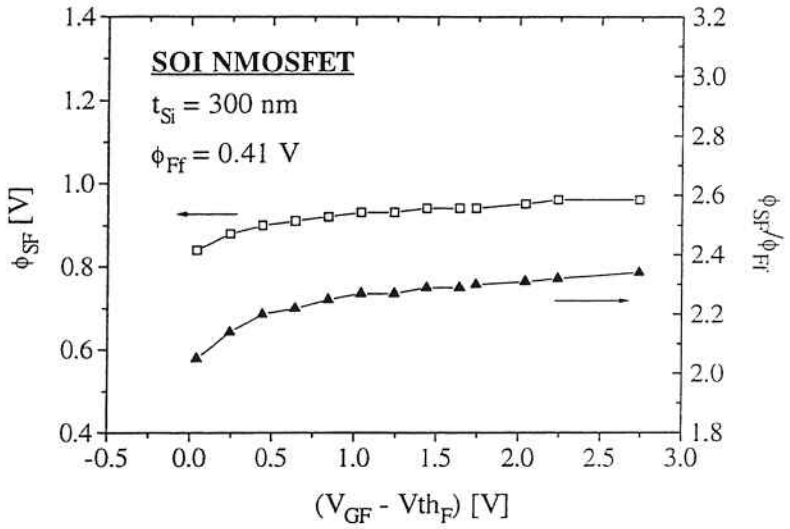


Figure 8: Front surface potential variation for a thick-film LDD SOI nMOSFET as a function of the overdrive voltage.

Figure 9 shows the I_{DS} and $\delta^2 I_{DS}/\delta V_{GF}^2$ curves as a function of the V_{GF}. Figure 10 shows the values of ϕ_{SB} and ϕ_{SB}/ϕ_{Ff} as a function of the overdrive voltage $(V_{GB} - Vth_B)$. One can see that for $(V_{GB} - Vth_B) > 1.0$ V, $\phi_{SB} \approx 0.94$ V and $\phi_{SB}/\phi_{Ff} \approx 2.3$. These results are very close to the results expected by the Lindner's model, when strong inversion is used.

In order to analyze the proposed technique, different SOI devices were simulated with channel doping concentration $N_{af} = 1x10^{17}$ cm^{-3}, source/drain doping concentration $N_{DS} = 1x10^{20}$ cm^{-3}, LDD doping concentration $N_{LDD} = 1x10^{18}$ cm^{-3} and different oxide charge densities. Table I shows the results of Q_{ox1} and Q_{ox2} obtained by the proposed method. The error obtained is lower than 15 %.

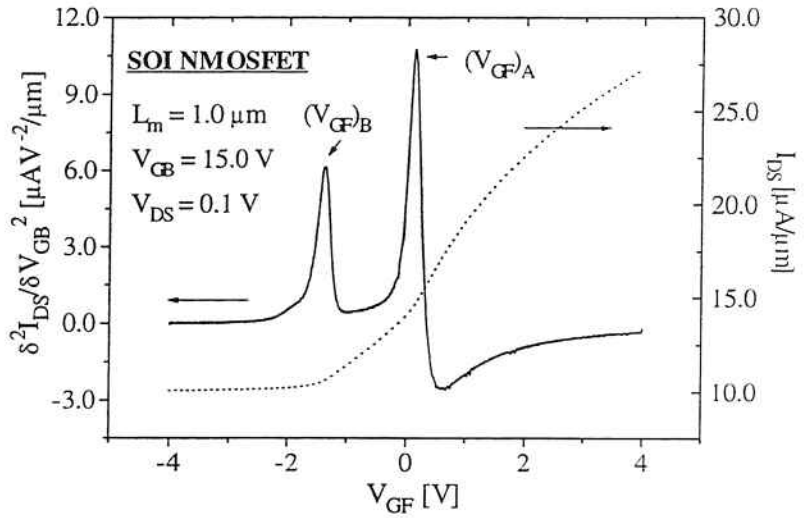


Figure 9: Simulated I_{DS} and $\delta^2 I_{DS}/\delta V_{GF}^2$ versus V_{GF} curves for a constant V_{GB} of an SOI nMOSFET, where $(V_{GF})_A = 0.12$ V and $(V_{GF})_B = -1.38$ V.

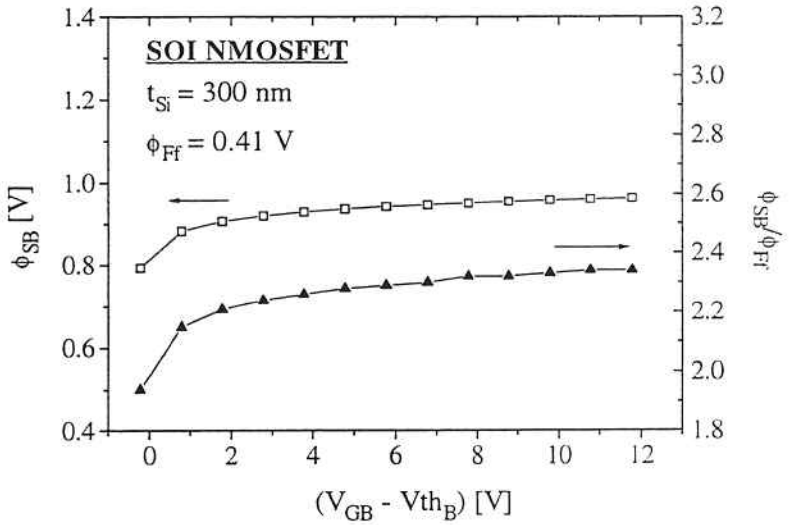


Figure 10: Back surface potential variation for a thick-film LDD SOI nMOSFET as a function of the overdrive voltage.

Table I: Results obtained by the proposed method using different devices simulated by MEDICI.

	Input Values [x 10^{11} cm^{-2}]		Method [x 10^{11} cm^{-2}]	
Dev.	Q_{ox1}/q	Q_{ox2}/q	Q_{ox1}/q	Q_{ox2}/q
S1	1.00	1.00	1.09	1.14
S2	1.00	2.00	1.09	2.07
S3	2.00	3.00	2.17	3.12
S4	2.00	4.00	2.17	4.09

4. Experimental Details and Results

The LDD SOI nMOSFETs used in this study had a drawn channel width W_m of 36 μm and different drawn channel lengths L_m of 1.5 (E1), 1.0 (E2) and 0.8 (E3) μm and were fabricated in a 0.5 μm SOI technology on SIMOX substrates. The devices have an effective channel doping density of $1.0x10^{17}$ cm^{-3}, front gate oxide thickness t_{oxf} of about 15 nm, buried oxide thickness t_{oxb} of 390 nm, and a silicon film thickness t_{Si} of about 80 nm.

The I_{DS} vs. V_{GB} curves were recorded with V_{DS} = 0.2 V, a front gate voltage V_{GF} of 0.6 V ($V_{GF} > Vth_{F,acc2}$), and a back gate voltage V_{GB} ranging from -30 to 20 V (steps of 0.10 V). The I_{DS} vs. V_{GF} curves were measured with V_{DS} = 0.2 V, a back gate voltage V_{GB} of 20 V ($V_{GB} > Vth_{B,acc1}$), and a front gate voltage V_{GF} ranging from -3 to 2 V (steps of 0.010 V). All measurements were done using a HP 4145B parameter analyzer.

Figure 11 shows the I_{DS} and $\delta^2 I_{DS}/\delta V_{GB}^2$ curves as a function of the V_{GB}, and figure 12 shows the I_{DS} and $\delta^2 I_{DS}/\delta V_{GF}^2$ curves as a function of the V_{GF} for the device with L_m = 0.8 μm.

Table II summarizes some experimental results of Q_{ox1} and Q_{ox2} values obtained by the proposed method for different SOI nMOSFETs. These results are as expected for the devices used.

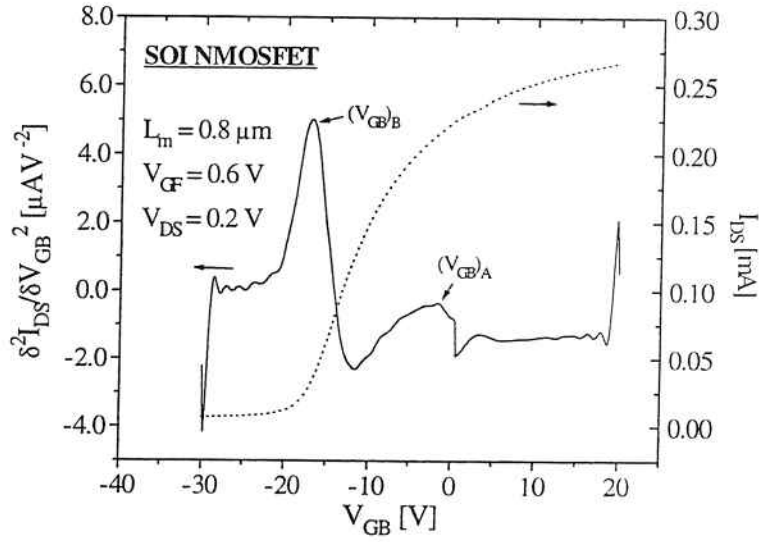


Figure 11: I_{DS} and $\delta^2 I_{DS}/\delta V_{GB}^2$ versus V_{GB} curves for a constant V_{GF} of an SOI nMOSFET, where $(V_{GB})_A$ = -1.60 V and $(V_{GB})_B$ = - 17.00 V.

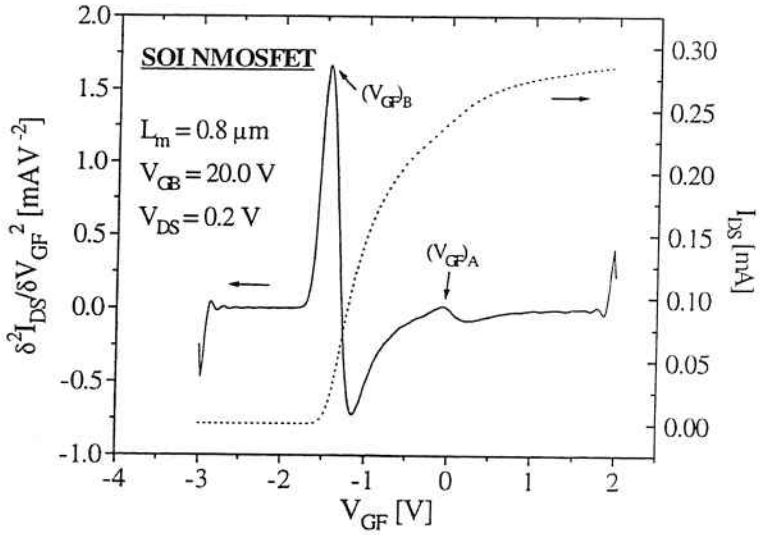


Figure 12: I_{DS} and $\delta^2 I_{DS}/\delta V_{GF}^2$ versus V_{GF} curves for a constant V_{GB} of an SOI nMOSFET, where $(V_{GF})_A$ = -0.06 V and $(V_{GF})_B$ = - 1.45 V.

Table II: Experimental results obtained by the proposed method of the oxide charge densities at front and back interfaces from different devices.

	Method [x 10^{11} cm^{-2}]	
Device	**Q_{ox1}/q**	**Q_{ox2}/q**
E1	2.71	4.49
E2	2.85	4.99
E3	2.78	4.96

5. Conclusions

The effect of the back and front gate voltages on the front and back channel region of fully depleted SOI nMOSFETs was explored using bi-dimensional numerical simulations. A new method to determine the oxide charge densities at front and back interfaces was derived from it. This method was also experimentally validated and good agreement with the simulation results has been obtained.

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BT/PSI/0013 – Estudo de Dispositivos Miniaturizados para Controle do Escoamento de Fluidos – ELIPHAS WAGNER SIMÕES, ROGÉRIO FURLAN

BT/PSI/0014 – Projeto de um Sistema de Sinalização de Tronco E1: Um Estudo de Caso usando o Ambiente Ptolemy – OSCAR W. PEÑA GUILARTE, MARIUS STRUM

BT/PSI/0015 – Obtenção de Filmes de Nitreto de Silício por Deposição Química Assistida por Plasma Acoplado Indutivamente – LUÍS DE S. ZAMBOM, ROGÉRIO FURLAN, RONALDO D. MANSANO

BT/PSI/0016 – Obtenção de Oxinitretos de Porta por Processamento Térmico Rápido Visando a Fabricação de Circuitos Integrados MOS – LEANDRO ZEIDAN TOQUETTI, SEBASTIÃO G. SANTOS FILHO

BT/PSI/0017 – Characterization of Silicon Oxide Thin Films Deposited by TEOS PECVD – ANA NEILDE R. DA SILVA, NILTON I. MORIMOTO

BT/PSI/0018 – Estudo e Caracterização de Filmes Sipos para a Passivação de Dispositivos de Potência – EDUARDO DOS SANTOS FERREIRA, NILTON ITIRO MORIMOTO

BT/PSI/0019 – Simulação, Funcional e Elétrica, de Diodos Controlados por Porta Visando Demonstrar a sua Aplicabilidade como Sensor de Radiação Luminosa – HUGO PUERTAS DE ARAÚJO, SEBASTIÃO GOMES DOS SANTOS FILHO

BT/PSI/0020 – Graded-Channel Fully-Depleted Silicon-on-Insulator Nmosfet for Reducing the Parasitic Bipolar Effects – MARCELO ANTONIO PAVANELLO, JOÃO ANTONIO MARTINO, DENIS FLANDRE

BT/PSI/0021 – FFT para Detecção de Aromas – G. C. SANTOS QUISPE, F. J. RAMIREZ FERNANDEZ

BT/PSI/0201 – Estudo e Aplicação de Litografia por Feixe de Elétrons na Fabricação de Estruturas de Relevo Contínuo para Utilização em Microóptica Integrada – HAMILTON FERNANDES DE MORAES JUNIOR, ANTONIO CARLOS SEABRA

BT/PSI/0202 – Sistemas de Adaptação ao Locutor Utilizando Autovozes – LISELENE DE ABREU BORGES, MIGUEL ARJONA RAMÍREZ

BT/PSI/0203 – A Wideband Down-Converter MMIC with Gain Control for Digital Radio Systems – D. VIVEIROS JR., M. B. PEROTONI, M. A. LUQUEZE, D. CONSONNI, J. G. C. POLOTO

BT/PSI/0204 – Highly Conductive N-Type μc-Si:H Films Deposited at Very Low Temperature – ALEXANDRE MANTOVANI NARDES, ELY ANTONIO TADEU DIRANI

BT/PSI/0205 – Effect of Stencil Alignment on the Solder Beading in SMT Process – FLÁVIO SOUSA SILVA , MAURÍCIO MASSAZUMI OKA

BT/PSI/0206 – Sistema de Reconhecimento de Voz Dependente de Locutor Utilizando-se a Transformada Discreta Cosseno – WASHINGTON LUIS SANTOS SILVA, IVANDRO SANCHES

BT/PSI/0207 – Construção e Caracterização de Diodos N^+P com Contatos Al/Ni/$TiSi_2$ -RONALDO WILLIAN REIS, SEBASTIÃO GOMES DOS SANTOS FILHO

BT/PSI/0208 – Diagnóstico de Falhas em Equipamentos Usando Técnicas de Redes Neurais Artificiais – MARIANA A. AGUIAR, ZSOLT L. KOVÁCS

BT/PSI/0209 – Analysis of the Leakage Drain Current Carriers in SOI MOSFETs Operating at High-Temperatures – MARCELLO BELLODI, JOÃO ANTONIO MARTINO