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Analytical Model for Ballistic 2D Nanotransistors

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Abstract—This paper describes device models for the current-voltage (I–V) and capacitance-voltage (C–V) characteristics of ballistic nanotransistors based on two-dimensional (2D) materials. The proposed methodology introduces a novel, fully analytical, and explicit approach grounded in fundamental physical principles. This approach enables seamless integration into circuit simulators and provides clear insight into device operation. In contrast to the drift-diffusion models commonly found in the literature, this approach accurately describes the ballistic transport regime observed in state-of-the-art 2D nanotransistors. The proposed model was validated against both experimental and *ab initio* numerical simulations from the literature for devices based on molybdenum disulfide (MoS_2) and indium selenide (InSe). The results show excellent agreement with the reference datasets, confirming the model's accuracy and its suitability for designing advanced nanoelectronic devices and circuits.

***Index Terms*—2D materials, analytical model, ballistic nanotransistors, compact model, nanoelectronics.**

I. INTRODUCTION

Silicon has long been the dominant material in the semiconductor industry, particularly for high-density digital-logic integrated circuits (ICs). Major manufacturers have strived to adhere to Moore's Law with silicon, given the maturity and sophistication of its manufacturing processes. The recent breakthrough of stacking gate-all-around nanosheets is expected to sustain scaling until around 2028 [1]. However, as transistor scaling reaches fundamental limits, research must focus on exploring nanomaterials for long-term technological advancement.

A promising solution consists of using two-dimensional materials. Since the discovery of graphene in 2004, these materials have garnered significant scientific interest. Among them, several are semiconductors with performance potentially superior to silicon, facilitating further transistor scaling and industry transition. Their inherent characteristic, of establishing the lower limit of channel thickness reduction, provides exceptional electrostatic control to the field-effect transistor (FET), making them particularly attractive for the next generation of electronics.

Consequently, there has been a surge in research interest in the various configurations of nanotransistors based on two-dimensional materials (2D-FETs), driven by both theoretical investigations, such as ab initio studies and device-level simulations, and experimental advances in the fabrication and characterization of these devices [2]. Also, given the rapid advancement in their fabrication processes, developing compact models becomes crucial to enable integrated circuit synthesis using these novel nanotransistors. Although there are some similarities to silicon MOSFETs, the distinct band structure, electrostatic behavior and carrier transport mechanisms in 2D-FETs widely justify the development of tailored models. As a result, several analytical or semi-analytical treatments have been proposed recently [3]–[12].

Nevertheless, most of the aforementioned analytical formulations employ the drift-diffusion formalism and disregard ballistic carrier transport, despite recent experimental demonstrations of ballistic 2D-FETs [13], [14]. The relevant exception regarding ballistic transport is the work by Prentki *et al*. [3] which develops two models based on Landauer formalism. Their models are physics-based, but their first routine requires an iterative solution for MOS electrostatics and Fermi–Dirac statistics, whereas the second is valid only above threshold and uses Fermi-Dirac integrals. As such, neither solution is fully suitable for standard compact modeling.

In addition, much of the analytical models available in the literature are dedicated to Schottky-barrier FETs (SB-FETs) and do not apply to the device configuration discussed here. Although SB-FETs are well-suited for experimental investigations, the development of corresponding compact models is less imperative because these devices are not intended to be building blocks for high-density or high-

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performance integrated circuits. Instead, SB-FETs are being explored for niche applications, such as cryogenic electronics and sensing devices [15].

In contrast, the target of our paper is a device configuration similar to the standard metal-oxide-semiconductor FET (MOSFET) that can attract significant interest for nanoelectronics applications, particularly given the ability of 2D semiconductors to operate in ballistic current regimes. Accordingly, our goal is to develop fully explicit, analytical, and physics-based models. In this work, we expand and detail the models first described in our preliminary publications [16]–[18]. We present a comprehensive model to calculate the current-voltage (I–V) and capacitance-voltage (C–V) characteristics of several distinct configurations of ballistic nanotransistors, incorporating distinct features of different two-dimensional materials. In contrast to prevailing drift-diffusion formalisms, our approach is specifically tailored for the ballistic transport regime observed in state-of-the-art 2D nanotransistors. The model is validated against recently published experimental results that demonstrate ballistic transport in InSe [13] and MoS_2 [14] based transistors. Moreover, it was designed to be suitable for seamless integration into circuit simulators, while providing clear physical insight into device operation.

The paper is structured as follows: Section II introduces the device and its electrostatic model, including the analysis of carrier concentration, the band diagram, and an approximate analytical solution to the Poisson equation for the entire operating range. Next, we elaborate on the current characteristics in the ballistic regime, calculated based on Landauer formalism, and the capacitance characteristics. Section III validates the model with numerical and experimental data concerning different two-dimensional materials, highlighting their unique features. Finally, we draw our conclusions in Section IV.

II. Methods and Procedures

Fig. 1 depicts the device of interest. The layer structure starts from the substrate, usually highly-doped silicon, followed by an insulator, typically silicon dioxide. On top of the insulator lies the two-dimensional semiconductor, followed by the gate oxide, which can also be made of silicon dioxide or other insulating material with a higher dielectric constant. Without loss of generality, we assume an n-type device with a density of donor impurity N_D given in cm^{-2}. In any case, the formulation presented here can be easily extended to the p-type transistor.

The first step in the modeling process is to establish a charge-control relationship between the carrier concentration in the channel and the bias voltage applied to the gate terminal, considering there is no carrier flow. Therefore, we set $V_{ds} = 0$ and the Fermi level potential is invariant along the channel.

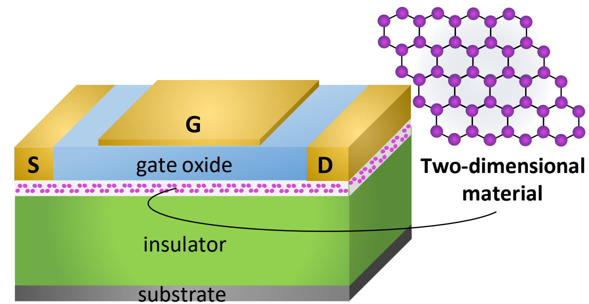

Fig. 1. Three-dimensional schematic of a 2D-FET, showing the substrate, insulator, semiconductor channel (highlighted), gate oxide, and the source (S), gate (G), and drain (D) contacts.

A. Carrier Concentration

The carrier (electron) concentration in the 2D semiconductor is given by

$$n_s = \int_{E_c}^{\infty} g_{2D}(E) f(E - E_F) dE, \tag{1}$$

where $g_{2D}(E)$ is the two-dimensional density of states, $f(E - E_F)$ is the Fermi-Dirac distribution, and E_F is the Fermi level energy. Due to quantum size effects, the conduction band of 2D materials consists of discrete energy levels. However, since carriers are confined within a thickness of ~1 nm, these levels are widely spaced and typically only the first level is significantly occupied. As a consequence, only the ground state will be considered in the ensuing calculations. This ground state position corresponds to the bottom of the conduction band for these materials and will be denoted simply as E_c throughout the paper.

The density of states in two-dimensional systems is constant at each energy level and can be formally described by the Heaviside step function, that is,

$$g_{2D}(E) = \sum_j g_j \, \mathrm{H}(E - E_j), \tag{2}$$

where j is the index labeling each discrete energy level within the conduction band. Again, in practice, only the first level needs to be considered, and the notation is simplified to a constant value g_{2D}. Additionally, since g_{2D} takes into account the specific features of each two-dimensional material, such as the contribution of multiple valleys, we will leave a more detailed discussion to Section III.

Next, we can define $E_c = -q\varphi$, the channel electrostatic potential distribution, and $E_F = -qV$, so that we have that

$$n_s = \frac{m^* k_B T}{\pi \hbar^2} \ln\left[1 + \exp\left(\frac{\varphi - V}{\phi_T}\right)\right] \tag{3}$$

is the carrier concentration density within the framework of Fermi-Dirac statistics. In this expression, $\phi_T = k_B T / q$ is the thermal voltage, being k_B the Boltzmann constant, T the temperature, and q the fundamental charge.

To use the above equation to obtain an expression for the I–V characteristics of the device would require special functions or lead to integrals that need to be numerically

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solved. Therefore, to obtain fully analytical expressions, it is convenient to assume a non-degenerate semiconductor and employ the Maxwell-Boltzmann approximation:

$$n_s = N_{\mathrm{DoS}} \exp\left(\frac{\varphi - V}{\phi_{\mathrm{T}}}\right), \tag{4}$$

where $N_{\mathrm{DoS}} = g_{2D} k_B T$.

The use of the Boltzmann statistics is justified because doping 2D materials remains a significant technological challenge and the assumption of an undoped or lightly doped channel is not only realistic but also consistent with typical experimental conditions so far.

Also, an in-depth analysis, developed by Cao *et al.* [7] in the context of transition metal dichalcogenides (TMDs), shows that the high density of states prevents the Fermi level from penetrating deeply into the conduction band. In particular, even though a higher doping concentration would naturally place the Fermi level closer to the conduction band at $V_{gs} = 0$, such that degeneracy would occur more readily as the gate bias increases, this effect is mitigated by the large density of states, thereby preserving the validity of the non-degenerate approximation over a wider bias operating range, even for doped channels. This shielding effect should be even more pronounced in the case of very anisotropic materials, such as phosphorene, for instance, due to their higher density-of-states effective mass, when compared to TMDs.

B. Conduction Band Profile

Fig. 2 depicts the conduction band profile for a 2D-FET. Analyzing from left to right, we first encounter the gate metal contact, characterized by the work function ϕ_M, given in volts. The applied gate voltage (V_{gs}) represents the shift of the Fermi level in the metal with respect to the semiconductor. Next, we have the potential drop across the gate oxide (φ_{ox}), and the semiconductor channel, characterized by the electron affinity (χ_S), given in electron-volts. The work function of the two-dimensional semiconductor can be calculated by

$$\phi_S = \frac{\chi_S}{q} + \frac{E_g}{2q} - \phi_T \ln\left(\frac{N_D}{n_i}\right), \tag{5}$$

where E_g is the bandgap energy and n_i is the intrinsic carrier concentration.

In general, $N_D \cong n_i$ for these nanotransistors, which places the Fermi level of the semiconductor near the middle of the bandgap. Consequently, these nanotransistors are accumulation FETs. In other words, the semiconductor transitions from a regime of carrier depletion in the OFF state to a regime of carrier accumulation in the ON state [19].

The flatband voltage is defined from the band diagram as

$$V_{FB} = \phi_{MS}. \tag{6}$$

As such, oxide charges and interface traps are not included into the model, since we are focusing on the upper limit of high-performance devices.

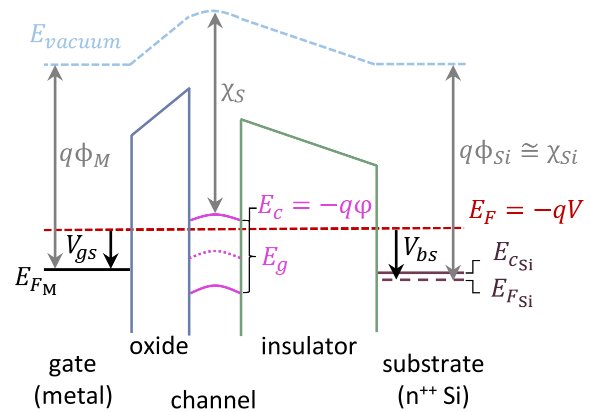

Fig. 2. Conduction band profile of a 2D-FET in the accumulation condition ($V_{gs} > V_{FB}$). A highly-doped n-type silicon substrate is assumed.

Next, the substrate is typically made of highly n-doped silicon, so the work function of silicon is approximately χ_{Si}/q. A fixed voltage V_{bs} can be applied to shift the electrostatic profile along the channel with respect to the Fermi level at the source side, thereby altering the electrostatic characteristics of the nanotransistor. Assuming a highly doped semiconductor substrate and a thick insulator, the band bending within the silicon substrate can be neglected.

Finally, the structures in Figs. 1 and 2 can also be modified to model a double-gate (DG) device. In this case, the insulator and substrate are replaced by the gate oxide and gate metal, respectively, and the gate voltage V_{gs} is applied symmetrically at both ends, instead of the fixed voltage V_{bs} on the substrate.

C. Poisson Equation

To establish the charge control relation, it is first necessary to solve the Poisson equation governing this family of devices. Following the approach by Cao *et al.* [7], the 2D-FET can be analyzed according to the schematic shown in Fig. 3.

In this two-dimensional representation, the gate voltage is applied along the z-axis, and the current flow occurs in the x-direction. There is no potential difference along the y-axis, which is parallel to the cross-sectional area of the channel, of width W and length L. The gate oxide, semiconductor, and insulator have thicknesses t_{ox}, t_s and t_i, and electric permittivities ε_{ox}, ε_s and ε_i, respectively.

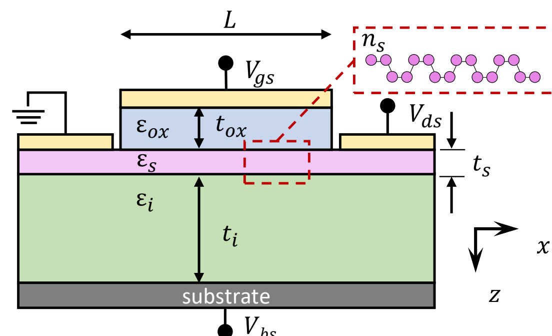

Fig. 3. Two-dimensional schematic of a 2D-FET for electrostatic analysis.

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Because the channel consists of only a few layers of a 2D material, it is reasonable to assume that $\varphi(x,y,z) \approx \varphi(x)$. In other words, any variations of the electrostatic potential in the y and z directions can be disregarded and the Poisson equation, which is valid for all bias regimes, can be written as

$$\frac{d^2\varphi}{dx^2} - \frac{\varphi}{\lambda^2} + \frac{C_{ox}(V_{gs} - V_t)}{\varepsilon_s t_s} = \frac{qN_{\mathrm{DoS}}}{\varepsilon_s t_s}\exp\left(\frac{\varphi - V}{\phi_{\mathrm{T}}}\right), \quad (7)$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance, λ is the characteristic length of the 2D-FET, given by

$$\lambda = \sqrt{\frac{\varepsilon_s t_s t_{ox} t_i}{\varepsilon_{ox} t_i + \varepsilon_i t_{ox}}}, \quad (8)$$

and V_t is the threshold voltage, expressed as

$$V_t = V_{FB} + \frac{C_i(V_{bs} - V_i) - qN_D}{C_{ox}}, \quad (9)$$

where the term V_i corresponds to the difference between the work functions of the semiconductor and the substrate, whereas $C_{\mathrm{i}} = \varepsilon_i/t_i$ is the capacitance of the insulator.

With slight modifications, the Poisson equation for a double-gate 2D-FET becomes:

$$\frac{d^2\varphi_{\mathrm{DG}}}{dx^2} - \frac{\varphi_{\mathrm{DG}}}{\lambda_{\mathrm{DG}}^2} + \frac{2C_{ox}(V_{gs} - V_{t_{\mathrm{DG}}})}{\varepsilon_s t_s} = \frac{qN_{\mathrm{DoS}}}{\varepsilon_s t_s}\exp\left(\frac{\varphi_{\mathrm{DG}} - V}{\phi_{\mathrm{T}}}\right), \quad (10)$$

where λ_{DG} is the characteristic length of the double-gate 2D-FET, given by

$$\lambda_{\mathrm{DG}} = \sqrt{\frac{\varepsilon_s t_s t_{ox}}{2\varepsilon_{ox}}}, \quad (11)$$

and $V_{t_{\mathrm{DG}}}$ is the threshold voltage of the double-gate 2D-FET, expressed as

$$V_{t_{\mathrm{DG}}} = V_{FB} - \frac{qN_D}{2C_{ox}}. \quad (12)$$

D. Approximate Analytical Solution of the Poisson Equation

Next, it is necessary to analytically solve the Poisson equation above to obtain the behavior of the electrostatic potential along the channel and subsequently derive expressions for the current and capacitance characteristics. Taking the gradual channel approximation, the second derivative in (7) can be set to zero. Rearranging the terms, we derive an equation that relates the electrostatic potential of the channel to the bias voltage at the gate contact:

$$(C_{ox} + C_i)\varphi + qN_{\mathrm{DoS}}\exp\left(\frac{\varphi - V}{\phi_{\mathrm{T}}}\right) = C_{ox}(V_{gs} - V_t). \quad (13)$$

Equation (13) is a transcendental equation for $\varphi(x)$; therefore, analytical approximations are required to obtain an explicit solution for the potential as a function of the applied bias voltages. Specifically, to obtain a fully analytical and explicit expression for the potential, one can expand the exponential term in (13) into a Taylor series about a fixed expansion point Φ.

$$\exp\left(\frac{\varphi}{\phi_{\mathrm{T}}}\right) = \exp\left(\frac{\Phi}{\phi_{\mathrm{T}}}\right)\sum_{j=0}^{\infty}\frac{1}{j!}\left(\frac{\varphi - \Phi}{\phi_{\mathrm{T}}}\right)^j. \quad (14)$$

The accuracy of this expansion within a range of interest will primarily depend on the number of terms retained in the approximation and the choice of the expansion point Φ. Since the expansion results in a polynomial function, retaining n terms implies finding the roots of an nth-degree polynomial, which is a rather laborious task for $n > 2$. Also, the use of a single and static expansion might not be suitable to provide accurate roots for the whole range of interest.

As an alternative, we have worked out a new approach, which we originally applied to find the eigenstates of asymmetric quantum wells [20]. In this approach, we use a sliding expansion point Φ, which varies accordingly to a mapping function obtained on the basis of a graphical inspection of φ within a given range of interest. In our case, this analysis to obtain the mapping function is facilitated since the asymptotic behavior of $\varphi(V_{gs})$ at the end points of the range of interest can be easily computed and typical values for the transistor fabrication parameters are known. We have found that a simple function of the form

$$\Phi = 2\phi_T + \frac{2[\alpha(V_0 - V_t) - 2\phi_T]}{1 + \exp[d(V_{gs} - V_0)]} \quad (15)$$

is an optimal choice, where V_0 and d are fixed parameters, and $\alpha = C_{ox}/(C_{ox} + C_i)$ [17]. The parameter V_0 essentially governs the behavior in deep subthreshold regime, $V_{gs} \ll V_t$, whereas d assures a smooth transition between the asymptotic behaviors of φ when $V_{gs} \approx V_t$.

It is worth mentioning that the mapping function, eq. (15), and its associated parameters are always the same for each device analyzed and remains unaltered throughout the simulations. As such, the solution for φ (and the overall model) will remain explicit, and one only needs to find the root of a second-order polynomial.

As it will be shown in the next subsection, calculating the drain current using the Landauer ballistic transport formalism requires knowing the potential only at the source side of the channel. Therefore, eq. (13) needs to be solved only in the special case that $V = 0$. Then, further analysis of eq. (13), reveals that only the first two terms of the expansion in eq (14), are necessary to obtain fair accuracy, resulting in a simple compact expression for $\varphi(V_{gs})$ at the source side:

$$\varphi = \frac{qN_{\mathrm{DoS}}(\Phi - \phi_T)\exp\left(\frac{\Phi}{\phi_T}\right) + \phi_T C_{ox}(V_{gs} - V_t)}{qN_{\mathrm{DoS}}\exp\left(\frac{\Phi}{\phi_T}\right) + \phi_T(C_{ox} + C_i)}. \quad (16)$$

As shown in Fig. 4(a), the proposed approximation shows excellent agreement with the exact solution. Furthermore, if necessary, the accuracy of this method can be readily improved by retaining one more term in eq. (14) and finding the roots of a quadratic polynomial.

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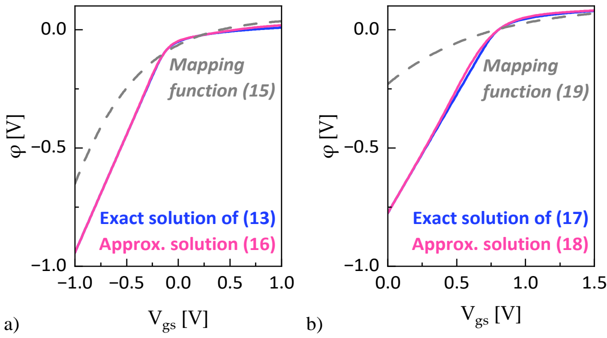

Fig. 4. Comparison between the exact and the approximate solutions for the electrostatic potential of: a) Single-gate, monolayer MoS_2 channel with $N_D = 10^{12}$ cm^{-2}, Al_3O_2 gate oxide ($t_{ox} = 2.8$ nm), SiO_2 insulator ($t_i = 270$ nm), Ti gate, and n^{++} Si substrate. b) Double-gate, trilayer InSe channel with $N_D = 10^{11}$ cm^{-2}, HfO_2 gate oxide ($t_{ox} = 2.6$ nm), and Au gate. The respective mapping functions are also shown.

In addition, for a double-gate nanotransistor, we have the following relation:

$$2C_{ox}\varphi_{\mathrm{DG}}(x) + qN_{\mathrm{DoS}} \exp\left[\frac{\varphi_{\mathrm{DG}} - V}{\phi_{\mathrm{T}}}\right] = 2C_{ox}(V_{gs} - V_t). \quad (17)$$

Applying the same steps as before, a simple compact expression for $\varphi_{\mathrm{DG}}(V_{gs})$ is obtained as

$$\varphi_{\mathrm{DG}} = \frac{qN_{\mathrm{DoS}}(\Phi_{\mathrm{DG}} - \phi_T)\exp\left(\frac{\Phi_{\mathrm{DG}}}{\phi_T}\right) + 2\phi_T C_{ox}(V_{gs} - V_t)}{qN_{\mathrm{DoS}}\exp\left(\frac{\Phi_{\mathrm{DG}}}{\phi_T}\right) + 2\phi_T C_{ox}}, \quad (18)$$

where the expansion value can be determined by [16]

$$\Phi_{\mathrm{DG}} = 4\phi_T + \frac{2(V_0 - V_{t_{\mathrm{DG}}} - 4\phi_T)}{1 + \exp[d(V_{gs} - V_0)]}. \quad (19)$$

Fig. 4(b) also demonstrates the excellent agreement between the exact behavior and the proposed approximation for double-gate devices.

E. Ballistic Current-Voltage Characteristics

The superior electrostatic channel control provided by the atomic thickness of two-dimensional materials potentially allows the physical length of the transistor to be reduced below the carrier mean free path, ℓ, which is the average distance an electron can travel freely, without scattering events. In other words, if $L \ll \ell$, carriers move between source and drain without significant scattering, characterizing a ballistic transport. In this regard, several numerical studies have addressed ballistic features in 2D materials [21], [22], [23], [24]. More recently, experimental demonstrations of 2D nanotransistors approaching [25] or reaching [13], [14] the ballistic regime have been reported, indicating the increasing maturity of fabrication processes.

For analytical modeling in ballistic or quasi-ballistic regimes, the Landauer formalism is commonly employed [26], [27], [28], [29]:

$$I_{ds} = \frac{2q}{h}\int_{-\infty}^{\infty} \mathcal{T}(E)\mathcal{M}(E)[f_s(E) - f_d(E)]dE, \quad (20)$$

where h is the Planck constant, $\mathcal{T}(E)$ is the transmission coefficient, $\mathcal{M}(E)$ is the mode transmission distribution for the channel, and $f_s(E) - f_d(E)$ is the difference between the Fermi distributions at the source and drain contacts.

In the framework of the Landauer formalism, the source and drain contacts are seen as electron reservoirs separated by the potential barrier in the channel, which is reduced when a voltage is applied to the gate contact. Then, when a voltage difference V_{ds} is present along the channel, we have $E_{fd} = E_{fs} - qV_{ds}$, and this imbalance allows a current flow.

The transmission coefficient $\mathcal{T}$ describes the probability of an electron at the source contact to enter the channel and reach the drain contact without scattering. Consequently, for the ballistic case, $\mathcal{T} = 1$. In the quasi-ballistic case, $\mathcal{T}$ assumes a value close to unity, indicating that there is still some residual but relevant scattering in the channel. For simplicity, here we assume $\mathcal{T}(E) = \mathcal{T}_0$, being $\mathcal{T}_0$ an effective and constant value representing this residual amount of channel scattering.

In the Landauer formalism, the mode transmission distribution $\mathcal{M}(E)$ describes how an electron with energy E travels along the channel. A detailed explanation can be found in [29]. In essence, $\mathcal{M}(E)$ is proportional to the product of the density of states and the average carrier velocity at a given energy E, thus combining the availability of states and their contribution to current flow:

$$\mathcal{M}(E) = \frac{2\mathrm{W}g_{2D}}{\pi}\sqrt{\frac{2(E - E_c)}{m_t^*}}, \quad (21)$$

where m_t^* is the carrier effective mass at the transport direction.

With these considerations in mind, one can solve (20) to obtain an expression for I_{ds}:

$$\begin{gathered} I_{ds} = I_0[\mathcal{F}_{1/2}(\xi_{fs}) - \mathcal{F}_{1/2}(\xi_{fd})], \\ I_0 = \frac{2q\mathcal{T}_0\mathrm{W}k_BTg_{2D}}{h\pi}\sqrt{\frac{2\pi k_BT}{m_t^*}}, \\ \xi_{fs} = \frac{E_{fs} - E_c(x=0)}{k_BT}, \\ \xi_{fd} = \frac{E_{fs} - qV_{ds} - E_c(x=0)}{k_BT} = \xi_{fs} - \frac{V_{ds}}{\phi_{\mathrm{T}}}, \end{gathered} \quad (22)$$

where $E_c(x = 0)$ corresponds to the value of the conduction band (first discrete level) at the source side. $E_{fs} = -qV_s = 0$ in this formulation and, in the context of the gradual channel approximation (GCA), $E_c(x = 0) = -q\varphi_s$. Then

$$\begin{gathered} \xi_{fs} = \frac{-E_c(x=0)}{k_BT} = \frac{\varphi_s}{\phi_{\mathrm{T}}}, \\ \xi_{fd} = \frac{-qV_{ds} - E_c(x=0)}{k_BT} = \frac{\varphi_s - V_{ds}}{\phi_T}. \end{gathered} \quad (23)$$

Therefore, in a first approximation under the Landauer formalism, the I–V characteristics are dictated primarily by the electrostatic potential at the source side of the channel. This potential, φ_s was derived previously in Eq. (16).

Inspecting eq. (22), we have the special Fermi-Dirac integral function of index 1/2, $\mathcal{F}_{1/2}(\xi)$. Assuming the Boltzmann approximation, $\mathcal{F}_{1/2}(\xi)$ reduces to $\exp(\xi)$. Equation (22) can

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then be rewritten in terms of the charge density at the source side, $Q_s(V_{gs},V_{ds}) = -qn_s(V_{gs},V_{ds})$:

$$I_{ds} = \mathcal{T}_0 W\left|Q_s(V_{gs},V_{ds})\right|\sqrt{\frac{2k_BT}{\pi m^*}}\left[\frac{1-\exp(-V_{ds}/\phi_T)}{1+\exp(-V_{ds}/\phi_T)}\right],$$
$$Q_s(V_{gs},V_{ds}) = -\frac{qN_{DoS}}{2}\exp\left(\frac{\varphi_s}{\phi_T}\right)\left[1+\exp\left(-\frac{V_{ds}}{\phi_T}\right)\right]. \quad (24)$$

In summary, we have obtained a general expression for the I–V characteristics considering ballistic transport in 2D-FETs. By working out the above expression, it can be rewritten as:

$$I_{ds} = I_0\exp\left[\frac{\varphi(V_{gs})}{\phi_T}\right]\left[1-\exp\left(-\frac{V_{ds}}{\beta\phi_T}\right)\right]. \quad (25)$$

Since carriers move through the channel without significant scattering, the I–V characteristics of these devices become highly dependent on the process of carrier injection and collection at the source and drain contacts, respectively. Therefore, the empirical non-ideality factor β was included in the above expression to phenomenologically capture the combined impact of contact resistance and other deviations from ideal ballistic transport in experimental results.

F. Capacitance-Voltage Characteristics

The explicit expression for the electrostatic potential also allows for the calculation of the gate capacitance of these devices, written as a series combination of the oxide capacitance and the quantum capacitance, that is

$$C_{gg} = \frac{C_{ox}C_Q}{C_{ox}+C_Q}. \quad (26)$$

The quantum capacitance is defined as the derivative of the charge in the two-dimensional channel with respect to the electrostatic potential. Also known as electrochemical capacitance [30], this term refers to the two-dimensional density of states and the variation on the filling of the discrete energy levels in the conduction band with the changes in the channel potential. Considering the Fermi-Dirac distribution to describe the carrier concentration, we have

$$C_Q = q\frac{\partial n_s}{\partial\varphi} = \frac{q^2N_{DoS}}{k_BT}\left[\frac{\exp\left(\frac{\varphi-V}{\phi_T}\right)}{1+\exp\left(\frac{\varphi-V}{\phi_T}\right)}\right]. \quad (27)$$

III. Results

For digital-logic applications of nanodevices, the most attractive two-dimensional semiconductors so far are transition metal dichalcogenides, such as molybdenum disulfide, and indium selenide. The first nanotransistors based on MoS_2 presented an excellent ON-OFF ratio, with experimentally reported values of 10^8, and carrier mobilities up to 200 $cm^2V^{-1}s^{-1}$ [31]. Later, a three-layer indium selenide device provided the best experimental performance of a 2D-FET recorded to date [13]. More recently, similar results were also obtained for three-layer molybdenum disulfide [14]. For these reasons, devices based on these two materials were chosen to validate our model.

A. Molybdenum Disulfide

Transition metal dichalcogenides (TMDs) are layered materials composed of MX_2 structure, where M is a transition metal atom, and X is a chalcogen atom (sulfur, selenium, or tellurium). The monolayers of most semiconductor TMDs have a direct bandgap at the K point of the first Brillouin zone. However, they exhibit a second valley in the conduction band with an energy difference $\Delta\mathcal{E}_c$ to the main valley that is very small, comparable to k_BT. This second valley is located at the Q point, an intermediate position to the K and Γ points, and computational calculations suggest that it contributes significantly to the total current of TMD-based nanotransistors [32].

The contribution of these valleys is taken into account when calculating the output drain current. Specifically, in our particular case of the current amplitude where the channel material is a TMD, eq. (22) for I_0 becomes:

$$I_0 = \mathcal{T}_0\frac{qk_BTW}{2\pi\hbar^2}\left[g_Km_K^*\sqrt{\frac{2k_BT}{\pi m_K^*}} + g_Qm_Q^*\sqrt{\frac{2k_BT}{\pi m_Q^*}}\exp\left(-\frac{\Delta E_c}{k_BT}\right)\right], \quad (28)$$

where $g_s = 2$ is the degeneracy factor due to spin, g_i and m_i^* are, respectively, the degeneracy factor and effective mass corresponding to the ith valley considered. Given the crystalline structure of TMDs, $g_K = 2$ and $g_Q = 6$, which also increases the contribution of the secondary valley to the overall current.

In other words, the use of the Landauer formalism under the Boltzmann approximation for MoS_2 nanotransistors leads to a tailored current expression comprising two additive contributions: one from the K valley and another from the Q valley, thermally activated via the Boltzmann factor $\exp\left(-\frac{\Delta E_c}{k_BT}\right)$. This term is not present in eq. (22), which is a general expression considering a single valley.

The first experimental dataset selected to validate our model corresponds to a three-layer MoS_2 nanotransistor ($t_s \approx 2$ nm) with $L = 10$ nm [14]. Their fabrication method employs a novel yttrium-doping technique to achieve ohmic contacts with resistance as low as 69 Ω-μm. At room temperature, the mean free path value extracted from experimental data for this nanotransistor was $\ell \approx 4$ nm, which is smaller than the physical channel length. However, as pointed out by the authors in [14], the effective channel length is reduced to approximately 1-2 nm under high-field conditions. For this reason, they observed high ON-current levels due to ballistic transport.

As shown in Fig. 5, the model accurately describes the I–V characteristics of this device using a fitting parameter $\beta = 8$. This parameter empirically accounts for a deviation from the fully ballistic transport in the linear region of the output curve, as discussed above, causing a low-field channel resistance which is much higher than would be expected. In the validation process, we have tuned β to fit the experimental I_{ds}–V_{ds} curves in the linear region without changing the other physical parameters, thus ensuring consistency with the analytical formulation. It is important to stress that, for a given device, the value of β is always the same, for all simulation points (i.e., every bias condition) in the I–V and C–V curves.

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Next, the value of the threshold voltage $V_t = 0.64$ V is extracted by fitting the measured (I_{ds}–V_{gs}) characteristics. Although our framework provides a physics-based expression for V_t (see Eqs. 9 and 12), this adjustment is necessary on account of the device-to-device variability and other process-dependent effects inherent in maturing 2D technologies.

The validity of our final pair of parameters is unequivocally demonstrated by the model ability to simultaneously achieve an excellent fit for both the output (I_{ds}–V_{ds}) and the transfer (I_{ds}–V_{gs}) characteristics, using a single, consistent pair of fixed β and V_t for each device. An arbitrary compensation between parameters do not hold across these two distinct curves for multiple devices.

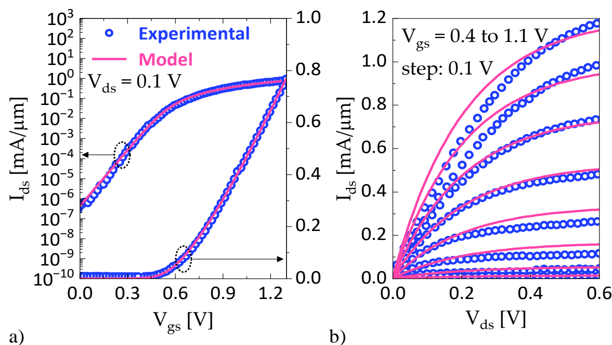

Fig. 5. Validation of the model for the I–V characteristics, when compared to experimental data [14]. a) Linear and logarithmic scale $I_{ds} - V_{gs}$. b) $I_{ds} - V_{ds}$ for different values of V_{gs}. Parameters: MoS_2 channel with $t_s = 1.95$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, HfO_2 gate oxide ($t_{ox} = 2.6$ nm), identical oxide insulator, Ti gate, n^{++} Si substrate, $L = 10$ nm. The threshold voltage was set to $V_t = 0.64$ V. Fitting parameter: β = 8.

Fig. 6 shows the behavior of these MoS_2 nanodevices with respect to temperature variations. In log scale, the subthreshold slope varies with $k_B T$, as expected. In addition, the slope remains almost constant with V_{gs} in 250 and 300 K, suggesting that nearly ideal ohmic contacts were achieved [14].

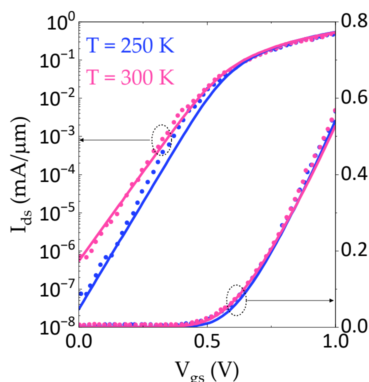

Fig. 6. Validation of the transfer characteristics (I_{ds}–V_{gs}) in linear and log scale considering temperatures of 250 and 300 K. Solid lines are results from our model whereas dotted lines are experimental data from [14]. Parameters: MoS_2 channel with $t_s = 1.95$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, HfO_2 gate oxide ($t_{ox} = 2.6$ nm), identical oxide insulator, Ti gate, n^{++} Si substrate, $L = 10$ nm and $V_{ds} = 0.5$ V. The threshold voltage was set to $V_t = 0.48$ V. Fitting parameter: β = 8.

Fig. 7 illustrates the validation of the C–V model, eq. (26), when compared to simulation data [33] for a double-gate 2D-FET with a monolayer MoS_2 channel ($t_s = 0.65$ nm) and oxide with an equivalent oxide thickness (EOT) of 0.5 nm. The threshold voltage was set to $V_{t_{DG}} = 0.22$ V. The result shows that the model accurately describes the capacitance-voltage characteristics of this device.

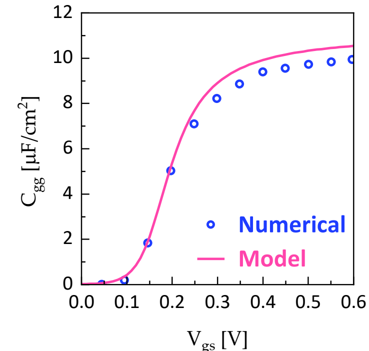

Fig. 7. Validation of the C–V characteristics when compared to simulation data [33] considering a double-gate nanotransistor. Parameters: MoS_2 channel with $t_s = 0.65$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, and SiO_2 gate oxide ($t_{ox} = 0.5$ nm). The threshold voltage was set to $V_{t_{DG}} = 0.22$ V.

Fig. 8 illustrates another validation of the C–V model, this time with experimental data [34], for a single-gate 2D-FET with a monolayer MoS_2 channel ($t_s = 0.65$ nm), gate oxide composed of 10 nm Al_2O_3 and 1 nm Y_2O_3, and a Si substrate below a 90 nm SiO_2 layer. The threshold voltage was set to $V_t = -2$ V, and the gate capacitance was set to $C_{ox} = 0.41$ μF/cm^2, according to the measured values. This transistor has a gate length of ~20 μm, so it cannot be classified as ballistic. Nevertheless, the result demonstrates that our model can still accurately describe the capacitance behavior of this device, as the C–V characteristics do not depend on the transport nature. The small discrepancy just below the threshold is attributed to interface trapping effects, as comprehensively discussed by the authors in [34].

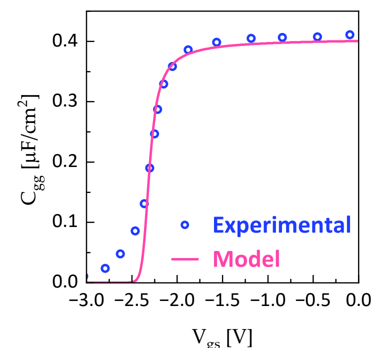

Fig. 8. Model validation for the C–V characteristics when compared to experimental data [34] considering a single-gate transistor. Parameters: MoS_2 channel with $t_s = 0.65$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, gate oxide with $C_{ox} = 0.41$ μF/cm^2, Si substrate, SiO_2 insulator (90 nm). The threshold voltage is $V_t = -2$ V.

B. Indium Selenide

Semimetal chalcogenides (SMCs) are layered materials similar to TMDs, but with a MX-type structure, where M is a semimetal atom (such as gallium or indium) instead of a transition metal, and X is a chalcogen atom (sulfur, selenium, or tellurium). The SMC that has attracted the most interest is indium selenide (InSe), as it displays a bandgap of around 1.5

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eV and mobility of the order of 10^3 $cm^2V^{-1}s^{-1}$ [35].

Recently, InSe 2D-FETs have also been reported to exhibit ballistic transport [13]. In a remarkable achievement, the performance of these devices fabricated is comparable to or even surpasses those of commercial FinFETs (for 10 nm technology node). For instance, a record high transconductance of 6 mS/μm was measured, revealing the enormous potential of this material for the future of nanoelectronics.

Thus, the results provided by our model are also contrasted with the experimental measurements for these nanotransistors fabricated with three layers of InSe ($t_s \approx 2.4$ nm) and $L = 10$ nm [12]. At room temperature, the mean free path estimated for this material is $\ell = 27.76$ nm (see Appendix). It is important to note that the mobility used in this estimation was derived from *ab initio* simulations. Experimentally, the effective mobility is often significantly lower than predicted, making the mean free path presented here an upper-limit value. Nevertheless, as previously discussed for the MoS_2 nanotransistor, the ballistic regime is readily achievable under high-field conditions.

Fig. 9 validates the transfer characteristics (I_{ds}–V_{gs}) predicted by our model, showing excellent agreement with measured data. Using two distinct samples, Fig. 9(a) demonstrates accuracy in both logarithmic and linear scales, whereas Fig. 9(b) indicates that our model yields an idealized description of the subthreshold slope and highlights the need for additional work to fully incorporate short-channel effects, such as the drain-induced barrier lowering (DIBL) effect observed in the experimental data.

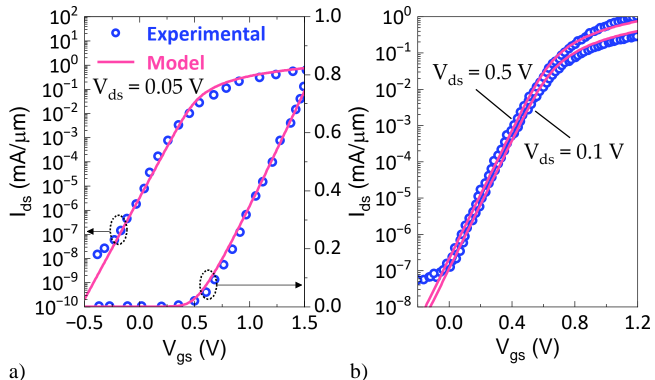

Fig. 9. Validation of the model for the transfer characteristics ($I_{ds} - V_{gs}$), when compared to experimental data [13]. a) Linear and logarithmic scale curves for $V_{ds} = 0.05$ V [18]. The threshold voltage was set to $V_t = 0.5$ V. b) Logarithmic scale curves for $V_{ds} = 0.1$ and 0.5 V. The threshold voltage was set to $V_t = 0.61$ V and the saturation current was set to $0.3I_0$. Parameters: InSe channel with $t_s = 2.4$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, HfO_2 gate oxide ($t_{ox} = 2.6$ nm), identical oxide insulator, Ti gate, n^{++} Si substrate, $L = 10$ nm. Fitting parameter: β = 5.

Our roadmap to address this limitation involves improving the electrostatic model, by moving beyond the gradual channel approximation. The goal is to develop an analytical solution to the 2D Poisson equation to obtain an enhanced potential expression which intrinsically includes DIBL and other short-channel effects, such as subthreshold-slope degradation. Although the unification of this more complex electrostatic solution with the Landauer transport formalism is a non-trivial extension, it provides a clear path for future work. Integrating this improved potential into the ballistic transport framework described here will enhance our model capabilities in the case of aggressively scaled devices, where short channel effects are more pronounced.

Fig. 10 validates the output characteristics (I_{ds}–V_{ds}) for two different samples. For the first sample (Fig. 10(a)), a fitting factor of β = 8 was applied to match the experimental data. In contrast, for the second sample (Fig. 10(b)), a factor of β = 5 was used to account for the reduced contact resistance, reported as 62 Ω-μm by the authors.

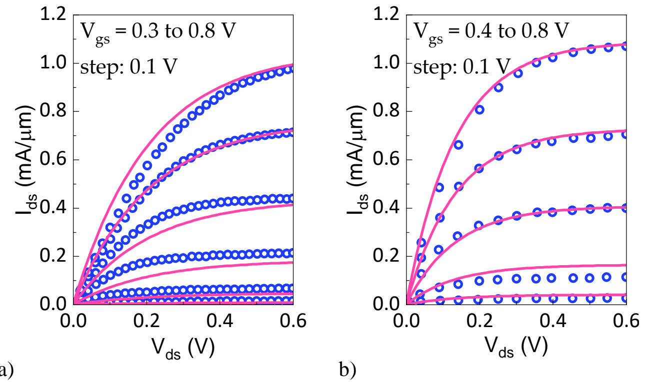

Fig. 10. Validation of the output I–V characteristics with experimental data [13]. a) Sample #1 with fitting factor β = 8. b) Sample #2 with fitting factor β = 5 [18]. Parameters: InSe channel with $t_s = 2.4$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, HfO_2 gate oxide ($t_{ox} = 2.6$ nm), identical oxide insulator, Ti gate, n^{++} Si substrate, $L = 10$ nm. The threshold voltage was set to $V_t = 0.5$ V.

As it was done in the case of the MoS_2 channel device, Fig. 11 illustrates the impact of temperature variations on the InSe nanotransistors DC output characteristics. Again, the subthreshold slope follows the expected log scale dependence with the temperature.

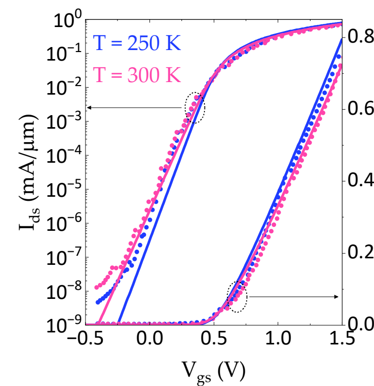

Fig. 11. Validation of the transfer characteristics (I_{ds}–V_{gs}) in linear and log scale considering temperatures of 250 and 300 K. Solid lines are results from our model and dotted lines are experimental data from [13]. Parameters: InSe channel with $t_s = 2.4$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, HfO_2 gate oxide ($t_{ox} = 2.6$ nm), identical oxide insulator, Ti gate, n^{++} Si substrate, $L = 10$ nm and $V_{ds} = 0.3$ V. The threshold voltage was set to $V_t = 0.5$ V. Fitting parameter: β = 5.

Fig. 12 shows the validation of the C–V model against simulation data [33] for a double-gate 2D-FET with a single-layer InSe channel ($t_s = 0.8$ nm) and an oxide with an EOT of 0.5 nm. The threshold voltage was adjusted to $V_{t_{DG}} = 0.2$ V. The result demonstrates that our model precisely describes the

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capacitance-voltage relationship of this device.

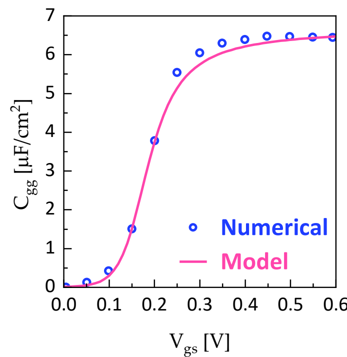

Fig. 12. Validation of the C–V characteristics with simulation data [33] considering a double-gate nanotransistor [18]. Parameters: InSe channel with $t_s = 0.8$ nm and $N_D = 3.5 \times 10^{11}$ cm^{-2}, SiO_2 gate oxide ($t_{ox} = 0.5$ nm). The threshold voltage was set to $V_{t_{DG}} = 0.2$ V.

IV. Conclusion

In the near future, 2D materials will not replace silicon in high-performance and high-density integration applications. Instead, 2D-FET applications are expected to focus on niches not well-served by current technology, such as flexible electronics. Another promising path is heterogeneous integration, where modules composed of silicon and 2D materials can perform complementary functions within the same chip.

In any case, as 2D-FETs gradually enter the nanoelectronics market, design techniques need to be refined to meet the demands of cutting-edge applications. Thus, the availability of reliable device models for IC design will be crucial.

To address this need, our paper presents an analytical model for the I–V and C–V characteristics of 2D-FETs considering the ballistic transport regime. Starting from the solution to the Poisson equation for the channel's electrostatic potential, we derived fully analytical and explicit charge-based expressions. These expressions are based on the intrinsic physical principles of the devices and the specific properties of 2D materials, including their band structure.

The developed models successfully reproduce the main characteristics of various devices, matching numerical and experimental results, for different channel materials, namely MoS_2 and InSe (and a preliminary model validation on phosphorene is available in a previous publication [16]). Therefore, this work contributes to the development and analysis of devices emerging as promising candidates for both the More than Moore and More Moore perspectives.

Appendix

This appendix outlines the material parameters used in the simulation of the ballistic nanotransistors based on three-layer MoS_2 [14] and InSe [13] at room temperature.

TABLE I
THREE-LAYER MOLYBDENUM DISULFIDE PARAMETERS

Parameter	Symbol	Value
Bandgap [36]	E_g	1.47 eV
Effective mass (K-valley) [14]	m_K^*	$0.48m_0$
Effective mass (Q-valley) [14]	m_Q^*	$0.57m_0$
Mobility (measured) [14]	μ_0	54 cm²V^{-1}s^{-1}
Thermal velocity	v_T	7.4×10^6 cm/s
Mean free path	ℓ	3.75 nm
Thickness [14]	t_s	1.95 nm
Relative permittivity [7]	ε_s	$4.8\varepsilon_0$

TABLE II
THREE-LAYER INDIUM SELENIDE PARAMETERS

Parameter	Symbol	Value
Bandgap [33]	E_g	0.87 eV
Effective mass [13]	m^*	$0.17m_0$
Mobility (*ab initio*) [37]	μ_0	697 cm²V^{-1}s^{-1}
Thermal velocity	v_T	1.3×10^7 cm/s
Mean free path	ℓ	27.76 nm
Thickness [13]	t_s	2.4 nm
Relative permittivity [13]	ε_s	$6.0\varepsilon_0$

The thermal velocity is calculated as

$$v_T = \sqrt{\frac{2k_BT}{\pi m^*}}. \tag{A1}$$

The mean free path is estimated as

$$\ell = \frac{2\phi_T\mu_0}{v_T}. \tag{A2}$$

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