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High Transconductance on Thiophene-Based Vertical Organic Electrochemical Transistors

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Organic electrochemical transistors (OECTs) are highly efficient ion-to-electron transducers, capable of achieving extremely large signal amplification, quantified by high transconductance (g_m) levels. Optimizing this parameters is crucial for developing highly sensitive electronic and bioelectronic devices. Here, record-high transconductances values exceeding 100 mS are obtained in vertical step-edge OECTs (vOECTs) utilizing two well-known p-type organic semiconductors: poly(3-hexylthiophene-2,5-diyl) (P3HT) and poly(3-[2-[2-(2-methoxyethoxy)ethoxy]ethyl]thiophene-2,5-diyl) (P3MEEET). Both materials exhibit high on-currents, small hysteresis and an on/off ratio on the order of 10^5. To benchmark the performance of vertical OECT architectures, it is proposed to normalize the maximum transconductance to the minimal footprint of the devices, which is equivalent to the cross-sectional area of the transistor channel defined by the product of channel width W and channel thickness d. By comparing $g_m/(Wd)$, these devices achieve one of the highest values reported to date. This work demonstrate record transconductances in well-known materials using step-edge vOECTs with a small cross-sectional area, establishing a robust platform for high-performance OECT-based applications.

1. Introduction

Organic Electrochemical Transistors (OECTs) have been proven to be a robust and reliable platform for a variety of applications, including neuromorphic devices,[1–3] logic circuits,[4–6] and biosensors.[7–9] Their versatility is largely due to their ability to provide efficient ion-to-electron transduction with high amplification at low operating voltages, as well as to their ease of manufacturing and reliable operation in aqueous conditions.

In OECTs, the channel between the source and drain electrodes consists of an Organic Mixed-Ionic-Electronic Conductor (OMIEC) film. The channel is interfaced by an electrolyte, into which a third electrode, refer to as the gate electrode, is immersed. The electrolyte is typically a liquid, with a Ag/AgCl pellet serving as a quasi-reference gate electrode. Upon gate voltage application (V_{GS}), ions migrate from the electrolyte into the OMIEC film, depleting or accumulating charges and thereby modulating the source–drain current (I_{DS}). Consequently, OECTs function as an efficient ion-to-electron transducers, undergoing redox reactions during doping or dedoping of the channel material.[10]

One of the most important parameters characterizing the operation of OECTs is the transconductance g_m, which quantifies the variation in I_{DS} in response to a given doping level established by the applied V_{GS}. Mathematically, it is defined as $g_m = \partial I_{DS}/\partial V_{GS}$, and, in the saturation regime it can be written as:

$$g_m = \frac{Wd}{L}\mu C^*(V_T - V_{GS}) \quad (1)$$

Here, W, d, and L are the channel width, thickness, and length, respectively, as defined in **Figure 1**, μ is the electronic mobility, C^* is the volumetric capacitance and V_T the threshold voltage. Thus, the transconductance depends simultaneously on the device geometry (Wd/L) and on the OMIEC's intrinsic material parameters (namely, μC^* and V_T). Higher g_m values indicate a high current amplification and increased device sensitivity. As a result, optimizing this parameter is a key focus in OECT research.[11–15]

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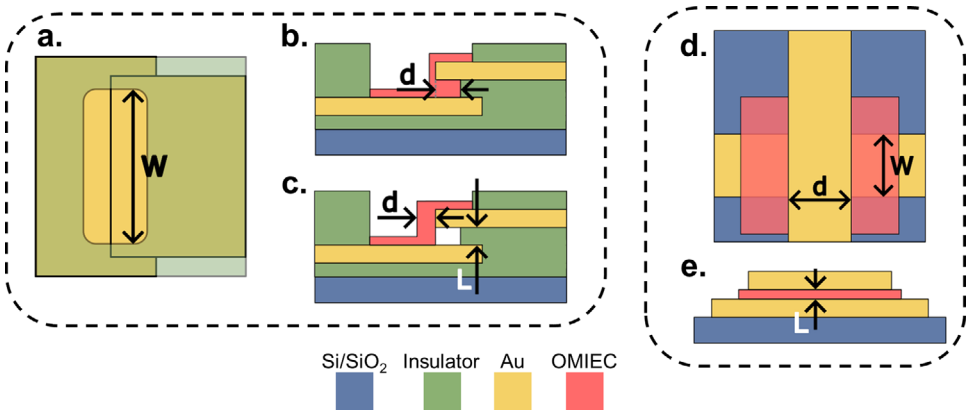

Figure 1. a) Top view sketch of vOECTs in the step-edge design. Lateral view of a step-edge device with the cavity b) filled and c) unfilled. See that the definition of *d* differs for each case. d) Top and e) lateral views sketches of a stacked vOECT.

The optimization of g_m can simultaneously be achieved through device or material engineering. As the transconductance g_m scales proportionally to Wd/L, miniaturization efforts have largely focused on reducing L by employing vertical structures, achieving transconductances >200 mS.[14–20] In vertical OECTs (vOECTs), in general, the source and drain electrodes are arranged vertically, with L defined as the vertical distance between these two electrodes. Several vOECT architectures exist, with the step-edge and stacked configurations being the most common ones to date,[21] as illustrated in Figure 1. In one of the step-edge construction, the source and drain electrodes are separated by a thin insulating layer, with the channel being formed vertically connecting the edge of the top electrode with the bottom one, without filling the cavity underneath the top electrode (see Figure 1c). Another possible step-edge construction is achieved by filling the cavity underneath the top electrode with the OMIEC material, e.g., by electropolymerization,[14,19,22] as illustrated in Figure 1b.

As for the stacked design, the source and drain electrodes are separated by the semiconductor itself, with the top electrode only partially covering the OMIEC to allow direct contact with the electrolyte (see Figure 1d,e). In terms of performance, both the step-edge and stacked configurations have demonstrated high transconductance, high on-current, and fast switching speeds.[14–18,23]

However, directly comparing different vertical architectures, as well as vertical and horizontal OECTs, is challenging due to their widely varying geometries, particularly the differing definitions of the geometrical dimensions width (W), thickness (d), and length (L). For instance, in the stacked architecture, the channel width W and thickness d are determined by the area beneath the top electrode.[16] Consequently, (W) and (d) are limited by the lithography resolution, typically in the range of a few micrometers (see Figure 1d). In contrast, for the step-edge design, d is significantly smaller, and care must be taken when defining it. As shown in Figure 1b,c, a small cavity typically exists between the top and bottom electrodes, resulting from the microfabrication process. During film deposition, such as by spin coating or electropolymerization, this cavity may or may not be filled. If the cavity is not filled, d is defined by the horizontal thickness of the OMIEC film in the step region, as shown in Figure 1c. On the other hand, if the cavity is filled, most of the conduction will occur across the cavity thickness,[14] and d can then be defined as the "depth" of the cavity, as illustrated in Figure 1b. In both cases, however, this thickness is on the order of a few nanometers only, making it an important feature for device miniaturization and enhanced performance metrics.

To compare the different OECT architectures, the transconductance must be normalized. In regular lateral OECTs the transconductance is typically normalized by the channel width (W), allowing for comparisons between devices with different OMIECs or channel widths. To compare vertical and horizontal architectures, however, it was proposed to normalize the transconductance to the footprint area of the devices.[24]

In lateral OECTs, the footprint area can be approximated by the channel area (i.e., WL), while in vOECTs the active area is defined as the product Wd.[16,18] For vertical OECTs, the area Wd also defines the cross-sectional area for current conduction. As a result, reducing the channel thickness d will lead to higher normalized transconductance values. It is important to note that, despite the area defined by Wd often represents only a small portion of the total OMIEC film area, most of the conduction indeed occurs near the step-edge region or within the overlap between top and bottom electrodes. Although a normalization method accounting for the total film area has been suggested,[21] a recent study showed that, especially for step-edge devices, once a specific d is reached, (typically until the cavity is filled). Further increases in film thickness do not significantly increase g_m further,[14] although reduces the switching speed of these devices.[14] These findings suggest that the Wd cross-sectional area is primarily responsible for current conduction in these devices, making it a valid metric for geometrical normalization.

Here, we investigate the performance of step-edge vOECTs for two thiophene-based p-type semiconductors: poly(3-hexylthiophene-2,5-diyl) (P3HT) and poly(3-[2-[2-(2-methoxyethoxy)ethoxy]ethyl]thiophene-2,5-diyl) (P3MEEET). We are able to demonstrate that the vOECT structure allows these materials to achieve high currents and high transconductance values. A maximum g_m beyond 100 mS was achieved for both materials for $W = 400$ µm and on-currents of ≈ –40 mA and ≈ –18 mA for P3HT and P3MEEET, respectively. Additionally, this study demonstrates that even without controlling the total area

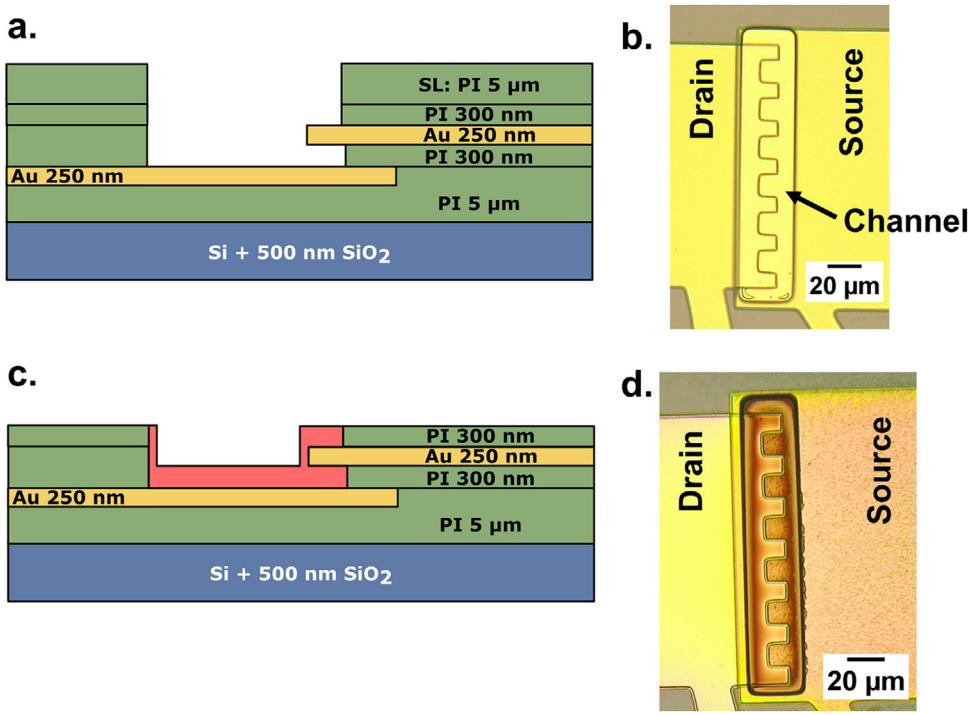

Figure 2. a) Side-view scheme and b) top view of the pristine vOECT (before OMIEC deposition). The top layer on (a) is the sacrificial layer (SL) and PI is the Polyimide insulation layer. c) Side-view scheme and d) top view of the vOECT after the OMIEC deposition and sacrificial layer removal.

of P3HT films, a linear trend of g_m against W was observed. This is associated with the filling of the cavity and indicates that the transconductance is not primarily affected by the total film area. Finally, we demonstrate that step-edge devices have smaller Wd product compared to the stacked architecture, leading to higher normalized performance. This work, therefore, paves the way for the development of high transconductance devices, showcasing a high normalized OECT transconductance to date.

2. Results and Discussion

The step-edge design, as shown in Figure 1a–c, is chosen here, mainly for its scalable manufacturing. Moreover, it also enables on-demand deposition of a wide range of semiconductors, offering a versatile platform for vOECT fabrication. Similar fabrication process as described in a previous report and as outlined in **Figure** 2a,c is used herein.[14] However, in contrast to the previous report, the edge of the top electrode is designed with a square sawtooth pattern (see Figure 2b,d and Figure S1, Supporting Information), in order to scale the channel width W without significantly altering the total film area. In this configuration, W is defined as the total length of all the edges of the top electrode. Two polymer mixed conductors, namely P3HT and P3MEEETs, are spin-coated onto the step edge. To delimit the open channel area, an additional sacrificial layer of polyimide (PI) is added to the layer stack. After peeling this layer, the semiconductor material remains only in the predefined area (see Figure 2d). For additional details on device design and fabrication, refer to the experimental section.

P3HT is a common material widely used in conventional (i.e. lateral) OECTs. As previously reported by Flagg and coworkers, annealing it at low temperatures or no annealing after deposition, results in a more amorphous P3HT film, which facilitates ionic transport into the channel and promotes swelling of the polymer film.[25–27] Therefore, after spin-coating the P3HT films, substrates were left overnight in a N_2 filled box to allow the solvent to evaporate. As shown in the supplementary information (Figure S2, Supporting Information), due to the small opening area of the channel, P3HT films with no annealing were almost completely removed during peeling-off of the sacrificial layer.

To overcome this, the films are annealed at 120 °C for 20 min. As depicted in Figure S2b, the annealing process promoted better adhesion of the P3HT films on Au electrodes, although, portions of the film are still removed along with the sacrificial polyimide (PI) layer. Nevertheless, five out of six devices per chip are still operational. As shown in **Figure** 3a–c, despite the non-uniformity of the film, devices exhibit good performance, with a maximum drain current of ≈–15 mA for $W = 400$ µm, maximum transconductance of up to 70 mS, an on/off ratio on the order of 10^5, threshold voltages around –0.33 V and turn-on time constant of (210 ± 80) ms (see Figures S3 and S4, Supporting Information, for more details).

To improve film adhesion and avoid any accidental peeling of the transistor channel, the annealing time is increased to 1 h, maintaining the same temperature. Unfortunately, even with this time increase, portions of the film are still peeled off during the removal of the sacrificial layer (see Figure S2, Supporting Information). Nonetheless, as shown in Figure 3d–f, all devices operate successfully with a substantial performance enhancement observed. The maximum drain current I_{DS} reaches ≈–40 mA, and the transfer curves exhibit reduced hysteresis (Figure 3e).

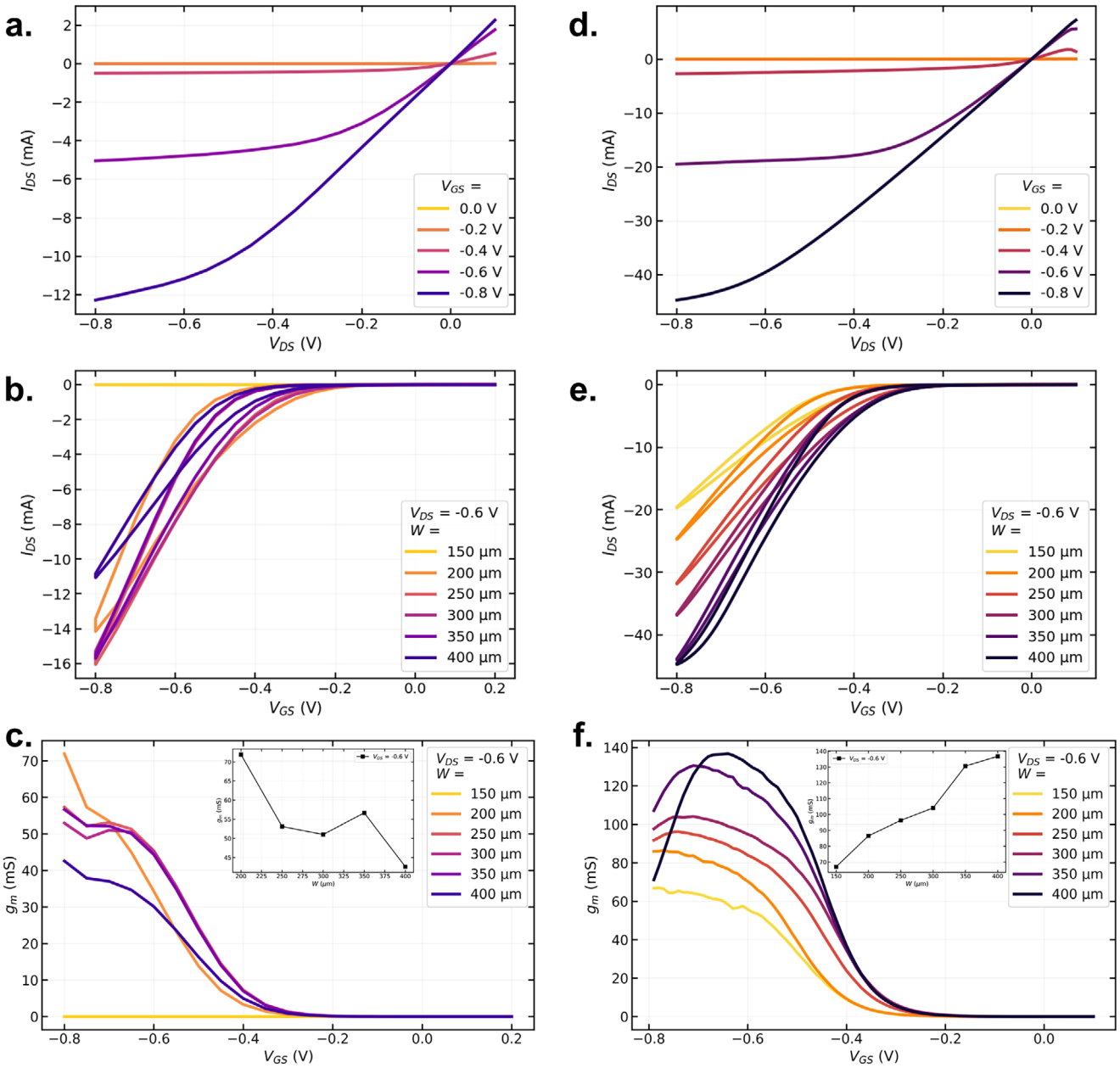

Figure 3. Electrical characteristics of P3HT vOECTs built under different annealing times. a) Output, b) Transfer, and c) transconductance for 20 min annealing. d) Output, e) Transfer, and f) transconductance for 60 min annealing. The inset in (c) and (f) depicts the maximum transconductance in respect to the channel width.

Furthermore, the maximum transconductance reaches 135 mS for $W = 400$ µm. The on/off ratio remains on the order of 10^5, while the threshold voltage varies with W, ranging from ≈–0.3 V to –0.36 V.

This performance improvement might be associated with a greater degree of crystallinity of the P3HT film, due to the extended annealing time. Crystalline structure in P3HT, are normally associated with improvements on the electronic mobility and, consequently, enhancement of the overall P3HT-based device performance. Moreover, the maximum transconductance follows a clear linear trend against W, as shown in the inset of Figure 3f. and S3d, and seems to be unaffected by the random total area of the P3HT film, resulting from bad adhesion.

To understand, why high-performance, highly reproducible OECTs are obtained despite poor adhesion and partial removal of the semiconductor layer, cross-sectional SEM images, as shown in **Figure** 4a and Figure S5 (Supporting Information) are taken. During the spin coating, the P3HT solution is able to fill the cavity and the annealing process hardens the film, leading to a round shape. The average depth of the cavity filled with the semiconductor, which corresponds to the channel thickness (d) (cf. Figure 1b), is ≈160 nm, being calculated by the average of

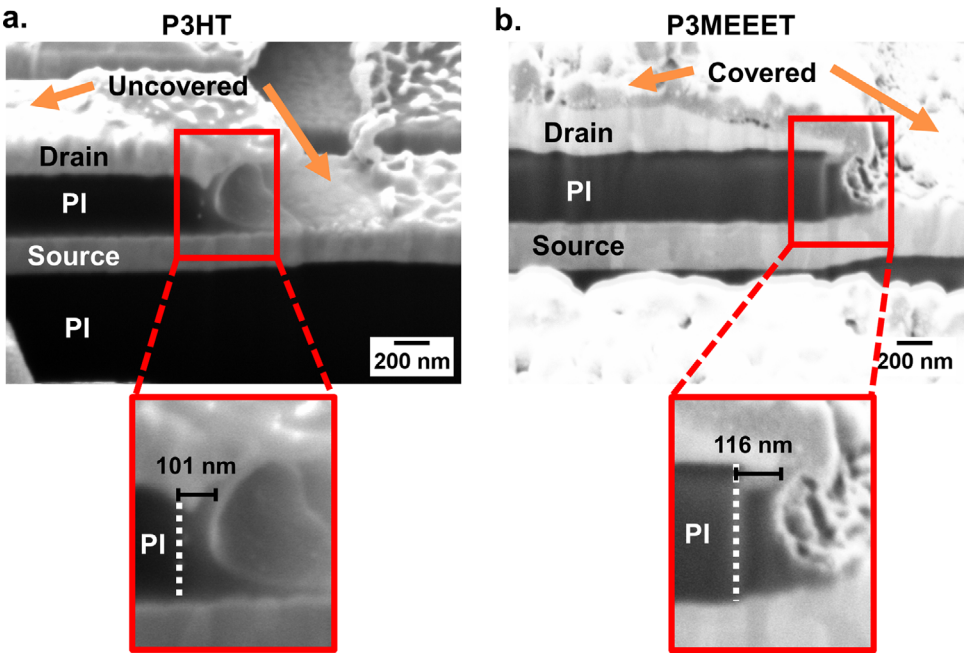

Figure 4. Scanning Electron Microscopy (SEM) images of a) P3HT and b) P3MEEET. The zoomed image shows the filled cavity for both materials.

different pictures at different locations. In addition to the filled cavity, peeling of the semiconductor film is clearly visible as well, leaving the source and drain electrodes uncovered (see Figure 4a). During the peeling of the sacrificial layer for P3HT, most of the film is removed, due to bad adhesion, but the cavity remains intact. This explains why, even with low film homogeneity, P3HT devices exhibit good and reproducible operation. Furthermore, this shows that g_m is mainly affected by the cross-sectional area defined by Wd in vOECTs, since no significant deviation from the linear relationship between the maximum transconductance and W is observed, despite the irreproducible total area of the film.

Additionally, vOECTs are fabricated using P3MEEET as the organic semiconductor, following the same 1 h annealing procedure as for P3HT. This ethyl-spaced thiophene-based OMIEC is a good candidate for high-transconductance devices, since it was reported that its modified side-chain allows for a swelling of roughly 80% of the polymer film in contact with electrolyte and under doping,[28] which leads to a higher volumetric capacitance C^*. As shown in Figure S6 (Supporting Information), structuring the channel film area by removing the sacrificial PI layer works very well, and the whole P3MEEET film remains on the substrate in the entire channel area after the peeling process. SEM images, as shown in Figure 4b and Figure S5 (Supporting Information) confirm the filling of the cavity with a round shape film, just as P3HT. The average film thickness in the cavity is 115 nm.

Despite the reported enhanced C^* as compared to P3HT, devices with P3MEEET exhibited lower drain current and transconductance (–18 mA and 111 mS, respectively for W = 400 µm) when compared to those measured on P3HT-based devices (see **Figure** 5a,b and **Table** 1). Despite the lower performance compared to P3HT, it still represents the highest transconductance reported, to date, in literature for this material. Notably, this g_m is achieved at relatively low V_{GS} and V_{DS}. At higher voltages, such as –0.8 V, devices exhibit significant degradation and instability, with increased hysteresis and reduced current in subsequent sweeping cycles (see Figure S7, Supporting Information). To mitigate this, V_{GS} is limited to –0.6 V and V_{DS} to –0.4 V. Consequently, the plateau of the transconductance curve in Figure 5b is not reached. Nevertheless, when operating within the reduced voltage range, the P3MEEET-based vOECTs demonstrate very good performance, with negligible hysteresis and improved switching speed (2.3 ms for the turn-on) when comparing with P3HT devices. (see Table 1 and Figures S7 and S8, Supporting Information).

For P3HT, even with low film homogeneity, devices demonstrate a maximum transconductance approaching the highest values reported for vOECTs. A summary of maximum transconductance values for vOECTs is provided in **Figure** 6a and summarized in Table 1. To date, vOECTs based on blends of gDPP derivatives with Cin-Cell cross-linkable polymers hold the highest transconductances among accumulation-mode transistors.[16,18] The highest reported g_m is 384 mS for a gDPP-g2T-based vOECT.[16] P3HT devices as reported here have a slightly lower absolute transconductance, marked by a black cross in Figure 6a.

Given the widely different device geometries and dimensions used to obtain the results plotted in Figure 6a, normalized metrics must be adopted for a fair comparison. As discussed above, performance parameters such as g_m and the on-current (I_{on}) can be normalized with respect to the footprint of the devices, which corresponds to the cross-sectional area of the active area of the vertical channel Wd, denoted by $g_{m,A}$ and $I_{on,A}$, respectively). However, the definitions of these two geometrical factors can be complex and depend strongly on the chosen design and the film deposition method. In the stacked architecture, W and d are limited by the lithography resolution of the metallic electrodes and are defined by the overlapping area under the top electrode. For step-edge devices, d is influenced by the film deposition process, specially whether the cavity between top and bottom

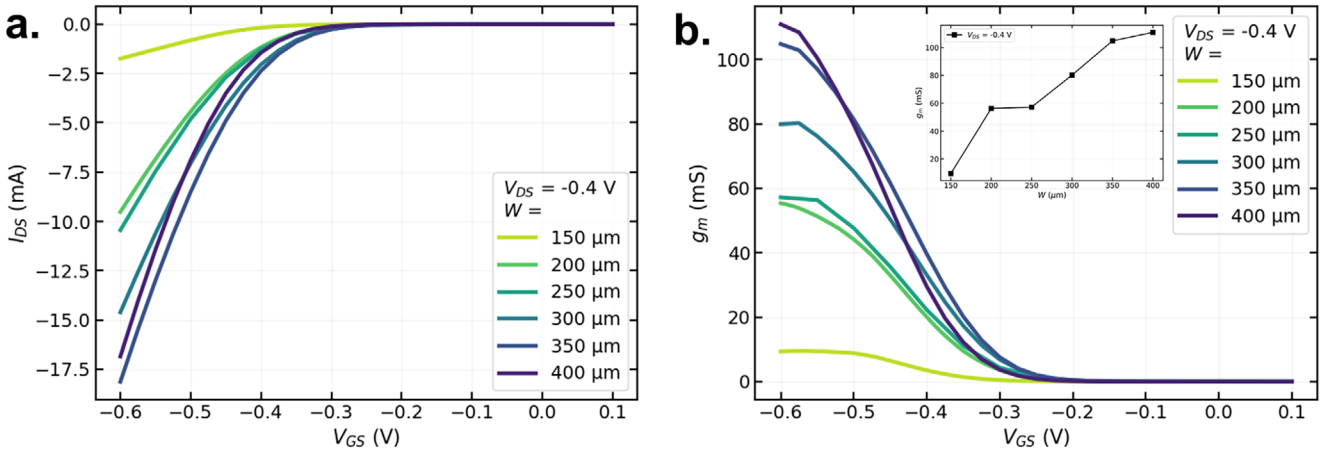

Figure 5. P3MEEET a) transfer and b) transconductance curves for different channel widths. The inset highlights the maximum transconductance in respect to *W*.

Table 1. Performance comparison for several p-type vOECTs.

OSC	Electrolyte	$W \times d$	$\lvert V_{GS}\rvert$	$\lvert V_{DS}\rvert$	g_m	$g_{m,A}$	$\lvert I_{on}\rvert$	$\lvert I_{on,A}\rvert$	On/off	Refs.
gDPP-g2T	PBS	70 × 70	−0.5	−0.5	384	78.3	82	16.7	10^6	[16]
		50 × 50	−0.5	−0.5	299	119.6	58	23.2	10^6	
		30 × 30	−0.5	−0.5	204	226.7	36	40	10^6	
PEDOT:PSS	Ringer's sol.	95 × 0.5		−0.5	39	821.1			10^5	[14]
		315 × 0.5		−0.5	71	450.8			10^5	
		660 × 0.5		−0.5	84	254.5			10^5	
		1130 × 0.5		−0.5	88	155.8			10^5	
		1730 × 0.5		−0.5	90	104.0			10^5	
	NaCl	50 × 50		−0.6	34	13.6	19	7.6	10^3	[17]
		100 × 100		−0.6	65	6.5	36	3.6	10^4	
		200 × 200		−0.6	97	2.4	37	0.9	10^4	
		500 × 500		−0.6	242	1.0	113	0.5	10^5	
		1000 × 1000		−0.6	275	0.3	150	0.2	10^5	
		70 × 0.7		−0.6	24	490	10	204		[23]
	KCl	50* × 0.6		−0.4	20	667				[29]
		100 × 0.4		−0.6	38	950	20	500	10^5	[30]
	[EMIM][TCM]	50 × 50		−0.5	64	25.6	19	7.6	10^2	[31]
PEDOT:PF_6	KCl	100 × 0.28		−0.6	68	2429				[30]
p(g2T-T)	PBS	35 × 30			130	123.8				[15]
		35 × 60			183	87.1				
		35 × 90			202	64.1				
		40 × 40		−0.1	69	43.1	18	11.3	10^5	[32]
gIDT-BBT		30 × 30			155	172.2	39	43.3	10^6	[33]
PIDTC16-BT	[EMIM][TFSI]	50 × 50		−0.1	73	29.2			10^7	[34]
PIDTPEG-BT		50 × 50		−0.1	13	5.2			10^7	
PDPP		100 × 0.08	−0.95	−0.3	12	1500			10^8	[22]
P3HT		100 × 0.1	−1.13	−0.3	1.5	150			10^4	
p(gDPP-V)	NaCl	30 × 30	−0.8	−0.4	268	297.8	45	50	10^7	[18]
P3HT[a,b]	LiTFSI	400 × 0.16	−0.8	−0.6	46	719	11	172	10^5	This work
P3HT[a,c]		400 × 0.16	−0.66	−0.6	135	2019	44	688	10^5	This work
P3MEEET[a]		400 × 0.12	−0.6	−0.4	111	2313	18	375	10^5	This work
		(µm × µm)	(V)	(V)	(mS)	(µS/µm^2)	(mA)	(µA/µm^2)		

*estimated from the circumference, [a]best performance device; [b]short annealing time; [c]long annealing time.

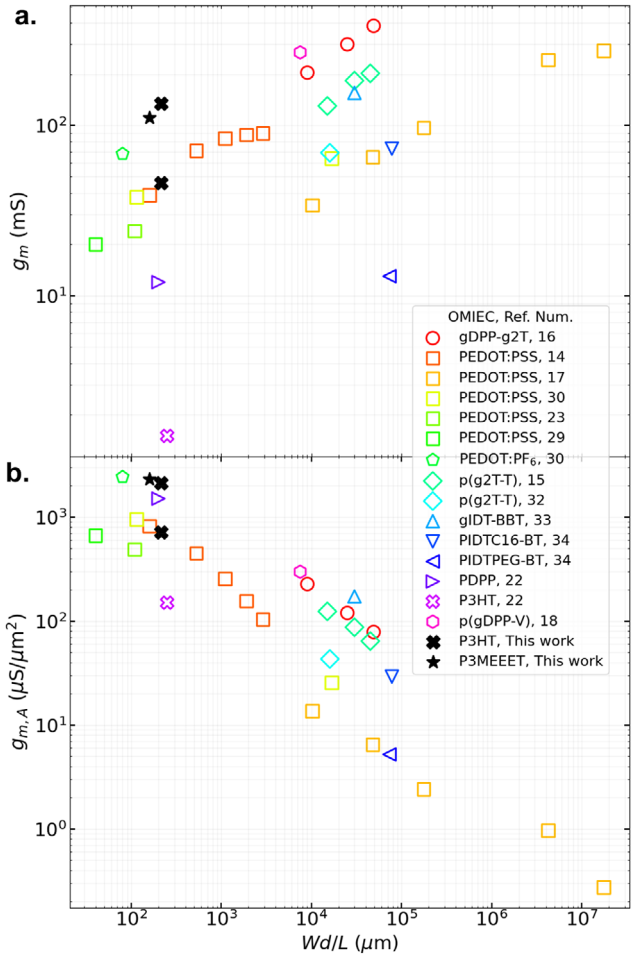

Figure 6. a) Literature transconductances of vOECTs. b) Transconductances normalized by the cross-sectional area *Wd*.

electrodes is filled. For electropolymerized films, the cavity is typically filled, and *d* can be tuned by changing the electropolymerization time.[14] For spin-coated films, however, the filling of the cavity can depend on various materials parameters, mostly on surface tension of the solution and capillary forces, with *d* being directly influenced by the spin-coating conditions. Thus, for step-edge devices, *d* can only be determined by microscopic imaging the cross-section of the cavity, as demonstrated here. Note, however, that even more complex architectures are possible, such as the stacked vOECT based on a nanoporous membrane.[35] In this case, the authors defined the cross-sectional as depending both on the pore area and the area of source and drain electrodes. Finally, it is evident that step-edge devices have a smaller cross-sectional area compared to the stacked devices, which is expected to result in higher normalized values.

As shown in Figure 4a,b and Figure S5 (Supporting Information), the cavities of the devices discussed here are completely filled, resulting in d = (160 ± 50)nm for P3HT and (120 ± 10)nm for P3MEEET. See that *d* is estimated from the average of at least five different cross-sectional SEM images. Normalizing the transconductance using these thicknesses results, a mean transconductance of (2.0 ± 0.5) mS μm^{-2} for P3HT (V_{DS} = –0.6 V) and (2.1 ± 0.6) mS μm^{-2} for P3MEEET (V_{DS} = –0.4 V) are obtained. The deviation is calculated from the standard deviation quantified from at least 11 devices. Compared to other literature results as plotted in Figure 6b and summarized in Table 1), our device performance surpasses or is on par with previously reported values for vertical OECTs. Notably, the highest normalized transconductance reported to date is from a PEDOT:PF_6-based vOECT,[30] which achieved 2429 μS μm^{-2}, on par with 2313 μS μm^{-2} obtained in our device. Additionally, the small standard deviation observed in our measurements further validates the use of cross-sectional area normalization as a reliable metric for comparing vOECT performance. This comes from the fact that in our devices the total film area varies with *W* (140 μm × 15–35 μm). A strong dependence of g_m with the total film area, instead of with *Wd*, would result in a high standard deviation when averaging these devices, but this is not the case for both of our vOECTs. Same observation holds true for the normalized absolute on-current, found to be (–0.6 ± 0.2) mA μm^{-2} for P3HT and (–0.4 ± 0.1) mA μm^{-2} for P3MEEET.

Finally, an inverse relation between $g_{m,A}$ and the geometrical factor is observed in Figure 6. From Equation (1), it follows that the normalized transconductance should indeed scale inversely with the geometrical factor *Wd*/*L*, indicating that this observed trend is primarily a geometric effect resulting from cross-sectional normalization. This behaviour primarily stems from the cross-sectional area (*Wd*), as devices with a larger *d* exhibit lower normalized transconductance and appear on the right side of the *Wd*/*L* x-axis. This indicates that devices with smaller cross-sectional areas and high g_m are more efficient at delivering the same absolute transconductance, requiring less area than those on the right side of the graph.

3. Conclusions

In this study, we demonstrate high transconductance step-edge vOECTs with reduced cross-sectional area, based on two well-known thiophene-based p-type semiconductors: P3HT and P3MEEET. The step-edge design for vOECTs has proven to be a versatile and robust platform for achieving high-transconductance devices with small cross-sectional area defined by *Wd*. All of the vOECTs reported exhibit high current, high transconductance, and low hysteresis, even with low film homogeneity, as for the case of P3HT. We show that, unlike planar OECTs, optimizing the annealing process for P3HT significantly enhances device performance. For a 400 μm width device, transconductance increased from 46 mS to 135 mS, while the on-current went from from –11 mA to –44 mA. P3MEEET devices reach a transconductance of 111 mS and on-current of –17 mA.

We also highlight the need to normalize the transconductance in order to facilitate a fair comparison between different vOECT architectures. We show that in our devices, a cavity underneath the source electrode is filled by the organic semiconductor, and that the effective channel width *d* is given by the depth of the cavity. By normalizing the maximum transcondutance by the cross-sectional area of the channel, i.e., the minimum footprint of the devices, *Wd*, both our devices achieve one of the highest transconductance among recent vOECTs. This is due to the small thickness of the vertical channel (*d*) in the step region for this architecture. Moreover, the small deviation of average value

supports the fact that despite different total film areas, the cross-section defined by *Wd* holds the major influence on the transduction of vOECTs. Finally, we demonstrate the robustness of step-edge vOECTs, establishing a basis for the development of high-transconductance and low footprint vOECTs with on-demand organic semiconductor deposition.

4. Experimental Section

Materials Preparation: The polymers poly(3-hexylthiophene) and poly(3-[2-[2-(2-methoxyethoxy)ethoxy]ethyl]thiophene-2,5-diyl), P3HT and P3MEEET, respectively, were purchased from Rieke Metals. Lithium bis(trifluoromethanesulfonyl)imide (LiTFSI) was purchased from Sigma–Aldrich Co. Chlorobenzene was purchased from TCI. All materials were used as received. Both polymers were dissolved in chlorobenzene at a concentration of 20 mg mL^{-1} and stirred at 60 °C overnight. All handling was made in open-air conditions.

vOECT Fabrication: The vOECTs wafers were fabricated in the IMSAS ISO-6 cleanroom, following similar microfabrication steps as previously reported in ref. [14]. However, after the deposition of a thin insulating polyimide (PI) layer onto the top electrode, an additional thick PI layer (around 5 µm) was spin-coated on top and cured with a vacuum hotplate. This additional layer was used as a sacrificial layer later on. Both layers were structured by photolithography (AZ 10XT, MicroChemicals GmbH) and oxygen RIE plasma (STS ICP). The distance between source and drain electrodes, the channel length, was around 300 nm. The width of the devices ranged from 150 to 400 µm, in steps of 50 µm. For devices with $W \geqslant 200$ µm, the step-edge was designed as a square sawtooth where the width was given by the perimeter of the top electrode edge. This allowed to scale device width while avoiding significant changes of the channel opening area. After dicing the wafers, the organic films were deposited. A small volume of the dissolved semiconductor was spin coated at 2040 RPM for 60 s. The device was then heated to 120 °C for 1 h, unless mentioned otherwise. Finally, the sacrificial layer was peeled, delimiting the channel area (140 × 15–35 µm). The electrolyte was prepared at a concentration of 100 mM in DI-water. The gate electrode was an external Ag/AgCl pellet.

vOECT Electrical Characterization: Steady-state measurements of vOECTs (transfer and output curves) were recorded using SweepMe software and a Keithley 2612b. For P3HT, transfer curves were measured ranging V_{GS} from 0.1 V to –0.8 V and V_{DS} from 0.0 V to –0.6 V, with steps of 0.2 V. Output curves were recorded for V_{DS} ranging from 0.1 V to –0.8 V and V_{GS} from 0.0 V to –0.8 V, with steps of 0.2 V. For P3MEEET the gate and drain voltages were limited up to –0.6 V and –0.4 V, respectively, for both curves. Each curve for all devices was measured at least twice, where always the last measurement was considered for analysis.

Scanning Electron Microscopy: Scanning electron microscopy (SEM) cross-sectional images were taken using a Auriga Zeiss Cross FIB-SEM. A thin gold layer was sputtered on top of the samples. The cross-sectional cuts were made with a FIB at 30 kV with 20 pA current (Canion FIB from Orsay Physics), resolution: 7 nm. The stage was positioned at 54° and tilted at 36° at 5.0 kV and 1.3 kV, for P3HT and P3MEEET respectively. The samples were mounted at 45° and tilted at 20°.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

high transconductance, P3HT, P3MEEET, vertical organic electrochemical transistor

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