PAPER

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Successive approximation register ADC single event effects protection and evaluation

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Abstract: This work analyses seven different alternatives to implement an ADC based on the successive approximation register (SAR) architecture. The influence of the encoding is taken into account while evaluating the importance of its reset approach. Different protection strategies against single event upsets are addressed, including the comparison of per block and per cell triplication. All versions of the SAR were designed and prototyped in the TSMC 130 nm technology. The die was packaged in an open window QFN64 and irradiated at the LAFN Pelletron particle accelerator, which revealed the impact of the encoding and reset choices in the block cross-section showing improvements of more than a thousand times.

Keywords: Data acquisition circuits; CMOS readout of gaseous detectors; Digital electronic circuits; VLSI circuits

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1 Introduction

Analog-to-digital converters (ADCs) are critical parts of numerous acquisition systems in high energy physics (HEP) experiments. There are several possible architectures to design an ADC and a popular one is the successive approximation register (SAR), due to its low power and area [1].

These blocks are usually in an early position in the system data-path and errors injected there are likely to influence or corrupt experimental data [2].

Several acquisition systems in HEP experiments are targeted to operate in environments with occurrence of SEEs (single event effects) as SEUs (single-event upsets) and SETs (single-event transients) that can change the data or the converter internal state [3].

In order to mitigate some of these errors, several possible implementations of SARs have been designed, fabricated, and then tested with an irradiation campaign to obtain the per block cross-section of each protection alternative as a metric to choose the most adequate option.

2 ADC architecture

The SAR ADC is a mixed-signal block and may be implemented using a comparator, a DAC and a control module. The last one is a digital block (here referred to as sar_reg) which is responsible for running the successive approximation algorithm, triggering the sampling, controlling the DAC switches and reading the comparator responses. Figure 1 illustrates the SAR ADC block diagram [1].

The *sar_reg* will be the focus here as it contains most of the ADC logic circuitry. The design in question is based on a state machine controlled by the comparator providing as output the digitized data word and two complementary vectors that control the capacitive DAC inputs.

The design was initially based on a typical implementation [1, 4] hereafter cited as reference ADC. The reference ADC is characterised by a state machine with an asynchronous reset, being restarted at each new conversion by the edges of the sample clock input, which is not required to be synchronous with the conversion clock.

This configuration can lead to two major adverse effects. First, a SET in the sampling lines feeding these resets can reset the full block as it has no filtering or synchronization to the main SAR

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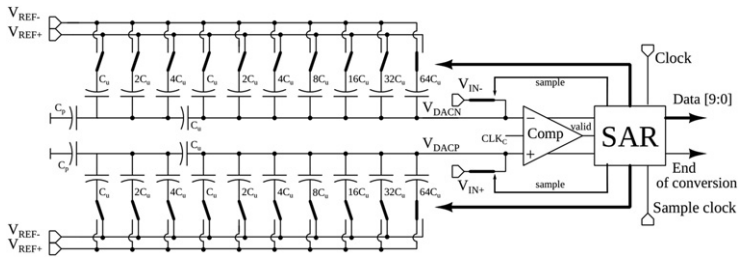

Figure 1. SAR ADC block diagram [1].

clock. This may cause meta-stability, wrong conversions and conversions with different sampling periods than the desired, where the last can be considered as distortion. Second, the SET can also act just partially in the block (due to the asynchronous nature of the reset), corrupting the conversion and producing wrong digitized data, which is bad for the experiment and is a kind of data loss.

Both cited cases can also have additional drawbacks on the receiver side (on the digital signal processor block), as these extra conversions in unexpected times could cause timing violations and meta-stability in the first register layer or further.

The ADC also has a synchronous section based on standard flip flops. This part is responsible to keep the current state and also to store the final digitized value. The final output was registered to relax the timing constraints of the inputs in the next block.

The reference ADC digital section is in fact not protected, being vulnerable to single event upsets which can lead at least to two main problems. The first is the corruption of the output data after a successful conversion. It can happen while the achieved result stored in the last register is waiting to be acquired by the digital signal processor. This corruption usually appears as bit-flips in the ADC value, destroying the sample data.

The second vulnerability appears when the SEU happens in the registers of the SAR state machine. This can lead to undesirable behavior and bad control of the analog blocks activated by this state machine, such as the sampling and capacitive DAC switches. After an event like this, at the end of the cycle, an unexpected result may be achieved and experiment data will be lost. This circuit has an additional aggravating factor, it runs much faster than the output register, being more active by a factor of ten in relation to the sampling clock, having a higher probability of capturing shorter SETs.

2.1 Designed prototypes

Due to the cited weaknesses, a set of different designs were fabricated and tested. The analysis was divided into two main topics, one regarding the coding of the state machine and the other concerning the redundancy architecture used for protection. Additionally, the role of the asynchronous sampling and reset was evaluated, where for the new alternatives synchronous resets were used.

Table 1 provides a list of the designed blocks according to the architectures and redundancy options selected, where all of them were manufactured in the 130 nm process. The initial lines of the table present comparatively the reference ADC (as ADC0 and ADC1, both functionally equivalent) and a version with parity in the outputs to check for SET in the output cells of the pad

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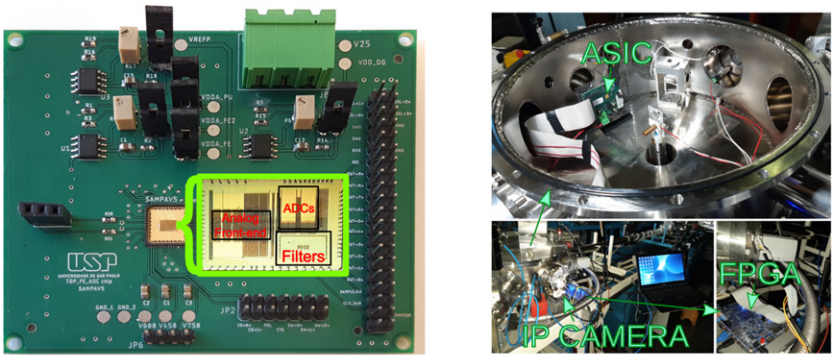
ring. The following blocks were incrementally identified from sar_reg03 to sar_reg08 focusing on the alternatives with synchronous reset, where for the binary and one-hot coding, 3 different blocks were implemented. This with the purpose of comparatively explore the protection alternatives with triplication by register and by full block. The implementations labeled as TMR (triple modular redundancy) have each of its individual registers triplicated followed by a majority voter cell, on the other hand, the BTMR (Block TMR) cases are composed of three full copies of the control block with voting on the top level. The encoding alternatives were first based on the use of one hot encoding [5] (maintaining the reference ADC encoding), where each SAR step was direct encoded as one active bit (as the one hot name suggests). The latter alternatives were made with binary values for each SAR conversion step. Table 1 also provides in its last column the target comparison motivating each specific implementation alternative.

Table 1. List of the ADC implementations and their main characteristics.

Block ID	Name	Encoding	Protection	Reset	Target
ADC0	Reference ADC	One hot	None	Asynchronous	Reference
ADC1	Reference (copy)	One hot	None	Asynchronous	Cross-check
ADC0P	Reference + parity	One hot	None	Asynchronous	SET check
sar_reg_03	sar_reg5_notmr_hot	One hot	None	Synchronous	Sync. X async.
sar_reg_04	sar_reg5_tmr_hot	One hot	TMR	Synchronous	Redundancy
sar_reg_05	sar_reg5_mod_hot	One hot	BTMR	Synchronous	Redundancy
sar_reg_06	sar_reg5_notmr_bin	Binary	None	Synchronous	Encoding
sar_reg_07	sar_reg5_tmr_bin	Binary	TMR	Synchronous	Encoding
sar_reg_08	sar_reg5_mod_bin	Binary	BTMR	Synchronous	Encoding

An irradiation was planned aiming the evaluation of the real behavior of these blocks when exposed to interactions with a controlled particle flow. Figure 2(a) shows the test board used in the irradiation tests of this ASIC (application specific integrated circuit). No digital components were included in this board except for the test chip itself.



(a) (b)

Figure 2. (a) Test board with the opened package. (b) Pelletron accelerator irradiation setup.

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The chip was housed in an open window QFN 64 package to permit the irradiation testing of the die with more exposure and precision. Figure 2(a) also provides a micro-photography of the die at the side of the packaged version. The total test chip area was 3346 µm × 2120 µm = 7.1 mm^2.

The test setup was based on the board shown in figure 2(a) connected to a SocKit Cyclone V System-on-Chip FPGA board. A data acquisition software was developed in C and run over a Linux operating system in a dual-core ARM HPS. The software automatically performs functional tests over the blocks in the ASIC, monitoring and accounting for any detected anomaly.

Figure 2(b) illustrates the actual irradiation setup used during the tests in the Pelletron particle accelerator at LAFN (Laboratório Aberto de Física Nuclear, Physics Institute of São Paulo University). The bottom pictures show a general view of the environment and a zoom over the FPGA. This board was placed outside of the irradiation chamber, minimizing the chances of the data acquisition system failing due to single events.

3 Results

The irradiation was performed using three different beam types, starting with 5 MeV alpha particles and going to 44 MeV$^{16}O^{7+}$ and finally 57 MeV$^{28}Si^{8+}$ with LET (linear energy transfer) in silicon of 0.6, 6.4 and 13.6 MeV/(mg/cm^2) respectively. The test with the alpha particles was discarded due to its extremely low event count and statistical content.

Focusing on metrics for comparison with the designed variations of the block, the reference SAR ADC was irradiated and the test data was processed targeting to obtain the cross-sections. The resulting values for^{16}O and^{28}Si were respectively $(1.61 \pm 0.03) \times 10^{-5}$ cm^2 and $(1.93 \pm 0.04) \times 10^{-3}$ cm^2.

These cross-sections numbers indicate that the block was very vulnerable and checking the data manually it had several losses and malfunctions, showing its fragility. All the failures were followed by good conversions after one or more sampling cycles, showing that the block was only temporarily disturbed and not hardly damaged by the previous event, re-enforcing that a SEU or SET was the main source of error, not latch-up or worse.

The failure levels found are not negligible and in order to understand and improve the block, the alternative versions of this circuit were irradiated. Table 2 shows the cross-section data for the distinct implementations focusing in the^{16}O, where bigger fluences could be achieved.

To start the analysis, it is possible to see that there is a huge difference in the global cross-section values between the reference ADC and the other implementations, and this happened for all particles and fluxes.

Searching for a closer comparison, the most similar implementation to the reference ADC can be found in table 1 as *sar_reg_03*. This alternative is basically designed with the same architecture and encoding scheme, but implemented with the synchronous reset/sampling.

Comparing the reference version with the *sar_reg_03* in table 2, a considerably bigger cross-section and error count is found in the reference case, where the major difference is just the reset.

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Table 2. Comparison between the different SAR implementations results for the ^{16}O beam.

Block ID	Architecture description	Flux [10^3/(cm^2 s)]	Fluence [10^6/cm^2]	Event count	Cross-section [cm^2]
Reference	Asynchronous	819.0	368.2	5932	$(1.61 \pm 0.03) \times 10^{-5}$
sar_reg_03	One hot	918.5	291.9	140	$(4.79 \pm 0.41) \times 10^{-7}$
sar_reg_04	One hot TMR	918.5	291.9	0	$<1.03 \times 10^{-8}$
sar_reg_05	One hot BTMR	918.5	291.9	0	$<1.03 \times 10^{-8}$
sar_reg_06	Binary	918.5	291.9	102	$(3.49 \pm 0.35) \times 10^{-7}$
sar_reg_07	Binary TMR	918.5	291.9	0	$<1.03 \times 10^{-8}$
sar_reg_08	Binary BTMR	918.5	291.9	0	$<1.03 \times 10^{-8}$

With these facts, a relevant hypothesis can be stated, this design should have the amount of asynchronous nets minimized, as they have shown to increase the sensitivity of the block to the interactions.

Further observations can also be made in the results of table 2, where differences in the cross-sections between *sar_reg_03* and *sar_reg_06* show that a slightly worse performance happened when using the one-hot coding in the state machines, probably due to its bigger register area.

Finally, it is possible to state that there are positive results concerning the evaluation of both inserted protections alternatives since, for all cases with redundancy, no errors were registered. And this scenario was the same for all the protected blocks with all beams, illustrating a great improvement in relation to the older versions in this aspect.

4 Conclusions

An ASIC containing several implementations of a 10-bit SAR was designed, produced and tested. The device was irradiated in a campaign on the Pelletron particle accelerator at LAFN using alpha particles,^{16} O and^{28}Si. The reset strategy and conversion start signals were found to be very important to the block sensitivity to single events and the amount of asynchronous logic should be minimized. The encoding used in the SAR state machine was evaluated and it also impacts the cross-section of the device, being the ADC standard one-hot approach more sensitive than the simple binary encoding, which represents a difference of about 25%. The use of triplication was essential to achieve lower cross-sections and no errors were measured in the implementations based on the per register and per block strategies within the tested ranges. With protection, the SAR achieved cross-sections improvements of more than 1500 times.

Acknowledgments

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