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Evaluation of an interleaved boost converter powered by fuel cells and connected to the grid via voltage source inverter

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Abstract: The connection of distributed generation systems powered by fuel cells (FCs) to the grid requires power electronics devices with high voltage gain, high capability of power processing and high levels of current absorbed from the direct current (dc) source. In this context, the authors propose the use of an interleaved boost with voltage multiplier (IBVM) converter connected to a FC and a voltage source inverter (VSI) to form a micro grid. To manage the power delivered by the FC in grid-connected operation, they propose two different control structures, mode 1 (FC cascade control) and mode 2 (controlling FC operating point). In mode 1, the dc-link voltage is adjusted by the dc/dc converter, while the injected current is controlled by the VSI. On the other hand, in mode 2, the VSI is responsible to keep the dc-link stable, while the dc/dc converter controls the current injected into the grid by means of the FC current reference. Since the VSI control structure has been exhaustively investigated in the literature, in this study, they evaluate the impact of the proposed control structures in the dc-side and also the IBVM efficiency. Finally, they conclude the study outlining the main points discussed.

1 Introduction

The grid connection of low voltage and high-current renewable energy sources requires the use of power converters to adjust the dc-link voltage and/or the current absorbed from the dc-source. Additionally, the fuel cells (FCs) are the renewable energy sources that operate with the aforementioned characteristics, i.e. in most applications they work at low and medium power and use dc/dc step-up converters to match the FC terminal voltage to the grid voltage. In this context, the converter topology and the control structure play an important role in terms of stability, capacity to block oscillations coming from the ac-side, and power processing [1].

Several topologies of non-isolated dc/dc converters have been investigated in this type of application. As FCs are low-voltage and high-current sources, they require converters with high voltage gain in order to connect them to the grid, thereby in [2, 3] the authors propose different techniques to achieve high-voltage gains with non-isolated dc/dc converters. Under these conditions, the authors of [2, 4] propose the use of dc/dc converters in series connection to achieve high-voltage gains; however, this solution decreases the total efficiency as the number of series connection is increased.

As shown in [5], the use of coupled inductors is another alternative to obtain high-voltage gains. However, the non-ideal coupling between the primary and the secondary windings results in leakage inductances, which causes high-voltage stress across the semiconductors and ringing losses. In [6], the authors apply an active clamping circuit to limit the voltage stress, and therefore avoiding to damage the semiconductors, and also recycling the energy from the leakage inductance, which improves the converter efficiency. Unfortunately, active clamping circuits require extra components as semiconductors, capacitors, and inductors.

In [7], the authors employ a high step-up converter for FC energy source applications. Through the three-winding coupled inductor and voltage doubler circuit, they achieve high step-up voltage gain without high values of duty-cycle. The passive lossless clamped technology does not only recycle the leakage energy to improve efficiency but also mitigate high-voltage spikes with the purpose to limit the voltage stress.

Among the most important topologies of dc/dc converters, the interleaving offers many advantages as the current sharing among the arms [7–9], the use of cheaper semiconductors, smaller inductors, reduction in the current ripple level, enhancement of the converter efficiency, and a better thermal distribution across the heat sink.

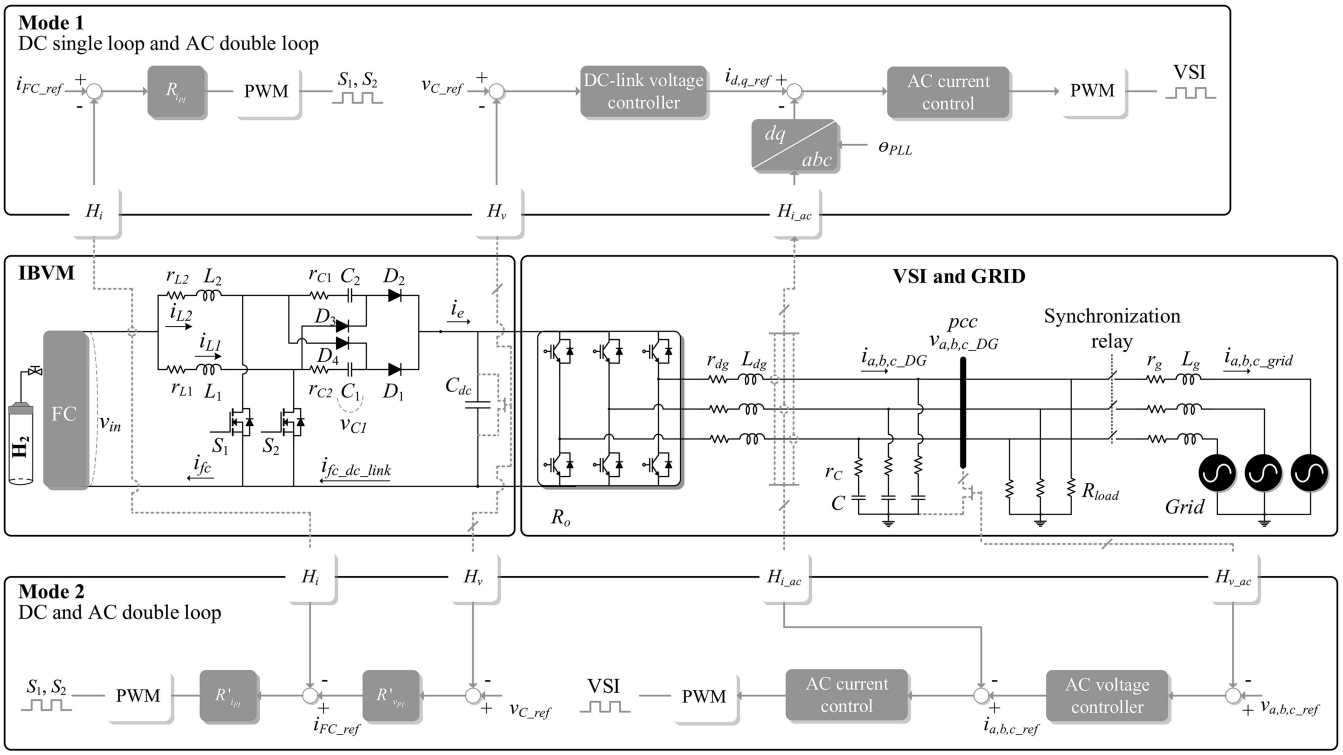
Additionally, the use of voltage multiplier cells in cascade with the interleaved boost converter improves the ability to achieve higher-voltage gains when compared with the classical boost converter [10, 11]. In this context, in [12], the authors provide a simplified model of a boost converter in cascade with voltage multiplier cells.

A novel high step-up converter, which is suitable for a renewable energy system that requires high-voltage gains is proposed in [13]. The converter is composed of dual switches, three winding coupled inductors, and two voltage multiplier cells to achieve the high-voltage gain. The dual switches reduce the voltage and current stress of the semiconductors, while the energy stored in the leakage inductor is recycled with the use of clamped capacitors.

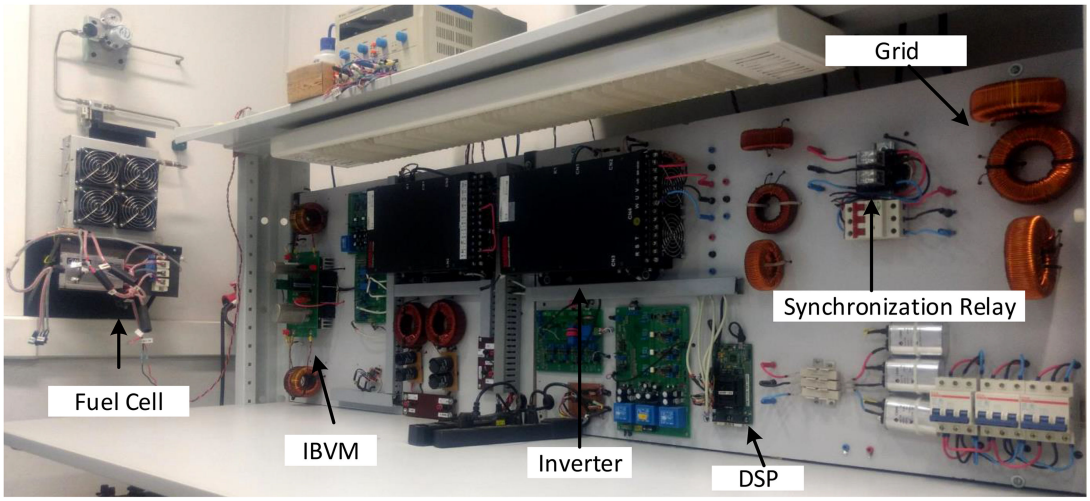
The interleaved boost with voltage multiplier (IBVM) presented in [14, 15] and modelled in [16] gathers advantages as the interleaving technique and the use of voltage multiplier cells. In addition, as mentioned in [17–22], the passive losses and the load variation affect the efficiency and the direct current (dc)/dc converter voltage gain.

Regarding the control method, in [23], the classical linear control relies on the dc/dc state space model, nonetheless, in [24], the sliding-mode control is used to reduce this dependence. Unfortunately, this type of solution produces variable switching frequency and oscillatory modes even when the switching frequency is constant.

Considering a precise process of design which ensures a wide range of stability, the linear proportional—integral (PI) controllers are the most useful solution because they present a low computational cost, easy implementation, and excellent performance, as well [25, 26].



a



b

Fig. 1 *Circuit diagram and experimental setup*
(a) Circuit and control diagram, ***(b)*** Experimental setup

Also, as mentioned in [27], the FC performance deteriorates as the current ripple increases through its terminals. The experiments presented in [27] confirm that the FC available power and voltage distortion increase proportionally with the current ripple.

Based on the aforementioned arguments, this study presents an IBVM converter powered by a dc source and connected to the grid by means of a voltage source inverter (VSI), as shown in Fig. 1.

In this approach, we present the model of the IBVM converter to design the controllers. To validate the model, we also included the IBVM efficiency analysis.

To assess the system performance in grid-connected mode, we propose two different control structures: control mode 1 and mode 2. In mode 1, the IBVM is controlled using a cascade structure with the FC current in the inner loop and the dc-link voltage in the outer loop, while the VSI controls the power transferred to the grid. On the other hand, in mode 2, the IBVM controls the FC operating point by using a single-loop current control, while the VSI regulates the dc-link voltage.

This paper is organised as follows: Section 2 shows the mathematical model of the IBVM converter in steady-state and small signals, Section 3 presents the analysis of the two control modes, in Section 4 the experimental results are evaluated, Section 5 shows the efficiency analysis, and finally in Section 6 we outline the main points presented.

2 Interleaved boost converter with voltage multiplier

The IBVM shown in Fig. 1 is a boost converter with current sharing between the phases and voltage doubler cell according to [16, 28]. To design the controller and evaluate the efficiency, we include the inductor L_1, L_2 losses (r_{L1}, r_{L2}); the capacitor C_1, C_2 losses (r_{C1}, r_{C2}) and the transistor S_1, S_2 losses (r_{S1}, r_{S2}). To reduce the level of ripple injected into the grid, we included a $L_{dg}C_fL_g$ filter, where r_{dg} and r_g are the inductors losses and r_f is a resistor connected in series with the capacitor C_f. In addition, at the point of common coupling a relay (S_g) is used to connect the distributed

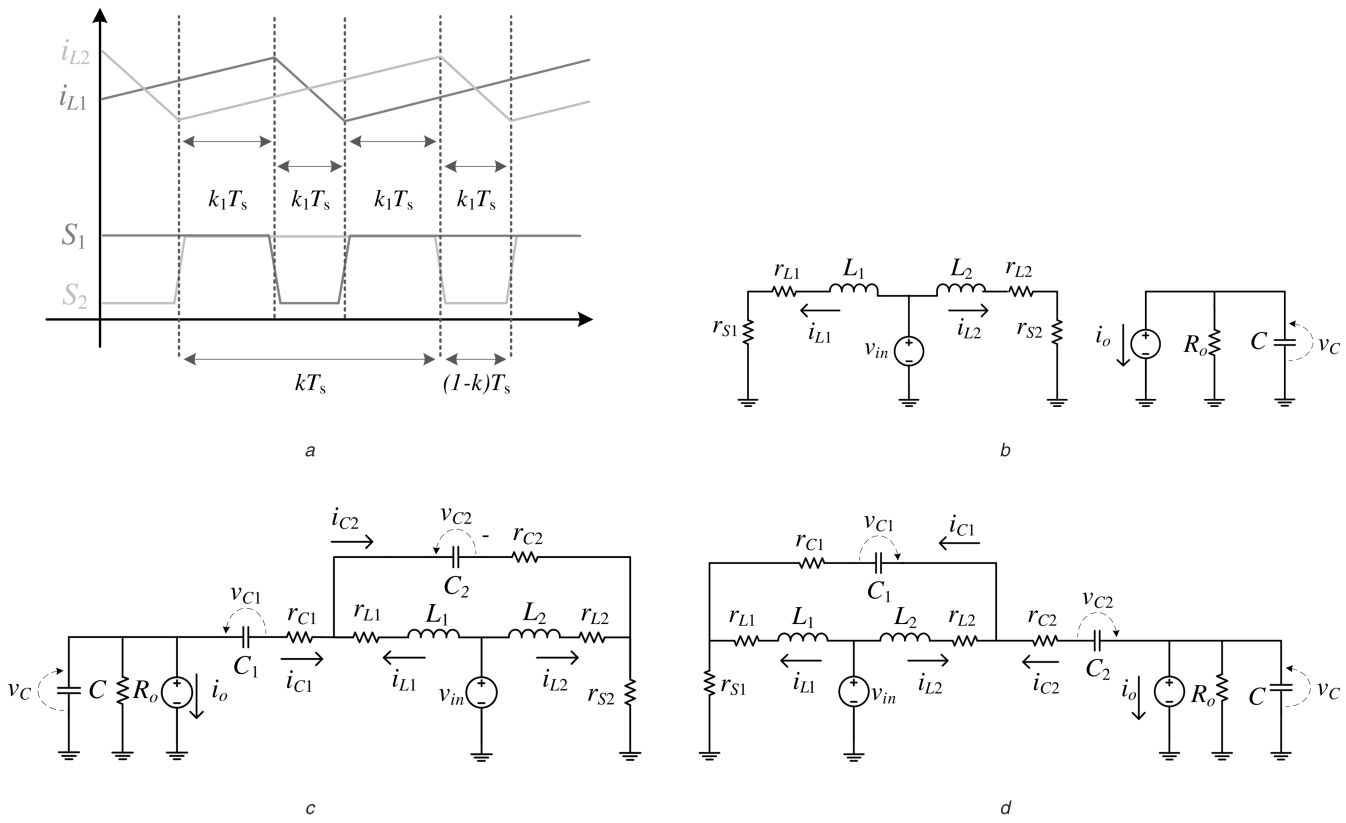


Fig. 2 *IBVM intervals of switching and equivalent circuits*
(a) Intervals of switching, ***(b)*** Equivalent circuit of the intervals k_1T_S and k_3T_S, ***(c)*** Equivalent circuit of the interval k_2T_S, ***(d)*** Equivalent circuit of the interval k_4T_S

generation (DG) to grid when the ac voltage is properly synchronised.

In terms of mathematical model, the state vector $\boldsymbol{x} = [i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}\ v_C]^T$ is compound by the current of the inductors (i_{L1} and i_{L2}), by the voltage of the doubler cells (v_{C1} and v_{C2}), and by the dc-link voltage (v_C) of the capacitor C. Using the same idea, the input vector $\boldsymbol{u} = [v_{in}\ \ i_0]^T$ is compound by the voltage at the FC terminals (v_{in}) and the equivalent current delivered to the VSI (i_0), while the model of the ac side (VSI + ac loads + grid) is the equivalent resistance R_O. The output vector $\boldsymbol{y} = [i_{L1} + i_{L2}\ \ v_C]^T$ is a function of the current ($i_{L1} + i_{L2}$) through the inductors placed on the FC terminals ($i_{fc} = i_{L1} + i_{L2}$) and the dc-link voltage (v_C).

Additionally, in Fig. 1, i_{fc_ref} is the IBVM current reference, v_{C_ref} is the dc-link voltage reference, i_{a,b,c_dg_ref} are the current reference at the DG terminals and i_{d,q_dg_ref} are the current reference at the DG terminals using the Park transformation. In the same picture, we observe current (i_{a,b,c_dg}) and voltage (v_{a,b,c_dg}) produced by the DG system, and the grid voltage (v_{abc_g}) used to synchronise the DG system to the grid.

With the purpose to minimise the FC current ripple, the IBVM converter duty-cycle must be >0.5. Therefore, the IBVM converter operates in the continuous-condition mode with four different intervals of switching, as shown in Fig. 2*a*.

During the first interval of switching (k_1T_S), the transistors are closed (S_1 and S_2) and the diodes (D_1, D_2, D_3, and D_4) are reversely biased. In this switching period, the mathematical model (1) of the IBVM converter is obtained from the circuit analysis in Fig. 2*b*. Consequently, the matrices $\boldsymbol{A}_1$ and $\boldsymbol{B}_1$ are obtained considering the state and input vectors, respectively.

In the second switching interval (k_2T_S), the transistor S_2 remains conducting while D_2 and D_4 are turned-on. The mathematical model (2) results by applying the Kirchhoff's law in Fig. 2*c*, from which the matrices $\boldsymbol{A}_2$ and $\boldsymbol{B}_2 = \boldsymbol{B}_1$ derive. In terms of dynamic behaviour, the third interval (k_3T_S) is equal to the first, in other words, the transistors (S_1 and S_2) are also closed while all diodes are blocked. In this case, the state space matrices are $\boldsymbol{A}_3 = \boldsymbol{A}_1$ and $\boldsymbol{B}_3 = \boldsymbol{B}_1$

$$\left.\begin{aligned}
\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} &= -\left(\frac{r_{L1} + r_{S1}}{L_1}\right)i_{L1} + \frac{v_{in}}{L_1}\\
\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} &= -\left(\frac{r_{L2} + r_{S2}}{L_2}\right)i_{L2} + \frac{v_{in}}{L_2}\\
\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} &= 0\\
\frac{\mathrm{d}v_{C2}}{\mathrm{d}t} &= 0\\
\frac{\mathrm{d}v_C}{\mathrm{d}t} &= -\frac{v_C}{CR_o} - \frac{i_o}{C}
\end{aligned}\right\} k_1 = k_3, \tag{1}$$

(see (2)) .

(see (3)) . The last interval (k_4T_S) illustrated by the equivalent circuit in Fig. 2*d* is similar to the second interval, in this case, S_1 is closed and the diodes D_1 and D_3 are conducting. The matrices calculated for this subinterval (3) are analogous to the second interval, and the equations can be easily obtained by swapping the indices 1 and 2, which results in the matrices $\boldsymbol{A}_4$ and $\boldsymbol{B}_4 = \boldsymbol{B}_1$.

To obtain the IBVM converter average model, we multiply the state, input, output and direct transition matrices of an ith subinterval ($\boldsymbol{A}_i$, $\boldsymbol{B}_i$, $\boldsymbol{C}_i$ and $\boldsymbol{D}_i$) by an ith duty-cycle (k_i). In this context, the matrices manipulation shown in (4) results in the state matrix $\sum_{i=1}^{4}\boldsymbol{A}_i k_i = \boldsymbol{A}$, input matrix $\sum_{i=1}^{4}\boldsymbol{B}_i k_i = \boldsymbol{B}$, output matrix $\sum_{i=1}^{4}\boldsymbol{C}_i k_i = \boldsymbol{C}$ and in the feedforward matrix $\sum_{i=1}^{4}\boldsymbol{D}_i k_i = \boldsymbol{D} = 0$

$$\begin{cases}
\dot{\boldsymbol{x}} = \left(\sum_{i=1}^{4}\boldsymbol{A}_i k_i\right)\boldsymbol{x} + \left(\sum_{i=1}^{4}\boldsymbol{B}_i k_i\right)\boldsymbol{u} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u},\\
\boldsymbol{y} = \left(\sum_{i=1}^{4}\boldsymbol{C}_i k_i\right)\boldsymbol{x} + \underbrace{\left(\sum_{i=1}^{4}\boldsymbol{D}_i k_i\right)}_{=0}\boldsymbol{u} = \boldsymbol{C}\boldsymbol{x} + \underbrace{\boldsymbol{D}}_{=0}\boldsymbol{u}\,.
\end{cases} \tag{4}$$

$$
\left.\begin{aligned}
\frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} =& -\left(r_{\mathrm{L1}}+\left(\frac{(r_{\mathrm{C2}}+r_{\mathrm{S2}})r_{\mathrm{C1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\right)\frac{i_{L1}}{L_1}-\left(\frac{r_{\mathrm{C1}}r_{\mathrm{S1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{L2}}{L_1}\\
&+\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{L_1}-\left(\frac{r_{\mathrm{C1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{L_1}-\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{L_1}+\frac{v_{\mathrm{in}}}{L_1}\\
\frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} =& -\left(\frac{r_{\mathrm{C1}}r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{L_2}-\left(r_{\mathrm{L2}}+\left(\frac{(r_{\mathrm{C1}}+r_{\mathrm{C2}})r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\right)\frac{i_{\mathrm{L2}}}{L_2}\\
&+\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{L_2}+\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{L_2}-\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{L_2}+\frac{v_{\mathrm{in}}}{L_2}\\
\frac{\mathrm{d}v_{\mathrm{C1}}}{\mathrm{d}t} =& -\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{C_1}-\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L2}}}{C_1}-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C_1}\\
&-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C_1}+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{C_1}\\
\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} =& \left(\frac{r_{\mathrm{C1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{C_2}-\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L2}}}{C_2}-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C_2}\\
&-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C_2}+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{C_2}\\
&\times\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C_2}-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C_2}\\
&+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{C_2}\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C}+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C}\\
&-\left(\frac{1}{R_{\mathrm{o}}}+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\right)\frac{v_{\mathrm{C}}}{C}-\frac{i_{\mathrm{o}}}{C}
\end{aligned}\right\}k_2, \tag{2}
$$

$$
\left.\begin{aligned}
\frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} =& -\left(r_{\mathrm{L1}}+\left(\frac{(r_{\mathrm{C2}}+r_{\mathrm{S2}})r_{\mathrm{C1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\right)\frac{i_{\mathrm{L1}}}{L_1}-\left(\frac{r_{\mathrm{C1}}r_{\mathrm{S1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L2}}}{L_1}\\
&+\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{L_1}-\left(\frac{r_{\mathrm{C1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{L_1}-\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{L_1}+\frac{v_{\mathrm{in}}}{L_1}\\
\frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} =& -\left(\frac{r_{\mathrm{C1}}r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{L_2}-\left(r_{\mathrm{L2}}+\left(\frac{(r_{\mathrm{C1}}+r_{\mathrm{C2}})r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\right)\frac{i_{\mathrm{L2}}}{L_2}\\
&+\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{L_2}+\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{L_2}-\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{L_2}+\frac{v_{\mathrm{in}}}{L_2}\\
\frac{\mathrm{d}v_{\mathrm{C1}}}{\mathrm{d}t} =& -\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{C_1}-\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L2}}}{C_1}-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C_1}\\
&-\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C_1}+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{C_1}\\
\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} =& \frac{1}{C_2}\left(\frac{r_{\mathrm{C1}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{C_2}-\frac{1}{C_2}\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L2}}}{C_2}\\
&-\frac{1}{C_2}\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C_2}-\frac{1}{C_2}\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C_2}+\frac{1}{C_1}\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C}}}{C_2}\\
\frac{\mathrm{d}v_{\mathrm{C}}}{\mathrm{d}t} =& -\frac{1}{C}\left(\frac{r_{\mathrm{C2}}+r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L1}}}{C}-\frac{1}{C}\left(\frac{r_{\mathrm{S2}}}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{i_{\mathrm{L2}}}{C}\\
&+\frac{1}{C}\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C1}}}{C}+\frac{1}{C}\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\frac{v_{\mathrm{C2}}}{C}-\frac{1}{C}\left(\frac{1}{R_{\mathrm{o}}}+\left(\frac{1}{r_{\mathrm{C1}}+r_{\mathrm{C2}}+r_{\mathrm{S2}}}\right)\right)\frac{v_{\mathrm{C}}}{C}-\frac{i_{\mathrm{o}}}{C}
\end{aligned}\right\}k_4\,. \tag{3}
$$

From Fig. 2*a*, the interval in which a single transistor is OFF (S_1 or S_2) is $(1-k)T_{\mathrm{S}}$. Considering the same picture, the transistors are commuting with 180° of displacement, then $k_1T_{\mathrm{S}}+k_2T_{\mathrm{S}}=1/2T_{\mathrm{S}}$ and $k_3T_{\mathrm{S}}+k_4T_{\mathrm{S}}=1/2T_{\mathrm{S}}$. Based on the IBVM operation characteristics, k_2 and k_4 are equal to $1-k$, while $k_1=k_3=1/2-(1-k)=k-1/2$. In this context, the state matrix assumes the form established in (5)

$$
\begin{aligned}
\boldsymbol{A} &= \sum_{i=1}^{4}\boldsymbol{A}_i k_i = \boldsymbol{A}_1\left(k-\frac{1}{2}\right)+\boldsymbol{A}_2(1-k)+\boldsymbol{A}_3\left(k-\frac{1}{2}\right)+\boldsymbol{A}_4(1-k)\\
&= (-\boldsymbol{A}_1+\boldsymbol{A}_2+\boldsymbol{A}_4)+k(2\boldsymbol{A}_1-\boldsymbol{A}_2-\boldsymbol{A}_4)\,.
\end{aligned} \tag{5}
$$

Therefore, substituting (5) in (4) and taking into account that $\boldsymbol{B}=\sum_{i=1}^{4}\boldsymbol{B}_i k_i=\boldsymbol{B}_1$ and $\boldsymbol{D}=0$, the IBVM average model (6) is obtained

$$
\begin{cases}
\dot{\boldsymbol{x}} = [(-\boldsymbol{A}_1+\boldsymbol{A}_2+\boldsymbol{A}_4)+k(2\boldsymbol{A}_1-\boldsymbol{A}_2-\boldsymbol{A}_4)]\boldsymbol{x}+\boldsymbol{B}\boldsymbol{u},\\
\boldsymbol{y} = \boldsymbol{C}\boldsymbol{x}\,.
\end{cases} \tag{6}
$$

With the aim to obtain the IBVM transfer function considering the duty cycle as the input variable, the small signal analysis is applied to the average model presented in (6). Therefore, as shown in (7), the input variables, output variables, state variables, and the duty-cycle are analysed considering the ac (small signals) and dc (steady-state regime) components, i.e. $\boldsymbol{u}=\boldsymbol{U}+\hat{\boldsymbol{u}}$, $\boldsymbol{y}=\boldsymbol{Y}+\hat{\boldsymbol{y}}$, $\boldsymbol{x}=\boldsymbol{X}+\hat{\boldsymbol{x}}$ and $k=K+\hat{k}$, where the uppercase variable denotes the

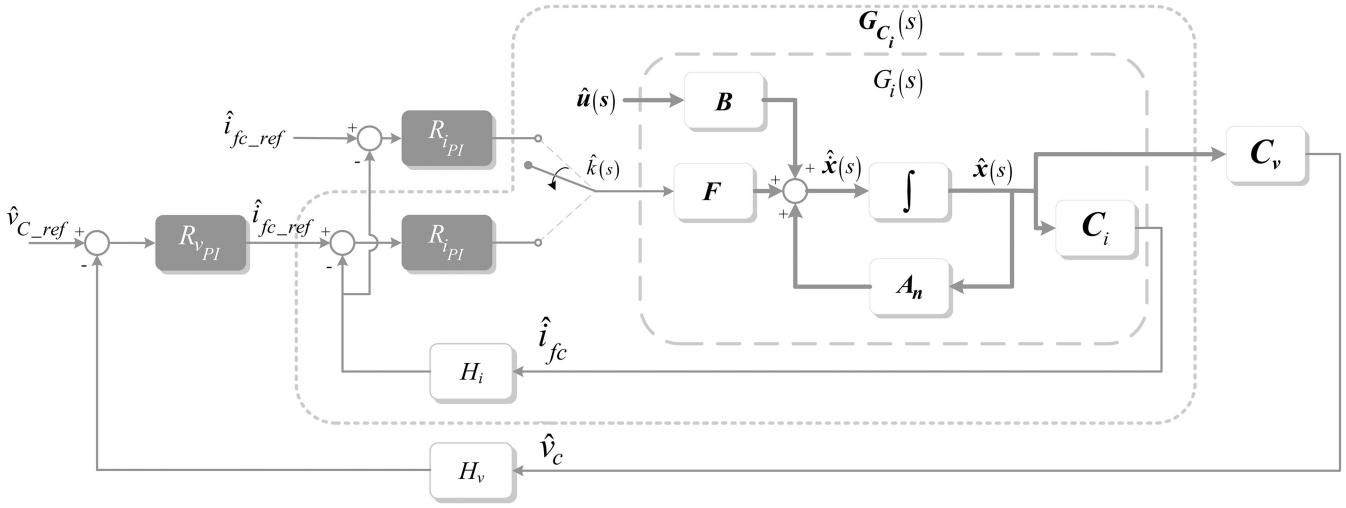


Fig. 3 *Block diagrams for the IBVM current and voltages loops*

steady-state value, and the circumflex accent means the small-signal perturbation around the quiescent operation point

$$\begin{cases} \dot{\boldsymbol{X}} + \dot{\hat{\boldsymbol{x}}} = \left[(-\boldsymbol{A}_1 + \boldsymbol{A}_2 + \boldsymbol{A}_4) + \left(K + \hat{k}\right)(2\boldsymbol{A}_1 - \boldsymbol{A}_2 - \boldsymbol{A}_4)\right](\boldsymbol{X} + \hat{\boldsymbol{x}}) \\ \qquad\qquad + \boldsymbol{B}(\boldsymbol{U} + \hat{\boldsymbol{u}}), \\ \boldsymbol{Y} + \hat{\boldsymbol{y}} = \boldsymbol{C}(\boldsymbol{X} + \hat{\boldsymbol{x}}). \end{cases} \tag{7}$$

In (7), the gradient of the state vector in steady-state regime is zero $\left(\dot{\boldsymbol{X}} = 0\right)$, then $\boldsymbol{X} = -\boldsymbol{A}_n^{-1}\boldsymbol{B}\boldsymbol{U}$, where the state matrix $\boldsymbol{A}_n$ is defined by $\boldsymbol{A}_n = (-\boldsymbol{A}_1 + \boldsymbol{A}_2 + \boldsymbol{A}_4) + K(2\boldsymbol{A}_1 - \boldsymbol{A}_2 - \boldsymbol{A}_4)$. Also, the matrix $\boldsymbol{F} = (2\boldsymbol{A}_1 - \boldsymbol{A}_2 - \boldsymbol{A}_4)\boldsymbol{X}$ is defined considering the input $\hat{k}$, which leads to the following equation:

$$\begin{cases} \dot{\hat{\boldsymbol{x}}} = [(-\boldsymbol{A}_1 + \boldsymbol{A}_2 + \boldsymbol{A}_4) + K(2\boldsymbol{A}_1 - \boldsymbol{A}_2 - \boldsymbol{A}_4)]\hat{\boldsymbol{x}} \\ \qquad + \boldsymbol{B}\hat{\boldsymbol{u}} + (2\boldsymbol{A}_1 - \boldsymbol{A}_2 - \boldsymbol{A}_4)\boldsymbol{X}\hat{k}, \\ \hat{\boldsymbol{y}} = \boldsymbol{C}\hat{\boldsymbol{x}}. \end{cases} \tag{8}$$

To simplify the ac model defined in (8), $\boldsymbol{F}$ is incorporated into $\boldsymbol{B}$ to produce a new matrix $\boldsymbol{B}' = [\boldsymbol{B} \quad \boldsymbol{F}]$. In the same way, $\hat{k}$ is incorporated into the input vector $\hat{\boldsymbol{u}}$ to produce a new input vector $\hat{\boldsymbol{u}}' = \left[\hat{\boldsymbol{u}} \quad \hat{k}\right]^{\mathrm{T}}$, according to the following equation:

$$\begin{cases} \dot{\hat{\boldsymbol{x}}} = \boldsymbol{A}_n\hat{\boldsymbol{x}} + B\hat{\boldsymbol{u}} + \boldsymbol{F}\hat{k} = \boldsymbol{A}_n\hat{\boldsymbol{x}} + [\boldsymbol{B}\ \boldsymbol{F}]\begin{bmatrix}\hat{\boldsymbol{u}} \\ \hat{k}\end{bmatrix} \\ \quad = \boldsymbol{A}_n\hat{\boldsymbol{x}} + \boldsymbol{B}'\hat{\boldsymbol{u}}', \\ \hat{\boldsymbol{y}} = \boldsymbol{C}\hat{\boldsymbol{x}} \end{cases}. \tag{9}$$

3 IBVM control analysis

This section presents an analysis for the grid-connected control modes presented in Fig. 1. Bearing in mind that the classical control technique applied to the three-phase dc/ac converter shown in Fig. 1 have already been exhaustively addressed in the literature, this section is limited only to design and analyse the IBVM control structures.

The control structures for both operating modes are illustrated in Fig. 3. Additionally, in the same figure $R_{i\mathrm{PI}}$ and $R_{v\mathrm{PI}}$ are the PI controllers for the two control modes, while H_v and H_i are the dc voltage and current sensors gains, respectively. Also, considering the small signal model, $\hat{v}_{\mathrm{c\_ref}}$ is the dc-link voltage reference, $\hat{v}_\mathrm{c}$ is the dc-link voltage measured at the IBVM terminals, $\hat{i}_{\mathrm{fc\_ref}}$ is the FC current reference and $\hat{i}_{\mathrm{fc}}$ is the current measured at the FC terminals.

Since the IBVM control structure in mode 2 is simpler, first we present the control analysis of mode 2, and then, the control analysis in mode 1.

3.1 Control mode 2: controlling the FC operating point

To design the current controller, the current input of the dc/dc converter is calculated as a function of the ac duty-cycle. To achieve this, we apply Laplace's transform in (9) and make the ac input vector equals to zero ($\widehat{\boldsymbol{u}}(s) = 0$), i.e. we evaluate the effects of the ac duty cycle ($\hat{k}$) on the ac state vector $\left(\hat{\boldsymbol{x}}(s)\big|_{\hat{k}} = (s\boldsymbol{I} - \boldsymbol{A}_n)^{-1}\boldsymbol{F}\hat{k}(s)\right)$.

To select the variable of interest in the state vector $\hat{\boldsymbol{x}}(s)\big|_{\hat{k}}$, the system output $\hat{\boldsymbol{y}} = \boldsymbol{C}\hat{\boldsymbol{x}}$ is obtained by multiplying $\hat{\boldsymbol{x}}(s)\big|_{\hat{k}}$ by $\boldsymbol{C} = \boldsymbol{C}_i = [1\ 1\ 0\ 0\ 0]$, which is the FC current. The result is the transfer function that represents the FC current, considering the duty-cycle as input in the following equation:

$$\frac{\hat{i}_\mathrm{L}(s)}{\hat{k}(s)} = \boldsymbol{C}_i(s\boldsymbol{I} - \boldsymbol{A}_n)^{-1}\boldsymbol{F}. \tag{10}$$

To assess the performance of the current controller $\boldsymbol{R}_{i\mathrm{PI}}$, using (11), we calculate the open loop transfer function, plot the frequency response, and the root-locus to estimate the system stability and performance as well.

Using the transfer function (11), Fig. 4*a* presents the current open loop root-locus. In this figure, the PI zero is plotted with three different values. The dashed line represents the compensator located at $k_{i_i}/k_{p_i} = 1000$, while the solid black line represents the PI located at $k_{i_i}/k_{p_i} = 4,434.0$, according to (12) and the parameters listed in Table 1.

$$\begin{aligned} H_i R_{i\mathrm{PI}}(s) G_i(s) &= H_i\left[k_{p_i}\frac{((k_{i_i}/k_{p_i}) + s)}{s}\right. \\ \left.\frac{\hat{i}_L(s)}{\hat{k}}\right. &= H_i\left[k_{p_i}\frac{((k_{i_i}/k_{p_i}) + s)}{s}\right]\boldsymbol{C}_i(s\boldsymbol{I} - \boldsymbol{A}_n)^{-1}\boldsymbol{F}. \end{aligned} \tag{11}$$

Additionally, from Fig. 4*a*, we observe that for $k_{i_i}/k_{p_i} = 1$, the dominant poles present lower damping factors when compared with higher values of k_{i_i}/k_{p_i}. However, to decrease the time to achieve a smaller steady-state error, the integrator gain must be increased. Then, for the designed PI controller, the dominant pole pair present a damping factor of $\zeta = 0.327$.

To complement the analysis, Fig. 4*b* presents the frequency response for the PI current controller (12) designed according to the parameters listed in Table 1

$$R_{i_{\mathrm{PI}}}(s) = 0.9505 + \frac{4,214.5}{s}. \tag{12}$$

3.2 Control mode 1: FC cascade control

In the second control structure, the inner loop regulates the current through the FC terminals and the outer loop the dc-link voltage. Using the same current controller designed in the previous section, to find the inner loop transfer function, we calculate the state space representation in time domain with the inner loop closed (13) using the control diagram illustrated in Fig. 3

$$\dot{\hat{x}} = \boldsymbol{A}_n\hat{\boldsymbol{x}} + \boldsymbol{B}\hat{\boldsymbol{u}} - H_i R_{i_{\mathrm{PI}}}\boldsymbol{F}\boldsymbol{C}_i\hat{\boldsymbol{x}} + R_{i_{\mathrm{PI}}}\boldsymbol{F}\hat{i}_{\mathrm{fc\_ref}}. \tag{13}$$

Then, we apply Laplace's transform in (13), and make the ac input vector equal to zero ($\widehat{\boldsymbol{u}}(s) = 0$) to find the state vector response for the current reference input (14). Then, replacing $\hat{v}_{\mathrm{c}}(s) = \boldsymbol{C}_{\mathrm{v}}\hat{\boldsymbol{x}}(s)\big|_{\hat{k}}$ into $\boldsymbol{G}_{\boldsymbol{c}_i}(s)$, with the output vector $\boldsymbol{C}_{\mathrm{v}} = [0\ 0\ 0\ 0\ 1]$, results in the inner loop transfer function (15) that represents the dc-link voltage response with the FC current reference input

$$\boldsymbol{G}_{\boldsymbol{c}_i}(s) = \frac{\hat{\boldsymbol{x}}(s)\big|_{\hat{k}}}{\hat{i}_{\mathrm{fc\_ref}}(s)} = \left(s\boldsymbol{I} - \boldsymbol{A}_n + H_i R_{i_{\mathrm{PI}}}(s)\boldsymbol{F}\boldsymbol{C}_{\boldsymbol{i}}\right)^{-1} R_{i_{\mathrm{PI}}}(s)\boldsymbol{F}, \tag{14}$$

$$\frac{\hat{v}_{\mathrm{c}}(s)}{\hat{i}_{\mathrm{fc\_ref}}(s)} = \boldsymbol{C}_{\mathrm{v}}\boldsymbol{G}_{\boldsymbol{c}_i}(s). \tag{15}$$

After reducing the current loop to the transfer function (15), we calculate the outer open-loop transfer function (16) to estimate the stability of the voltage loop when a PI controller $\left(R_{v_{\mathrm{PI}}}(s)\right)$ is used. Additionally, we compute the closed loop transfer function according to the following equation:

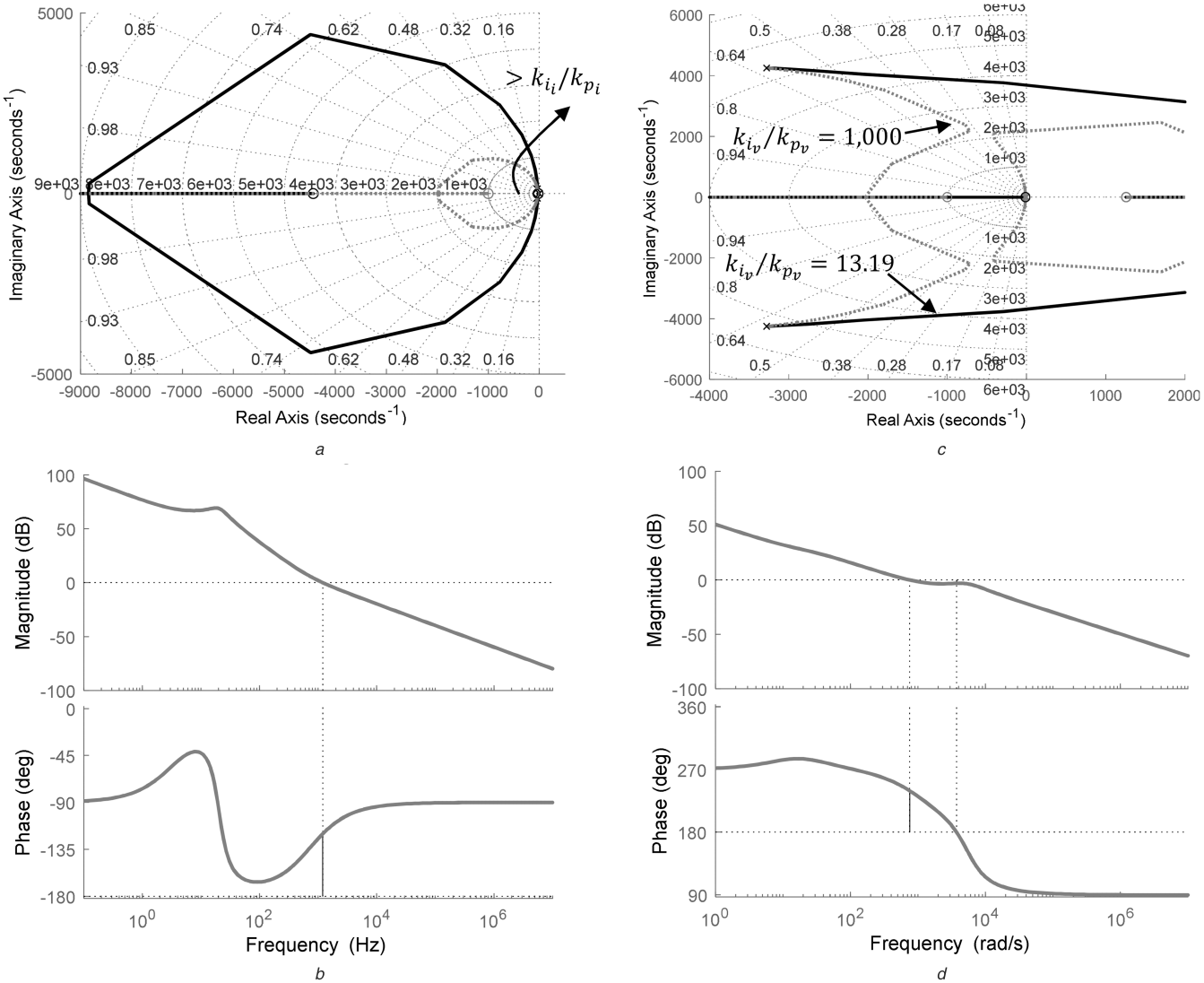


Fig. 4 *Control analysis for the IBVM voltage and current loops*
(a) Root-locus diagram for the current open loop, ***(b)*** Frequency response for the current open loop, ***(c)*** Root-locus diagram for the voltage open loop, ***(d)*** Frequency response for the voltage open loop

Table 1 IBVM PI current controller parameters

Parameters	Values
phase margin	60°
cut-off frequency	1200 Hz
R_{O}	62.5 Ω
H_i	0.0250

$$H_v R_{v_{\mathrm{PI}}}(s)\boldsymbol{C}_v\boldsymbol{G}_{c_i}(s) = H_v\left[k_{p_v}\frac{((k_{i_v}/k_{p_v})+s)}{s}\right]\left[\boldsymbol{C}_v\left(s\boldsymbol{I}-\boldsymbol{A}_n+H_i\left[k'_{p_v}\frac{((k_{i_v}/k_{p_v})+s)}{s}\right]\boldsymbol{F}\boldsymbol{C}_i\right)^{-1}\left[k'_{p_v}\frac{((k_{i_v}/k_{p_v})+s)}{s}\right]\boldsymbol{F}\right], \quad (16)$$

$$\frac{\hat{v}_{\mathrm{C}}(s)}{\hat{v}_{C_{\mathrm{ref}}}(s)} = \frac{H_{\mathrm{v}}R_{v_{\mathrm{PI}}}(s)\boldsymbol{C}_{\mathrm{v}}\boldsymbol{G}_{\boldsymbol{c}_i}(s)}{1+R_{v_{\mathrm{PI}}}(s)\boldsymbol{C}_{\mathrm{v}}\boldsymbol{G}_{\boldsymbol{c}_i}(s)H_{\mathrm{v}}}. \quad (17)$$

The same analysis used in the previous section is applied to the voltage controller. In this case, Fig. 4*c* shows the root-locus for the voltage controller in the dashed line at $k_{i_v}/k_{p_v} = 1000$ and in the solid line at $k_{i_v}/k_{p_v} = 13.19$.

At first, we notice a zero in the right half plane, which characterises the system as a non-minimum phase. The zero on the right half plane attracts the pole pairs from the left half plane to the right half plane as the gain increases. This characteristic limits the system bandwidth and many techniques to mitigate the presence of a zero at the right half plane, such as operation in discontinuous conduction mode or the addition of extra circuits in the dc/dc converter topology have been proposed in the literature [29].

The voltage controller bandwidth is limited by the switching frequency and also by the inner loop bandwidth. In this case, Table 2 shows the parameters for the PI voltage controller (18). As shown in the frequency response in Fig. 4*d*, even though the non-minimum phase tends to limit the system bandwidth, the controller is properly designed for a cut-off frequency one decade below the current controller (120 Hz) with a phase margin of 60°.

From Fig. 4*c*, we also notice that as the ratio k_{i_i}/k_{p_i} increases, the pole pairs near the origin move in the direction of the imaginary axis. In other words, the damping factor decreases indicating a more oscillatory behaviour

Table 2 IBVM PI voltage controller parameters

Parameters	Values
phase margin	60°
cut-off frequency	120 Hz
R_{O}	62.5 Ω
H_{v}	0.0020

Table 3 FC parameters

Parameters	Values
number of cells	48
maximum power	1.0 kW
voltage and current at maximum power	28.8 V–35 A
maximum temperature of operation	65°
hydrogen pressure	0.45–0.55 (bar)
humidification	self-humidified
consume of hydrogen	13, l/min
efficiency	40% at 28.8 V

$$R_{v_{\mathrm{PI}}}(s) = 118.9 + \frac{1,569.2}{s}. \quad (18)$$

4 Experimental validation

To test the proposed approach presented, we assembled a test-bed (VSI + IBVM) powered by a FC from Horizon Technologies H-1000. The VSI uses a pulse width modulation with a switching frequency (f_{S}) of 12 kHz. In stand-alone mode, the VSI is controlled by a double loop control in the synchronous reference frame, i.e. the ac current is adjusted in the inner loop while the ac voltage or the dc-link voltage are controlled in the outer loop. On the other hand, when the VSI is connected to the grid, the VSI algorithm switches to the control schemes presented in Fig. 1. In Tables 3–5, we show the main parameters of the FC, VSI, and IBVM, respectively.

The methodologies to design the control loops and stability analysis of the ac-side are not addressed in this study and it can be found in a vast number of papers in the literature, hence, we are committed to evaluate the performance of the IBVM control structures presented previously, and the effect of the ac-side on the control structures of the dc-side.

In this context, in this section, we present the experimental results for both modes of operation. The procedure used in both control modes, consists of starting the system in stand-alone mode until the ac voltage produced by the VSI is in synchronism with the grid, according to the phase-locked loop (PLL) algorithm. After the synchronisation, the S_{g} relay is switched on and the system starts operating in grid-connected mode [30].

With the aim to show the system start-up used in both operating modes before the connection to the grid, Section 4.1 presents an analysis in the system behaviour during the initialisation in stand-alone mode. On the other hand, Sections 4.2 and 4.3 present the analysis for the system in grid connected operation for mode 1 and mode 2, respectively.

4.1 System start-up

Initially, the relay S_{g} is open and the DG system operates in stand-alone mode. In this scenario, Fig. 5*a* shows the VSI and IBVM converter start-up with the FC connected to the IBVM input. With the aim to avoid current peaks at the FC terminals, we established a ramp rising >1.5 s. When the IBVM is turned on, the dc-link voltage is incremented from 45 V (FC voltage of open circuit) to the dc-link voltage set-point (250 V).

Regarding the FC behaviour during the start-up procedure, also in Fig. 5*a*, we detect that v_{in} drops 8 V along 300 ms, which occurs at the FC activation region. In addition, we notice a decreasing of 9 V in 1.3 s when the FC enters the linear region.

When the ac control algorithm start-up, we notice a current peak of 2 A (an overshoot of 40%) at the DG terminal, on the other hand, at the steady-state regime the system presents a low level of distortion (Total Harmonic Distortion less than 5%).

4.2 Grid-connected control mode 1: FC cascade control

After analysing the DG system behaviour in stand-alone mode, we investigate the system in grid-connected mode, i.e. when S_{g} is

Table 4 VSI parameters

Parameters	Values
phase voltage, rms,	63.5 V
dc-link voltage	250 V
gain of the transformer	2:1
L_{dg}	2 mH
r_{dg}	100 mΩ
L_{g}	5 mH
r_{g}	100 mΩ
C_{f}	10 μF
r_{f}	10 Ω

Table 5 IBVM parameters

Parameters	Values
dc-link voltage	250 V
c	1.36 mF
L_1, L_2	870 μH
r_{L1}, r_{L2}	34.8 mΩ
C_1, C_2	1 μF
r_{C1}, r_{C2}	29 mΩ
r_{S1}, r_{S2}	24 mΩ
f_S	12 kHz

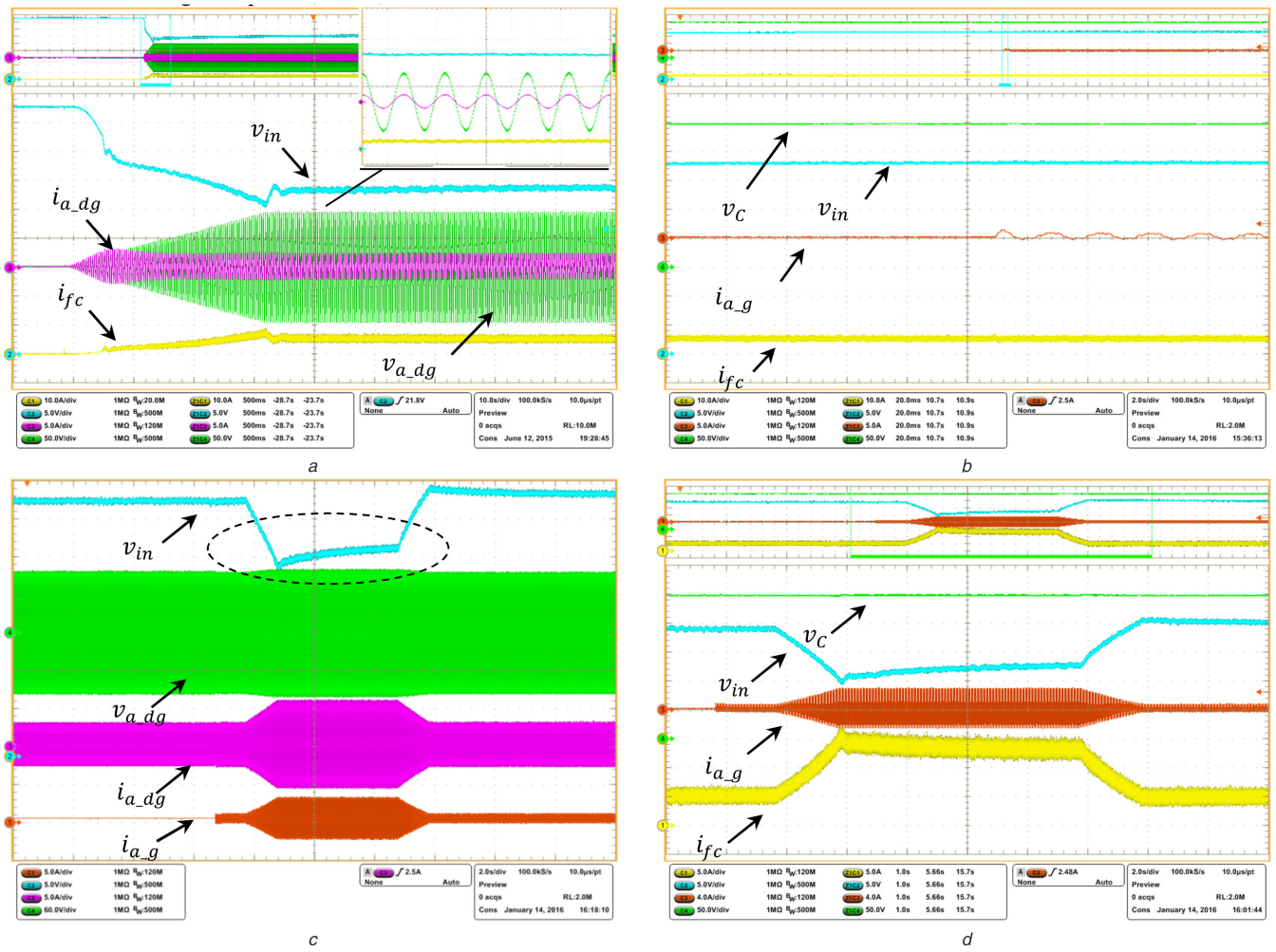


Fig. 5 *Experimental results for stand-alone operation and grid-connected control in mode 1*

(a) Vertical: v_{a_dg} in green 50 V/div, i_{a_dg} in pink 5 A/div, v_{in} in blue 5 V/div, i_{fc} in yellow 10 A/div, horizontal: 500 ms/div, ***(b)*** Vertical: v_C in green 50 V/div, i_{a_g} in brown 5 A/div, v_{in} in blue 5 V/div, i_{fc} in yellow 10 A/div, horizontal: 20 ms/div, ***(c)*** Vertical: v_{a_dg} in green 60 V/div, i_{a_dg} in pink 5 A/div, v_{in} in blue 5 V/div, i_{a_g} in brown 5 A/div, horizontal: 2 s/div, ***(d)*** Vertical: v_C in green 50 V/div, i_{a_g} in brown 5 A/div, v_{in} in blue 5 V/div, i_{fc} in yellow 10 A/div, horizontal: 1 s/div

closed. The transition between the stand-alone and grid-connected control in mode 1 is shown in Figs. 5*b*–*d*. Before closing the S_g relay, the PLL algorithm synchronises the DG voltages (v_{a,b,c_dg}) with the grid voltages (v_{a,b,c_g}). Once the DG voltages amplitude and phase comply with the grid instantaneous voltages, the relay S_g is safely closed.

After closing the S_g relay, Fig. 5*b* shows that a small current of 70 mA (1% of the current supplied by the FC) starts flowing between the DG and the grid.

After the synchronisation procedure, the DG is able to transfer power to the grid, as shown in Figs. 5*c* and *d*. To inject power to the grid, the DG current increases with a ramp reference. Considering that the local load is constant, the remaining power is fully injected to the grid until the current grid reaches 5 A peak-to-peak.

Moreover, when the current is drawn from the FC, the FC voltage drops 9 V, according to the ac current reference. However, when the ac current reaches the constant value, the FC voltage increases 2.5 V in 8 s. The FC slow dynamic behaviour is related to the FC double-layer capacitance, and to the time that the chemical reaction takes to achieve a new equilibrium point. When the equilibrium point is modified, some variables, such as the membrane humidity, are changed slowly.

Lastly, regarding the FC current and dc-link voltage frequency spectrum, as shown in Fig. 6, the FC current presents a maximum amplitude of 70 mA (1% of the current supplied by the FC) between 3 and 4 Hz and the dc-link voltage presents a peak voltage of 0.14 V between the same frequency bandwidth (3 and 4 Hz).

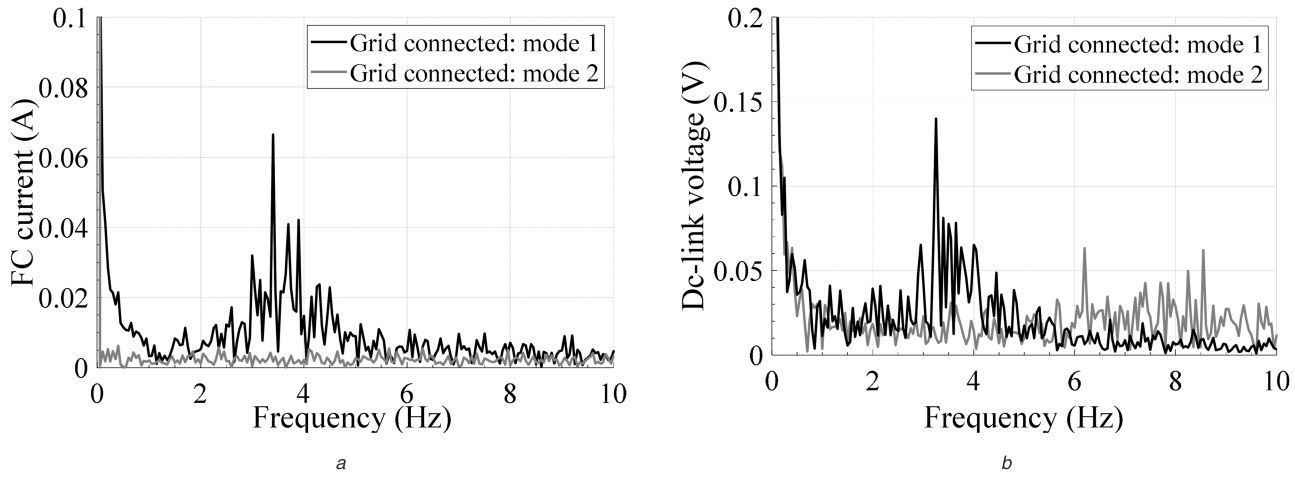


Fig. 6 *DC-side voltage and current frequency spectrum*
(a) FC current frequency spectrum, ***(b)*** DC-link voltage frequency spectrum

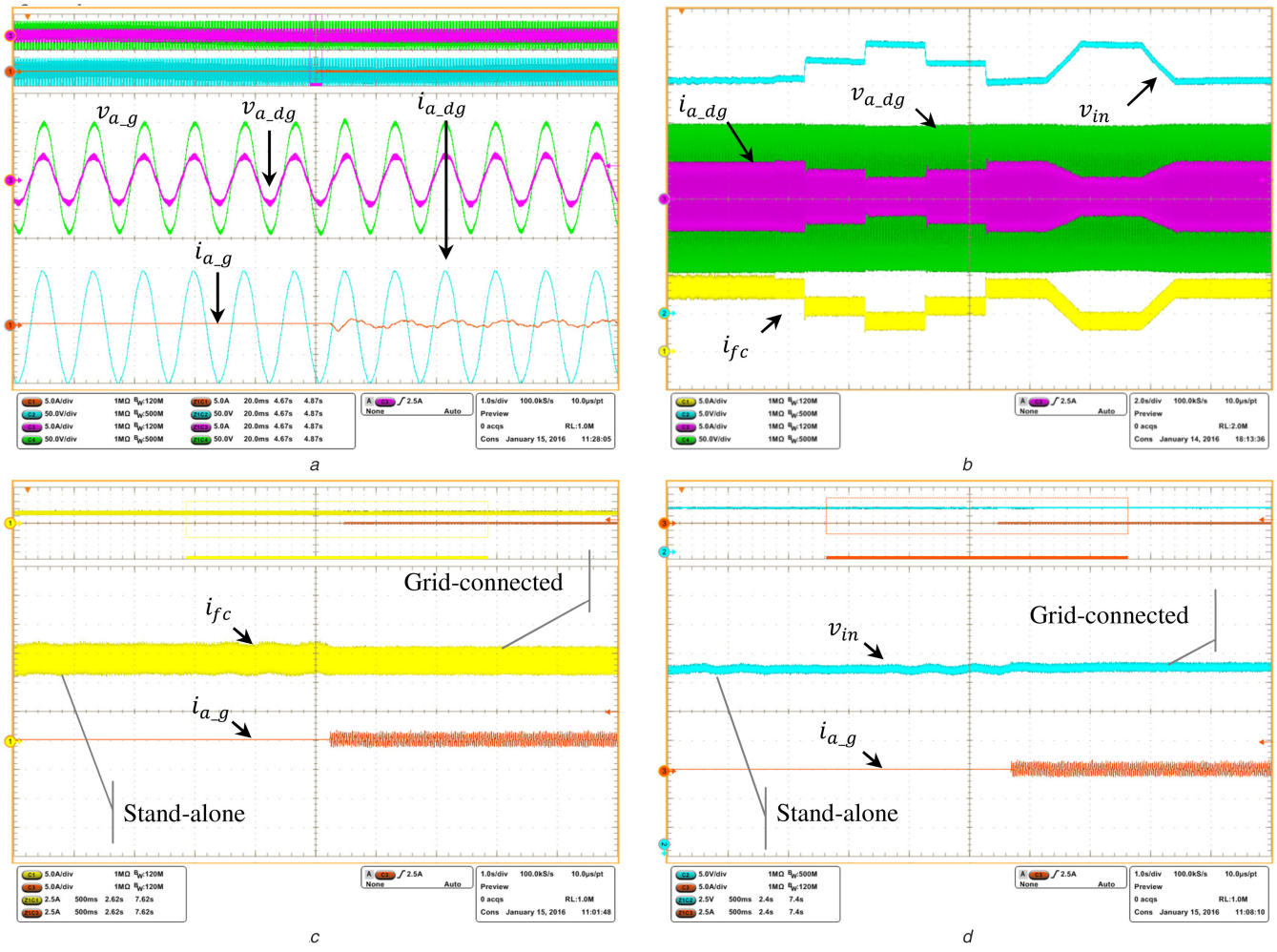


Fig. 7 *Experimental results for grid-connected control in mode 2*
(a) Vertical: v_{a_dg} in green 50 V/div, i_{a_dg} in pink 5 A/div, v_{a_g} in blue 50 V/div, i_{a_g} in brown 5 A/div, horizontal: 20 ms/div, ***(b)*** Vertical: v_{a_dg} in green 50 V/div, i_{a_dg} in pink 5 A/div, v_{in} in blue 5 V/div, i_{fc} in yellow 5 A/div, horizontal: 2 s/div, ***(c)*** Vertical: i_{fc} in yellow 5 A/div, i_{a_g} in brown 2.5 A/div. horizontal: 1 s/div, ***(d)*** Vertical: v_{in} in blue 5 V/div, i_{a_g} in brown 2.5 A/div. Horizontal: 1 s/div

4.3 Grid-connected control mode 2: controlling the FC operating point

In contrast to control mode 1, in mode 2 the dc-link voltage stabilisation is performed by the VSI, and the FC current set-point is implemented in the IBVM control loop. Consequently, the energy supplied to the grid depends exclusively on the FC current set-point.

The experimental procedure starts in stand-alone mode, after the synchronisation, the DG algorithm switches to the control mode 2 (Fig. 7*a*). As with mode 1, after the synchronisation a small current flows between the DG and the grid.

Once the DG is in grid-connected mode, the current reference is increased, in this case, the injected current is controlled by i_{fc_ref}. In this context, Fig. 7*b* presents the experimental results for various levels of current injected. In this result, we also notice a smaller oscillation in the FC voltage and current. Then, to compare the performance between this control mode 2 and mode 1, Fig. 6

presents the FC current and dc-link voltage frequency spectrum using the experimental results in Figs. 7*c* and *d*.

Unlike in the grid-connected control mode 1 and stand-alone operation, in this mode, the FC current and dc-link voltage peak do not exist at frequencies between 3 and 4 Hz. On the other hand, in this control mode, we notice a small amplitude (peak of 65 mV) in the dc-link voltage frequencies between 5 and 15 Hz.

5 Efficiency analysis

In this section, we introduce the IBVM converter efficiency analysis. Since the designed IBVM converter can withstand an input current up to 40 A, the simulations and experimental results in this section are performed using an inductor with higher parasitic resistance with the aim to confirm the mathematical model equivalence with the prototype results. Then, the parameters regarding the inductor used for the experimental results in this section are listed in Table 6.

To evaluate the IBVM efficiency ($\eta = P_O/P_{in}$), we calculate the power at the IBVM input (P_{in}) and output terminals (P_O) as shown in (19), where V_C, V_{in} and I_{fc} are the output voltage, input voltage and FC current in steady-state, respectively

$$\begin{cases} P_O = \int \frac{v_C^2}{R_o} dt = \frac{V_C^2}{R_o}, \\ P_{in} = \int v_{in} i_{fc} dt = \int v_{in} i_{fc} dt = V_{in} I_{fc}. \end{cases} \tag{19}$$

To obtain the efficiency mathematical model, the relationship between V_C and V_{in} is computed, which consists of finding the IBVM static voltage gain. To achieve this, Laplace's transform is applied in (6) to determine the IBVM voltage gain when $\boldsymbol{C} = \boldsymbol{C}_v$, $\boldsymbol{D} = 0$, and the input vector $\boldsymbol{u}(s)$ is analysed considering only $v_{in}(s)$. As a result, we obtain the output vector $\boldsymbol{y}(s) = v_C(s) = \boldsymbol{C}_v(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}v_{in}(s) + \underbrace{\boldsymbol{D}}_{=0} v_{in}(s)$. Taking into account the previous information, the voltage gain transfer function ($M_{IBVM}(s)$) is found according to (20). However, if the final value theorem is applied on the same equation, the result is the static voltage gain (m_{IBVM}) according to following equation:

$$M_{IBVM}(s) = \frac{v_C(s)}{v_{in}(s)} = \boldsymbol{C}_v(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \underbrace{\boldsymbol{D}}_{=0}, \tag{20}$$

$$m_{IBVM} = \lim_{s \to 0} sM_{IBVM}(s)\frac{1}{s} = -\boldsymbol{C}_v\boldsymbol{A}^{-1}\boldsymbol{B} + \underbrace{\boldsymbol{D}}_{=0}. \tag{21}$$

From the mathematical model defined in (21), we apply the following approximation $r_S = r_{S1} = r_{S2}$, $r_L = r_{L1} = r_{L2}$ and $r_C = r_{C1} = r_{C2}$ to calculate the static gain in the following equation:

$$m_{IBVM} = \frac{V_C}{V_{in}} = -\frac{4R_o(k-1)}{2k^2R_o - k(2r_C + r_S + 4R_o) + 2(R_o + r_C) + 4r_L + 5r_S}. \tag{22}$$

In the next procedure, we compute the equivalent admittance at the FC terminals. To reach this, Laplace's transform is applied in (6) when $\boldsymbol{C} = \boldsymbol{C}_i$, $\boldsymbol{D} = 0$, and the input vector $\boldsymbol{u}(s)$ is analysed considering only $v_{in}(s)$ as input.

The consequence is the output vector $\boldsymbol{y}(s) = i_L(s) = \boldsymbol{C}_i(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}v_{in}(s) + \underbrace{\boldsymbol{D}}_{=0} v_{in}(s)$. Considering the previous evidence, the admittance in the frequency domain ($Y_{IBVM}(s)$) is obtained as found in (23). Then, if the final value theorem is also applied on the same equation the result is the static admittance (y_{IBVM}) according to (24)

Table 6 IBVM parameters for the efficiency analysis

Parameters	Values
L_1, L_2	5 mH
r_{L1}, r_{L2}	113 mΩ

$$Y_{IBVM}(s) = \frac{I_L(s)}{V_{in}(s)} = \boldsymbol{C}_i(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \underbrace{\boldsymbol{D}}_{=0}, \tag{23}$$

$$y_{IBVM} = \lim_{s \to 0} sY_{IBVM}(s)\frac{1}{s} = -\boldsymbol{C}_i\boldsymbol{A}^{-1}\boldsymbol{B} + \underbrace{\boldsymbol{D}}_{=0}. \tag{24}$$

From the mathematical model proposed in (24), and using the following simplification $r_S = r_{S1} = r_{S2}$, $r_L = r_{L1} = r_{L2}$ and $r_C = r_{C1} = r_{C2}$, we also calculate the static admittance according to the following equation:

$$y_{IBVM} = \frac{I_{fc}}{V_{in}} = \frac{8}{2R_ok^2 - (4R_o + 2r_C + r_S)k + 2(R_o + r_C) + 4r_L + 5r_S}. \tag{25}$$

Finally, (22) and (25) are used in (26) to obtain (27), which represents the IBVM efficiency in terms of the parasitic losses. Also, it is important to highlight that this model does not include the switching losses.

To plot the efficiency as a function of the losses and output power, P_o in (28) is rewritten as a function of V_{in}^2, which is assumed as the FC voltage at maximum power, in this case, 28.8 V as presented in Table 3. Assuming the same simplifications to obtain (22) and (25), the output power results in (29)

$$\eta = \frac{P_o}{P_i} = \frac{(V_C^2/R_o)}{V_{in}I_{fc}} = \frac{\left((m_{IBVM}^2 V_{in}^2)/R_o\right)}{V_{in}I_{fc}} = \frac{m_{IBVM}^2}{R_o y_{IBVM}}, \tag{26}$$

$$\eta = \frac{2R_o(k-1)^2}{2R_Ok^2 - (4R_o + 2r_C + r_S)k + 2(R_o + r_C) + 4r_L + 5r_S}. \tag{27}$$

Lastly, we plot the efficiency as a function of the losses and the output power. In Figs. 8*a–c*, a similar behaviour can be observed, i.e. we have an enhancement of the efficiency when the losses (r_L, r_S and r_C) are reduced, as expected.

$$P_o = \frac{V_C^2}{R_o} = \frac{((V_C/V_{in})V_{in})^2}{R_o} = \frac{m_{IBVM}^2}{R_o} V_{in}^2, \tag{28}$$

$$P_o = \frac{16R_O^3(k-1)^2 V_{in\_ref}^2}{\left[2R_O^2k^2 - kR_O(4R_O + 2r_C + r_S) + R_O(2R_O + 2r_C + 4r_L + 5r_S)\right]^2} \tag{29}$$

The impact of (r_L and r_S) is 28% superior than the resistance (r_C), i.e. the efficiency goes down by 70% for high values of r_L and r_S (0.5 Ω), while the coupling capacitance resistance (r_C) decrements the efficiency at most 90%, as well.

Finally, in Fig. 8*d* we show the theoretical efficiency calculated according to (27) and the efficiency obtained experimentally. The equivalent error between the plots is reasonably small to validate the proposed model.

6 Conclusion

In this study, we presented the complete mathematical model in steady-state and small-signals of then IBVM converter. With the model, it is possible to analyse the different control structures in terms of stability and performance.

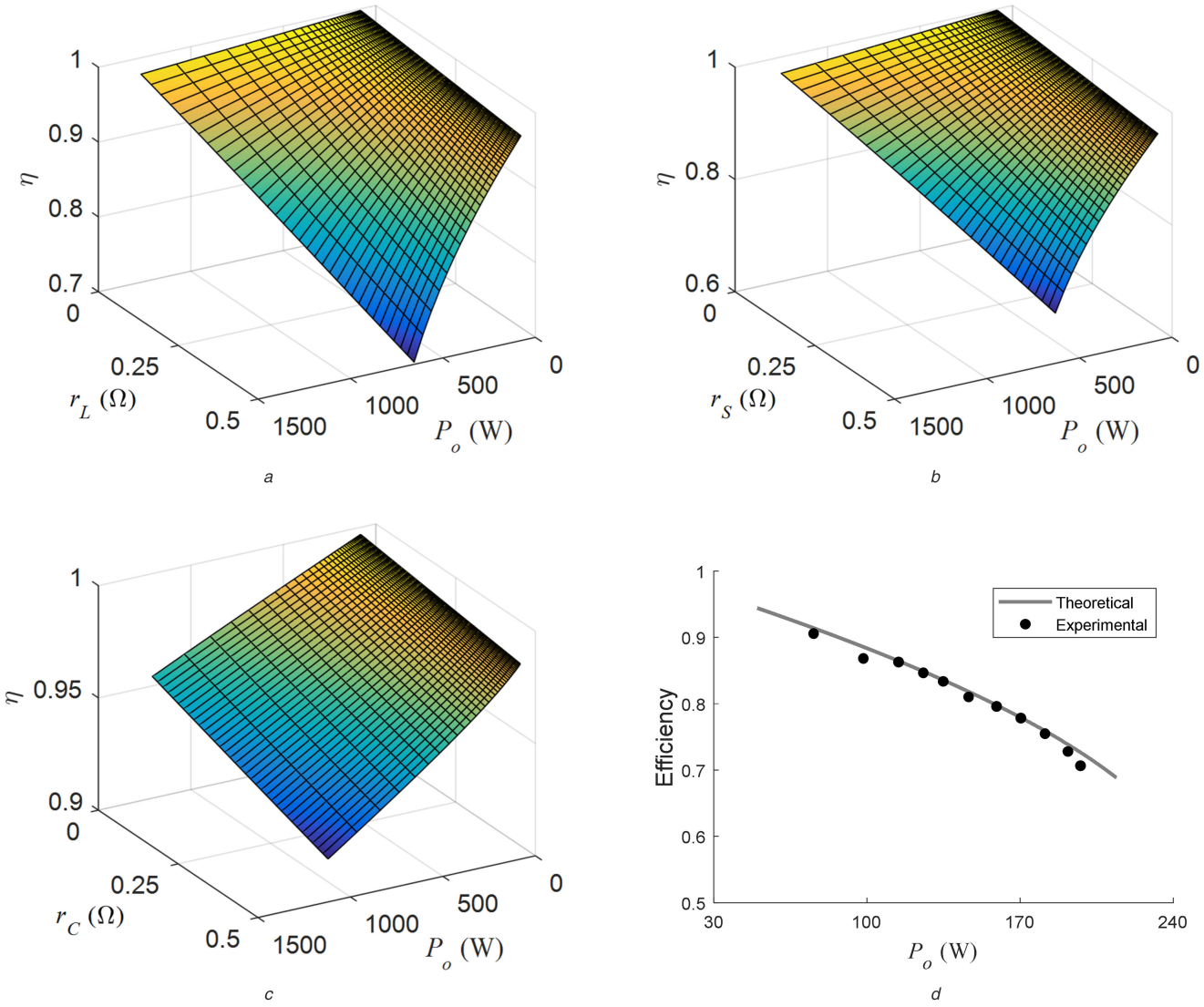


Fig. 8 *IBVM efficiency analysis*

(a) Efficiency as a function of the output power and the losses of the IBVM inductance, ***(b)*** Efficiency as a function of the output power and the losses of the IBVM transistors, ***(c)*** Efficiency as a function of the output power and the losses of the IBVM double cell capacitance, ***(d)*** Theoretical and experimental efficiency versus output power

In addition, we built a test bed composed of an IBVM and a VSI with different control structures to evaluate the effects of the ac-side on the dc-side. The tests performed take into account the grid-connected operation for the both proposed modes. Additionally, the results showed a significant difference in terms of performance between the two control modes. The control mode 2 (controlling the FC operating point) exhibited smaller oscillations in the dc-link voltage and in the FC current when compared with control mode 1.

Regarding the efficiency analysis, we also realise that the losses of the semiconductors and inductors are much more impacting in terms of efficiency than the capacitor's losses. Finally, we plot the theoretical and experimental efficiency to prove the effectiveness of the method developed in Section 5.

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