Tunnel-FET Evolution and Applications for Analog Circuits

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***Abstract*— In this work different generations of field effect tunneling transistor (TFET) are evaluated through DC digital and analog figures of merits. For TFET devices the main digital figure of merit is the subthreshold slope (SS), while for analog application the intrinsic voltage gain (A_V) is the most important one. For the early generations, that are based on silicon, the SS does not reach values smaller than 60mV/dec at room temperature, however, the A_V reaches values up to 80 dB, showing to be promising for analog applications. As the TFETs were being optimized for digital applications and consequently presenting better switching performance, the intrinsic voltage gain moves in the opposite direction. This opposite trend is related to which transport mechanism is predominant for each type of device. While III-V TFETs are more dependent on Band to Band Tunneling (BTBT), silicon devices are more relying on Trap-Assisted Tunneling (TAT). While BTBT allows for faster switching, TAT is less dependent on the drain electric field, so the former favors SS while the latter favors A_V. Based on the good analog behavior of silicon channel TFETs, a two-stage operational transconductance amplifier (OTA) was designed with different TFET technologies and the compared results were discussed.**

***Index Terms*— TFET; geometries; new materials; digital and analog performance.**

I. Introduction

Over the last few decades, the technological evolution was based on the dimensions reduction of metal–oxide–semiconductor field-effect transistors (MOSFETs). The evolution of fabrication processes, geometries and the use of different materials enable the enhancement of switching speed, integration scale and consequently the functionality of electronics. However, to keep the search for better performances, the semiconductor industry highlights the importance of lower power consumption, which is one of the major concerns.

Aiming to minimize the power consumption, it is required to reduce the supply voltage and consequently the threshold voltage, without degrading the leakage current. However, CMOS technology comes up against the physical limit of thermally injected charge carriers over a barrier, which in turn limits the subthreshold slope (SS) to a minimum value of 60 mV/decade at room temperature [1]. In this scenario the tunneling field effect transistor (TFET) appears as an alternative to the CMOS technology, since the TFET operation principle is based on a gate controlling the band-to-band tunneling (BTBT), making it possible to overcome 60 mV/dec [2, 3].

The physical limit of the subthreshold slope of CMOS technology causes a strong increase in off-state current (I_{OFF}) when the threshold voltage is reduced increasing the power consumption through the static component. The solution proposed by TFET design is to use a device with a steeper subthreshold slope making it possible to reduce the threshold voltage without increasing I_{OFF} [2, 4 ,5]. This solution is illustrated in figure 1.

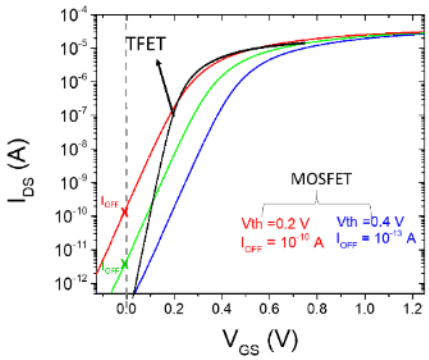

Fig.1 Schematic transfer curve, for MOSFET and TFET technologies.

Although the TFET concept allows an enhancement of transistor switching, some disadvantages have been pointed out for transistors based on silicon such as the low on-state current (I_{ON}) and the non-ideal SS measured on experimental transistors.

In order to improve the real behavior of TFET transistors, improving I_{ON} and SS, new researches were developed using different materials with lower bandgap, such as Si_XGe_{1-X} alloys [5-8] and III-V materials [9] and implementing different geometries [10-12].

Although TFETs were developed with a main focus on switching speed and digital applications, several researches have shown that this type of transistors also have a great potential for analog applications [8, 11-13].

In this paper, the transport mechanism (Section II), different structures and their behavior (Section III) and TFET application in a basic analog block of integrated circuits (Section IV) will be discussed.

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II. TFET Transport Mechanism

Tunneling transistors have a p-i-n diode structure with the intrinsic region covered by the gate. Its structure is similar to MOSFET transistors, the only change is the type of source dopant.

The presence of the gate structure modulates the potential of the channel region (intrinsic) controlling the transistor operation. Assuming a nTFET transistor (shown schematically in Figure 2), as the gate voltage becomes more positive, there is a greater bending of the energy bands, until the valence band of the source presents a greater potential energy than the conduction band of the channel, allowing the injection of carriers by the tunneling mechanism between bands. This band bending allowing the tunneling current is presented in figure 3.

For low gate bias (V_{GS}) two other transport mechanisms also take place in the TFET operation. The generation by Shockley-Read-Hall recombination (SRH), where carriers cross the bandgap through an intermediate energy state also called trap, and Trap-Assisted-Tunneling (TAT) mechanism where the same mechanism as SRH is observed but it is enriched by the gate electric field.

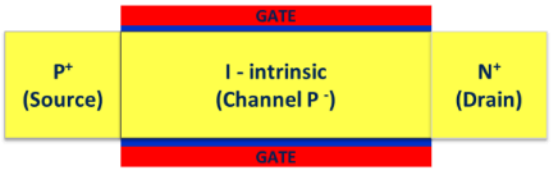

Fig.2 Schematic illustration of a TFET structure.

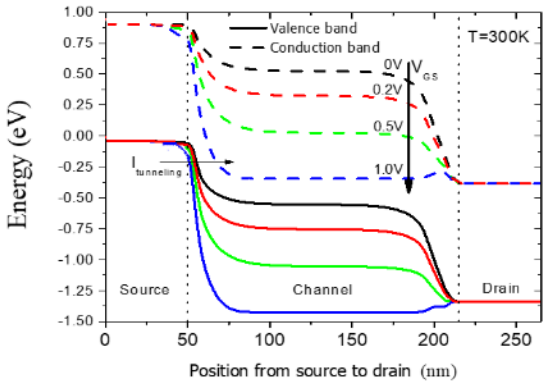

Fig.3 Energy band diagram illustrating the band-to-band tunneling mechanism.

The current composition of TFETs is shown in figure 4. For low V_{GS}, the active transport mechanism is the SRH. By increasing the voltage applied to the gate this mechanism is enriched, activating the TAT and for gate voltages where there are overlapping bands BTBT is activated. It is worth noting that when BTBT is activated the trap-assisted tunneling mechanisms remain active, only the current from BTBT grows exponentially, becoming the predominant one. The schematic TFET current is divided in 4 regions (A, B, C and D) in figure 4, where for each region is presented which transport mechanism is dominant.

It is important to say that in the case of self-aligned nTFETs, when the gate voltage becomes quite negative, the band bending occurs at the drain/channel junction, also enabling tunneling between bands and creating an undesirable current called ambipolar current [14-16].

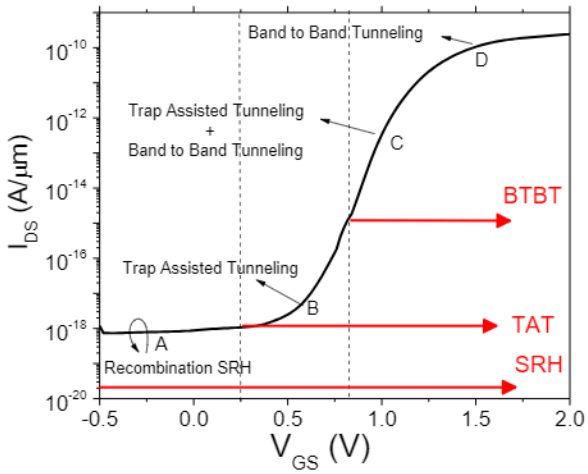

Fig.4 Schematic composition of the tunneling current illustrating the activation of each transport mechanism.

Figure 5 presents the drain current as a function of the gate voltage for a double gate nTFET reported in [15]. It is possible to notice that for the self-aligned transistor (black curve) there is a high off current that degrades the transistor performance while the ambipolar current is strongly reduced by increasing the gate to drain underlap. Besides the off-state current improvement, an increase of the underlap region also enhances the transistor switch, i.e., reduces the minimum subthreshold slope (SS).

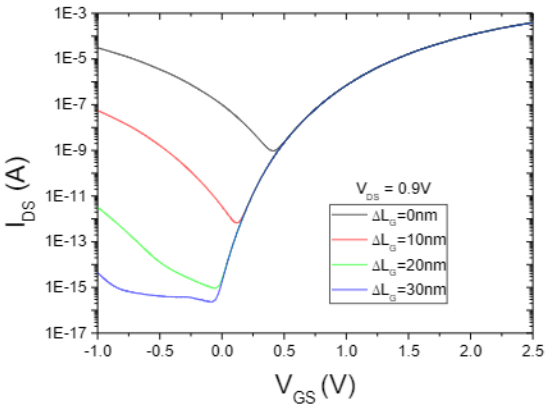

Fig.5 Simulated drain current curves as a function of gate voltage for a double gate nTFET with different gate-to-drain underlap dimensions.

III. TFET Evolution and Electrical Parameters

For TFETs to be a real alternative for digital application, it is necessary to achieve a steep subthreshold slope to ensure that when the onset voltage is reduced, the off-state current remains small. Furthermore, it is necessary to maximize the on-state current to guarantee a high I_{ON}/I_{OFF} ratio.

With this objective, several geometries with different source materials were studied. All devices were fabricated at imec in Belgium.

Initially, the triple gate TFET transistor was manufactured with the same structure as a standard FinFET [17], only changing the type of the source doping. Figure 6A shows the triple gate TFET structure.

To further enhance the channel control a gate all around TFET was fabricated in a silicon nanowire construction with different source materials as is shown in Figure 6B.

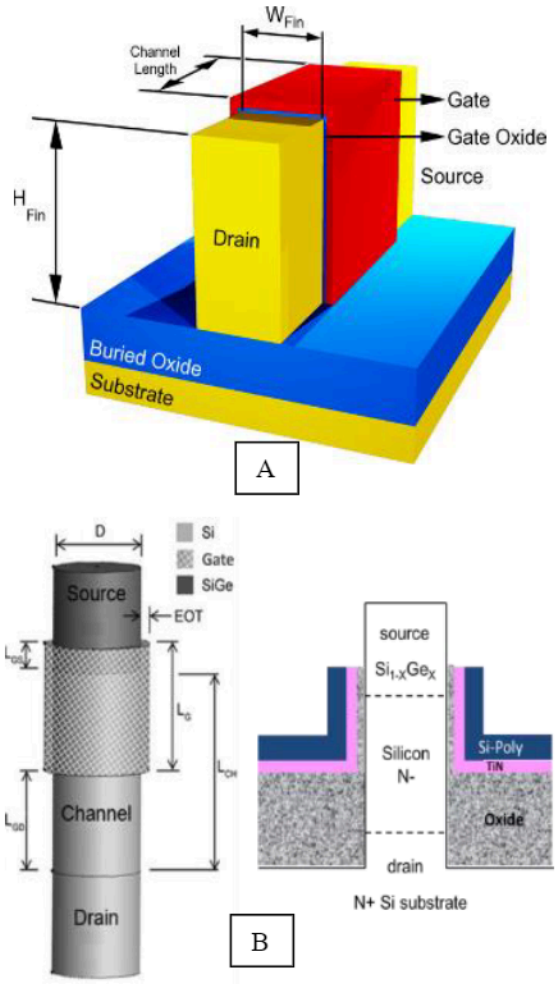

Fig.6 Multiple gate TFET structures with silicon channel: (A) Triple gate TFET (Tunel-FinFET) [11] and (B) silicon nanowire TFET (NW-TFET) [8] with a Si_XGe_{1-X} source.

Considering only silicon TFETs, it is possible to see that for both geometries the TFET technology presents an on-state current much lower than the one for MOSFET. However, the off-state current is in the same order of magnitude for triple-gate TFETs and for NW-TFETs, I_{OFF} is one order of magnitude smaller than for NW-MOSFET (Figure 7) due to the gate-to-drain underlap that reduces the ambipolar current.

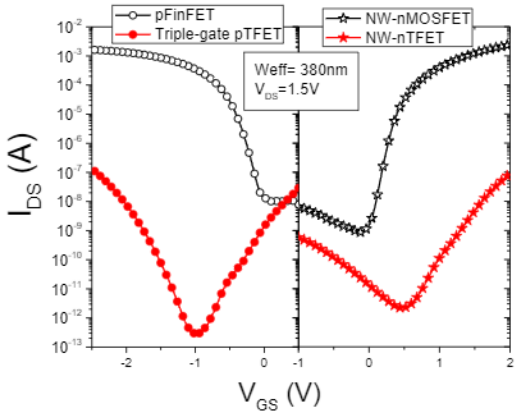

Fig. 7 Drain current as a function of gate voltage for MOSFET and TFET for Si-homo-junction devices [18]. I_{DS} for triple gate structures are presented in left graph while for Si nanowire structures they are shown in the right part.

Since the NW-TFETs presented a similar behavior in the on-state as the triple gate transistors, but the ambipolar current was reduced by the underlap insertion, these structures were again modified, now thinking about maximizing the on-state current. The new nanowire structures have different source compositions: only silicon, a SiGe alloy and 100% Ge. Figure 8 presents the drain current as a function of gate voltage for NW-TFETs with 4 different source compositions.

It is possible to notice that increasing the germanium amount in the source, the on-state current increases due to the smaller bandgap which increases the tunneling probability, but I_{OFF} decreases 1 order of magnitude when compared with Si source and the ambipolar current is reduced. This behavior results in a better I_{ON}/I_{OFF} ratio and smaller subthreshold slope, which better resembles the initial proposition for TFETs.

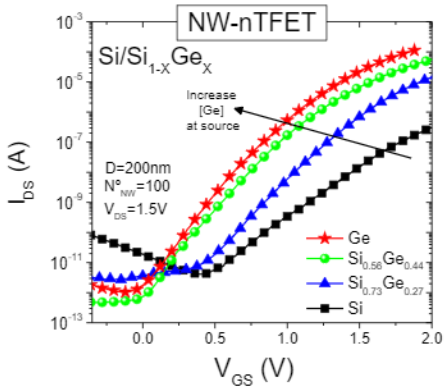

Fig.8 Nanowire TFET structures with different source compositions. The germanium amount at the source varies from 0% to 100% [19].

Despite of the increase of almost 2 orders of magnitude in the on-state current, the subthreshold slope still presents high values due to the great influence of TAT. A new structure was proposed aiming to increase the predominance of

BTBT and consequently minimizing SS. This new structure is the transistor where the tunneling occurs aligned with the perpendicular electric field and is called Line-TFET.

Line nTFETs are fabricated on silicon on insulator wafers with a $Si_{0.55}Ge_{0.45}$ p type source covered with a thin pocket layer of intrinsic silicon. The gate is only positioned above the source region while the intrinsic Si channel is self-aligned towards the gate and separates the source from the drain. It is important to mention that the gate does not cover this Si channel region which acts as gate-to-drain underlap. The Line-TFET structure is presented in figure 9 [20].

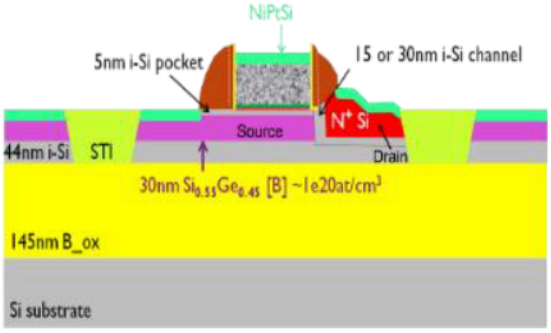

Fig. 9 Schematic structure of a Line-TFET [20].

Evaluating the transfer curves presented in Figure 10, it is possible to notice that with only one device it is possible to reach currents in the order of microamperes. This isdue to the enrichment of BTBT that takes place in the pocket region that is just below the gate and above the source. It is also possible to observe that with the reduction of drain voltage, a region with steeper subthreshold slope appears than those presented by the previous geometries.

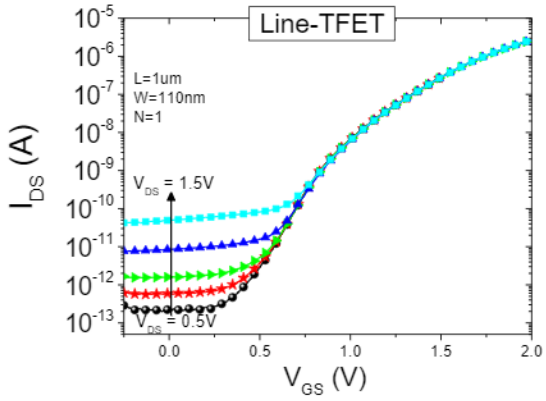

Fig. 10 Drain current as a function of gate voltage for Line-TFET with drain bias ranging from 0.5V to 1.5V [19].

Since the TFETs with a silicon channel, independent on source composition (Si, SiGe or Ge) do not overcome SS of 60mV/dec at room temperature, a new device fabricated with III-V materials was proposed. Figure 11 shows the proposed planar III-V TFET.

It is known that materials such as In(Ga)As have a high tunneling generation rate due to smaller bandgap [22], and as reported in [9, 23] a homojunction TFET with $In_{0.70}Ga_{0.30}As$ reaches sub-60mV/dec SS.

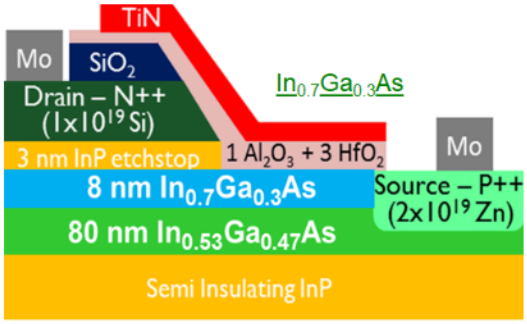

Fig. 11 Schematic Structure of a planar III-V TFET [21].

This III-V TFET technology was evaluated with different source doping processes [21] as well as different thicknesses of the HfO_2 gate dielectric [24]. The EOT reduction, from 3 to 2 nm of HfO_2, reported in [21], causes an I_{ON} enhancement due to the better electrostatic control as expected, while devices with a different doping source process (Spin-on-glass versus Gas Phase) present a strong variation in source/channel junction abruptness, that in turns modify the BTBT rate. The higher abruptness obtained for a transistor with a gas phase doping process results in a higher I_{ON} and better SS than for the transistor with a spin-on-glass doping process, as can be seen in figure 12.

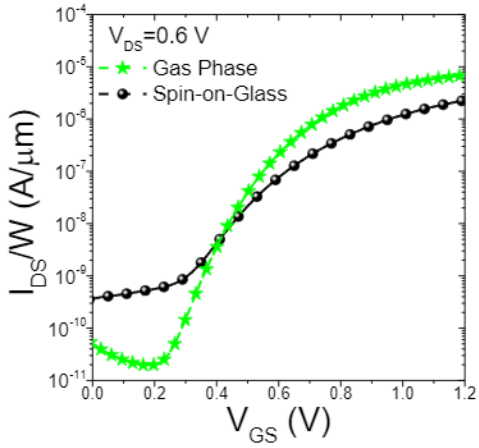

Fig. 12 III-V TFET experimental normalized transference curve for 2 different doping source processes.

Although TFETs do not have the theoretical limitation of 60mV/dec like transistors that operate by drift/diffusion mechanisms, there are 3 transport mechanisms that add up to compose the drain current. Transistors that rely heavily on trap-assisted tunneling have very high SS values, as in the case of homojunction silicon TFETs that have SS >150mV/dec.

However, with the optimization of the structure, either by the smaller bandgap, by the tunneling aligned with the electric field, by the abruptness of source/channel junctions or by the combination of the mentioned effects, the band-to-band generation rate is enriched making that the BTBT mechanism becomes increasingly dominant in the composition of the currents. The lower the dependence on TAT and

higher on BTBT, the higher the on-state current and the lower the SS value, surpassing the theoretical limit of MOSFETs as observed for III-V TFETs.

Figure 13 presents the experimental subthreshold slope values for studied TFETs and for the multiple gate MOSFETs. It is possible to notice that the MOSFET technologies (FinFET and NW) have a great electrostatic coupling reaching its theoretical limit for SS. When the SS values are compared with TFET technology, the silicon structures have very high values (SS > 150mV/dec), decreasing for SiGe source devices and reachingSS values smaller than 60 mV/dec for III-V TFETs.

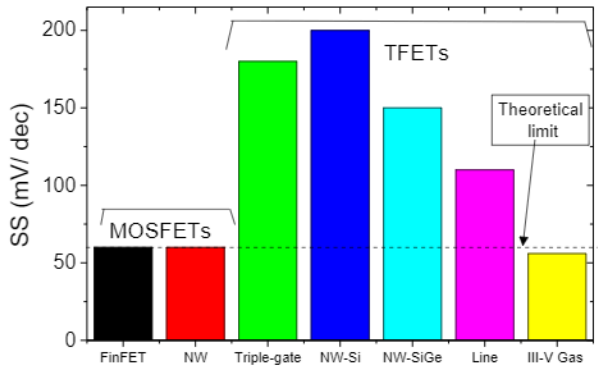

Fig. 13 Experimental SS values for all TFET structures and for FinFET and NW-MOSFET.

Although the evolution of structures has always been conceived with digital characteristics in mind, when the focus turns to analog applications, an opposite trend is observed. Taking the intrinsic voltage gain as a reference, which is one of the most important figures of merit for analog, we can see in figure 14, a reduction of the A_V with the evolution of TFET structures.

From figure 14 it is also possible to observe that even with the reduction of the intrinsic voltage gain (A_V) of the TFETs, the worst value obtained among the TFETs is at least 20 dB above the best value obtained for MOSFETs.

This behavior can be explained because the tunneling mechanisms are less dependent on the drain voltage than the drift mechanisms of MOSFETs.

When comparing A_V values among the tunneling transistors, the difference obtained can also be explained by the dependence of TAT and BTBT on the drain electric field. The trap-assisted tunneling mechanism is strongly dependent on the gate electric field, but it is almost independent of the drain voltage (V_{DS}) [24]. For a BTBT mechanism there is a small dependence with V_{DS}, which is higher than TAT but smaller than for a drift mechanism.

With the evolution of TFETs the improvement of I_{ON} results in a higher transconductance, but it is not enough to compensate the output conductance degradation caused by the V_{DS} influence on the current due to BTBT dominance.

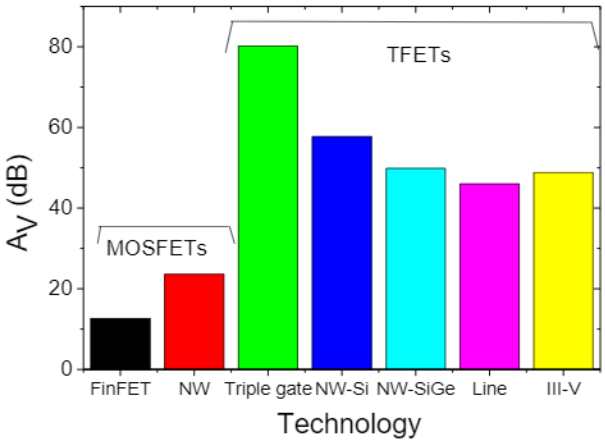

Fig. 14 Experimental A_V values for all TFET structures and for FinFET and NW-MOSFET.

Figure 15 presents the same A_V analysis for both TFET and MOSFET technologies but now as a function of temperature.

When the analog potential is evaluated for different temperatures, the analog response depends on the prevailing transport mechanism. Increasing the temperature in a small range (from 25°C to 150°C) a slightly reduction was observed for all TFETs, but for Si TFETs the A_V reduction is a little bit higher than for TFETs where the BTBT has a greater influence on the behavior due to the gm degradation caused by TAT that is thermally activated. It is worth to observe that for all TFETs in the analyzed temperature range, TFETs present higher Av than MOSFETs.

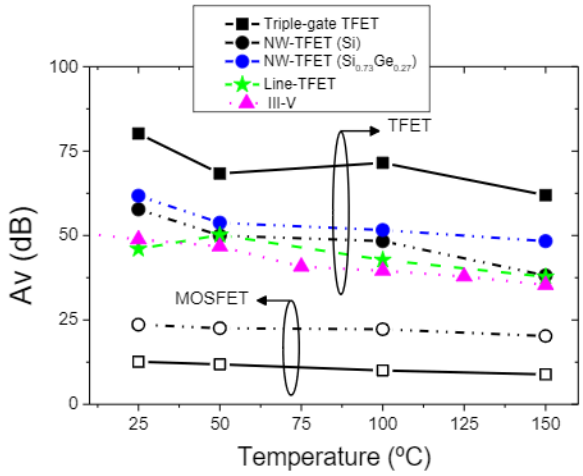

Fig. 15. Intrinsic voltage gain as a function of temperature for different TFET and MOSFET technologies.

IV. OTA Designed with TFETs

Since the TFETs present an excellent analog behavior, it is important to know how the TFET behaves at circuit level. Considering that the operational transconductance amplifier (OTA) is one the most common analog block in integrated circuits and also considering that the TFETs with silicon

channel presented good analog behavior, a two-stage OTA (figure 16) was designed with triple-gate TFETs, NW-TFETs and Line-TFETs.

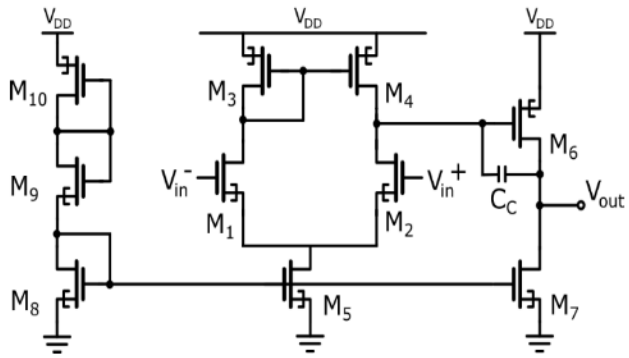

Fig. 16 Schematic OTA topology with two stages designed with p-type and n-type TFET devices.

The OTA simulation was performed with Cadence Virtuoso and ADE tools using the experimental TFET data. The TFETs were modeled with Verilog-A using the LookUp Table method (LUT).

In order to create the LUT, a very accurate set of measurements was performed using the Signatone microprobes and the Semiconductor Parameter Analyzer (B1500) from Keysight. The measurements were performed with the gate voltage swept from 0.5 V to -2 V for pTFETs and -0.5 V to 2 V for nTFETs. In pTFET cases the V_{DS} range was from -0.1V to -1.5V with steps of 50mV. For nTFET the absolute values were used.

For each type of TFET technology one LUT was created.

The main OTA simulation results are summarized in Table I, where 5 different OTA designs are compared, each one with a different device (4 TFETs and 1 MOSFET).

Table I. Two-Stage OTA results designed with different generations of TFET devices [25,26,27,28]

Two-Stage OTA parameters					
	Si NW-MOSFET	Triple gate TFET	Si NW-TFET	SiGe-source NW-TFET	Line-TFET
Power	120 µW	18.9 nW	280 nW	7.5 µW	3.2 µW
Cc	600 fF	--	--	--	25 fF
A_V	51 dB	130 dB	98 dB	90 dB	110 dB
GBW	9.2 MHz	100 Hz	41 kHz	900 kHz	5.5 MHz

Considering that the power consumption is one of the main challenges for the future of integrated circuits, homojunction silicon TFETs present a very low power dissipation. While for MOSFET the power consumption is 120 µW, for silicon TFETs it is about 4 orders of magnitude smaller for triple-gate TFET and 3 orders of magnitude smaller for NW-TFET due to the low drain current. Even for circuits designed with heterojunction (SiGe source) TFET the power dissipation is about 100 times smaller than for MOSFETs.

When the focus is the total voltage gain, all TFETs presents higher values of Av than the MOSFET one. A special attention should be given to triple-gate TFETs and Line-TFETs that reach values higher than 100 dB. However, TFET devices present good performance for low and medium frequencies. The only one TFET that reaches the MHz scale as for MOSFETs, is the Line-TFET. It is also worth to highlight that OTAs designed with triple gate TFETs and NW-TFETS do not need a compensation capacitor between first and second stage to obtain the stability.

V. Conclusions

In this work, the evolution of the TFET devices was presented. From the digital point of view the focus was the improvement of the on-state current without degrading the I_{OFF}, allowing a good I_{ON}/I_{OFF} ratio and a reduction in the SS values, showing a greater switching ability. This work started with the triple gate TFETs built in silicon which proved to be very dependent on the trap-assisted tunneling mechanism, resulting in an unwanted digital behavior. A very similar response was also obtained for the Si-NW-TFETs excepted for a small improvement in the ambipolar current caused by the gate-to-drain underlap.

In addition to the multiple gate geometry, NW-TFETs were manufactured with source/channel heterojunctions that allowed to increase I_{ON} and improved SS thanks to the reduction of the bandgap and the enrichment of the BTBT current. Although I_{ON} increases almost 2 orders of magnitude when comparing TFET with a germanium source in relation to one with a silicon source, the SS still does not reach reasonable values, due to the great influence of the trap-assisted tunneling mechanism.

Considering as source material a silicon/germanium alloy, another way that was found to enrich the tunneling between bands was an alignment between the tunneling mechanism and the electric field lines. This was the Line-TFET proposal that allowed to improve the switching even more, mainly for lower drain voltages.

Only the planar tunneling transistors made of III-V material, due to their lower bandgap, overcome the SS of 60mV/dec, proving to be more promising for digital applications than all their predecessors.

However, comparing the individual performance of tunneling transistors with 4 different geometries, it was shown that the digital TFET evolution is not necessarily an evolution when the focus is on analog circuits. A degradation in intrinsic voltage gain was observed for devices that are strongly dependent on BTBT and weakly dependent on TAT, showing an opposite trend between analog and digital development for TFETs.

A two-stage OTA circuit was designed with 4 different TFETs and a comparison was made between the OTA TFET performance and with MOSFET technology. TFET shows its superiority for low and medium frequency applications.

Another advantage of Silicon TFETs is that they are totally compatible with a CMOS fabrication process and hybrid projects can be proposed.

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