PAPER

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Onchip digital calibrated 2 mW 12-bit 25 MS/s SAR ADC with reduced input capacitance

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Abstract: We present a 12-bits asynchronous SAR ADC with a low complexity digital on-chip calibration and just 2 pF of total array capacitance. The ADC architecture utilizes a redundant weighting switching of 2 fF MOM capacitors consuming 14 clock-cycles to complete the conversion. Taking advantage of redundancy, the weights of the MSB capacitors are estimated using the LSB array, thus it is possible to digitally compensate for the mismatch non-linearity directly over the ADC output. The circuit consumes 2 mW at 25 MS/s on a core area of 300 µm × 500 µm in 180 nm CMOS technology. ENOB improvements of 0.85 bits were post-layout simulated after calibration. Sample characterization is ongoing.

Keywords: Analogue electronic circuits; CMOS readout of gaseous detectors; Front-end electronics for detector readout; VLSI circuits

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1 Introduction

The growing HEP experimental needs are pushing for improved acquisition systems where ADCs with increased resolution are desired, going even beyond 12 bits, with sampling frequencies in the order of tens of MHz. Small area and low power consumption are critical specifications since many channels in a single integrated circuit are a trend in HEP detectors. Successive Approximation Register (SAR) has been shown in the last decade to be an adequate architecture to reach these specifications, but for resolutions greater than 10 bits the mismatch in the capacitors array limits the effective resolution. The use for special techniques for the capacitor array layout and the increase of the unit capacitor are strategies often employed by the designer to reduce the mismatch, but this generally leads to an excessive increase in power and area consumption. Mismatch calibration is a better solution for high-resolution SAR ADC, then chip-by-chip calibration is not necessary, which will reduce the testing costs. Calibration techniques with bearable complexity and small area performed during the system startup, without external components or signals, is an attractive strategy for the new generation of ASICs for HEP. Mismatch compensation allows us to reduce the array capacitor unit close to the limit imposed by kT/C noise and thereby leading to considerable energy and area reduction. Minimizing the total capacitance of the SAR ADC will relax the settling requirement of the voltage reference buffer and the input signal driver (analog front-end output), which are commonly power-hungry blocks. In multi-channel ASIC where many ADC instances are integrated in a single chip, many bond-pads and large decoupling capacitance are required for the voltage reference due to the settling error generated by the bondwire inductance during the bit cycling phase. This effect becomes really critical as the sampling frequency increases. Redundant weighting is a simple way to avoid the conversion errors generated by this, with the cost of consuming more clock cycles to complete the conversion. This work presents the design of a

12-bits 25 MS/s asynchronous SAR ADC with redundant weighting switching of MOM capacitors and on-chip calaibration in 180 nm CMOS technology.

2 SAR ADC architecture

Figure 1 shows the simplified schematic of the 12-bit SAR ADC proposed in this work. To relax the reference voltage settling time requirement, the binary-scaled recombination capacitor weighting method proposed in [1] with 2 bits of redundancy was used. The advantage of this binary-scaled capacitor weight redistribution is that it reduces the complexity of digital output decoding from 14 bit to 12 bit. To reduce the DAC total capacitance, the adopted strategies were: (1) a monotonic switching [2] was used, which reduces the total capacitance by a factor of 2; (2) the reference voltage of the LSB capacitor is $V_{\mathrm{REF}}/2$ defined by a resistors divider ($R_1 = R_2 = 1\ \mathrm{k}\Omega$), which also reduces the capacitance by a factor two; (3) MOM capacitors of 2 fF were utilized as the DAC unit capacitor instead of MIM, because in the 180 nm CMOS technology the minimum MIM capacitor is 24 fF. The mismatch of the MOM capacitor was estimated to be $\sigma = 5.5\%$ [3]. The proposed on-chip calibration is based on the technique presented in [4], in which the weights of the MSB capacitors can be extracted using the LSB array taking advantage of redundancy. It is possible to digitally compensate for the mismatch non-linearity directly over the ADC output. To perform this technique, the DAC was split into LSB array (C_0–C_8) and MSB array (C_9–C_{13}). This distribution was estimated from the requirement that the $3\sigma_{\mathrm{DNL}}$ due to the mismatch of the resistor voltage divider and the MOM unit capacitor must be less than 1 LSB, such that the LSB DAC is linear enough to have an adequate estimation of the real weight of every MSB capacitors.

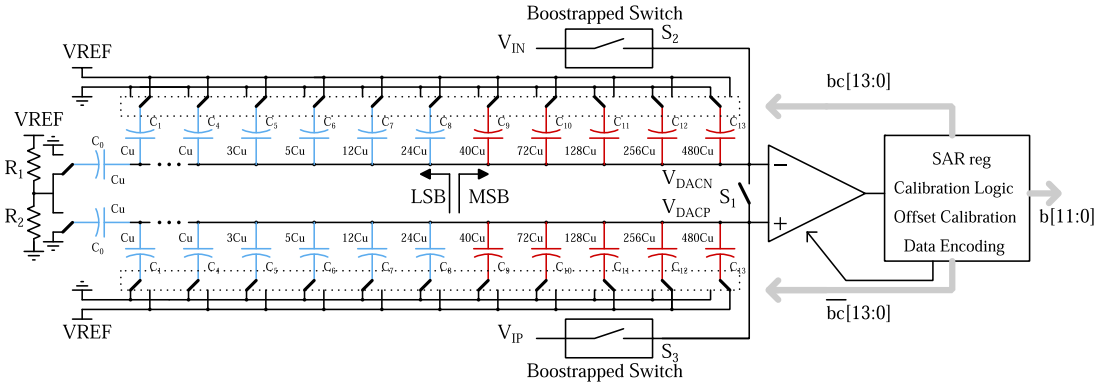

Figure 1. Schematic of the proposed SAR ADC architecture.

3 Offset calibration of the comparator

The technique to determine the real weight of the MSB capacitors assumes that the bits weight sum of the LSB capacitors (C_0 to C_{i-1}) is greater than the of the MSB capacitor weight (C_i) to be extracted, which is true because of the capacitive array redundancy. However, this requirement may not be met due to the comparator offset. Therefore, the comparator offset must be reduced below 1 LSB before beginning the extraction procedure of the MSB capacitors weights.

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The schematic of the dynamic comparator used in this work is presented in figure 2(a), basically composed of a preamplifier and a latch. The main offset sources of the comparator are the differential pair mismatch, the capacitance imbalance at the latch input, and the latch offset. The offset calibration scheme implemented in this work is based on the approach presented in [5], in which a digital controlled binary-weighted array of NMOS transistors as capacitors connected at the latch input allow the offset tuning. The offset value can be roughly reduced from 32 mV (3σ of the offset simulation) down to 1 mV by a 5-bit successive approximation algorithm. During the offset calibration procedure, the comparator inputs is kept at the same voltage and DC common mode such that $V_{GS} > V_{TH}$ for the differential pair transistors during the evaluation phase (CLK = high). The strategy used to generate a suitable common-mode voltage before starting the offset calibration is to initially sample the input signal on the top plate of the capacitor array through the bootstrapped switches S_2–S_3, and a clock cycle after S_1 is closed and S_2–S_3 are opened, generating a common-mode voltage approximately equal to the common-mode voltage of the input differential signal. During this procedure, the bottom plate of all capacitors in the array is connected to the ground. The time diagram of the offset calibration procedure is illustrated in figure 2(b). This strategy assumes that the signal at the ADC input is symmetrical with respect to the common-mode DC voltage (V_{CM}). The noise and offset at the ADC input do not interfere with the calibration procedure, since any voltage difference between the comparator inputs is eliminated when S_1 becomes on.

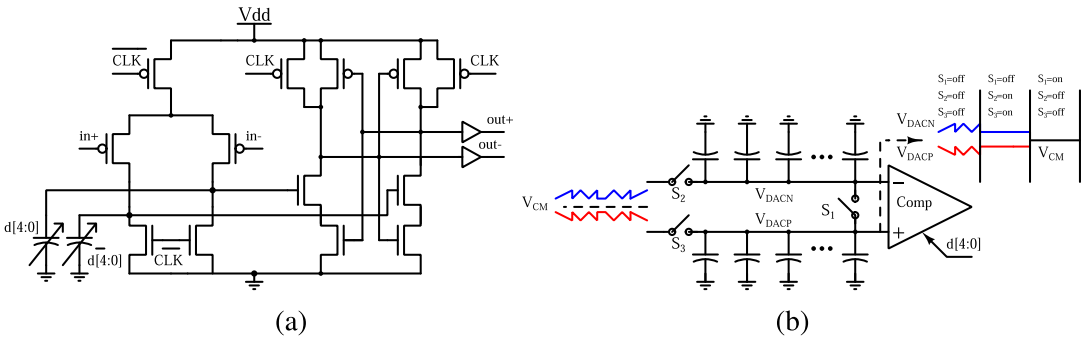

Figure 2. Offset calibration of the comparator: (a) schematic; (b) signal time diagram.

4 Real bit-weight extraction

To determine the real weight of any of the MSB capacitors (C_9 to C_{13}) in the proposed scheme, it is necessary first establishing a proper common mode on the bottom plate of the capacitors array. It is done performing by the same procedure of the offset calibration phase, i.e. the bootstrapped switches S_2–S_3 sample the input signal over the top plate of the capacitor array (step 1), and in the following clock cycle the S_1 switch is closed and S_2–S_3 are opened (step 2). However, now the bottom plates of the LSB capacitors (C_0 to C_{i-1}) of the positive and negative array are connected to V_{REF}, while the bottom plates of the MSB capacitors (C_i to C_{13}) are connected to ground.

After setting the common mode, at the next clock cycle the bottom plate of the positive array capacitor to be determined (C_i) is connected to V_{REF}, which sets a voltage difference across the top plate of the positive and negative array ($V_{DACN} - V_{DACP}$) equal to the real weight of the analyzed

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MSB capacitor (step 3). Figure 3 show a simplified diagram of the common mode definition and C_i capacitor weight sampling phases. Then the ADC performs a conversion and the 12-bit digital result is stored in a register (w_p). The same procedure is performed for the capacitor C_i of the negative array and the digital result of the conversion is stored in a register (w_n). Finally, the real bit weight representing the capacitor C_i is calculated to be $w_i = w_p - w_n$. The extracted weight of each bit of the MSB array is stored in a look-up table, to be used during the ADC output decoding.

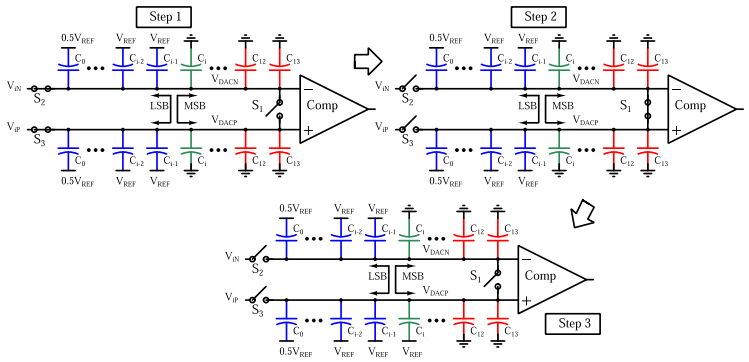

Figure 3. Common mode definition and C_i capacitor weight sampling.

5 Mismatch compensation

The compensation of the ADC nonlinearity generated by the capacitors mismatch involves three phases: (1) to calibrate the comparator offset; (2) to extract the real weight of each bit of the MSB array (C_i from C_9 to C_{13}) using the LSB array (C_0 to C_{i-1}), and store these in a look-up table; (3) after the weights extraction phase when the ADC operates normally, to decode the 12 bits ADC output from the weights defined in the look-up table. The error generated by the kT/C noise of the capacitive array over the weight extraction can be reduced by averaging the result of N weight extraction for every MSB bit [4]. However, this operation can take excessive time and becomes infeasible depending on the application. To minimize this error, without the need to perform N bit weight extraction, the total array capacitance was limited to 2 pF, which is equivalent to a kT/C noise of 45 µV (0.2 LSB). The ADC output is digitally calculated based on the following equation:

$$b_{\text{out}} = \sum_{i=0}^{13} w_i b[i]. \tag{5.1}$$

Where w_i is the extracted weight of each bit and b is the digital word resulting from the ADC conversion.

6 Simulations results

Figures 4(a) and (b) illustrate the layout of the designed ADC indicating the blocks distribution and the metal stack of the 2 fF proposed MOM capacitor, respectively. The total array capacitance is only 2 pF and the whole ADC consumes less than 2 mW on a core area of 300 µm × 500 µm. To determine the impact of the proposed onchip calibration technique on the ADC linearity, ENOB simulations were performed for 512 samples, 1 MHz input frequency, $V_{\text{REF}} = 1.8$ V, $2.7V_{pp}$ of

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input amplitude, and 25 MS/s of sampling frequency. For every simulation, random variations were introduced on the values of each DAC capacitor (σ = 5.5%), the relationship between the resistances R_1 and R_2 (σ = 0.25%), and the input differential pair dimensions (σ = 5%). The ENOB was simulated before and after the ADC calibration. Figure 4(c) presents the result of 10 simulations, showing an average improvement of 0.85 bits in the ENOB specification. Notice that increasing the number of MSB capacitors to be calibrated will improve this result, but lead to complexity increment of the digital part.

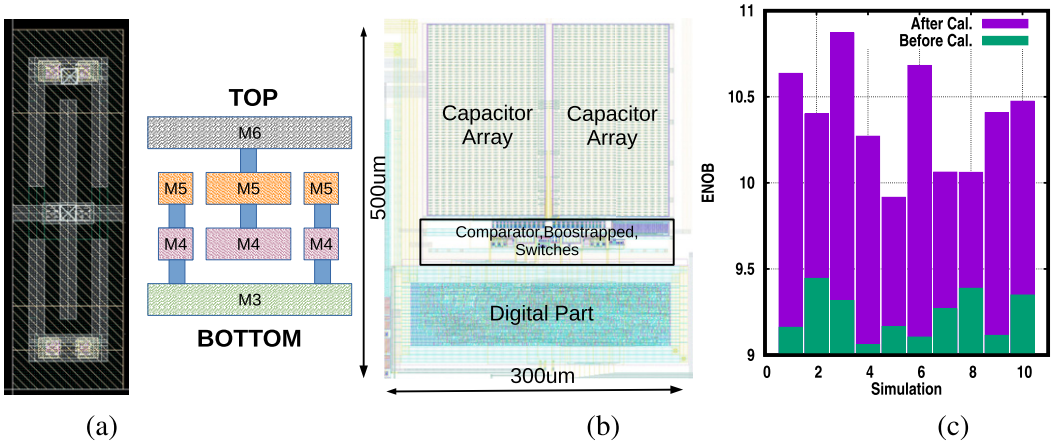

Figure 4. (a) MOM cap metal stack structure; (b) ADC layout; (c) ENOB simulation results.

7 Conclusions

This work presented a 12-bits asynchronous SAR ADC with on-chip digital calibration able to improve in 0.85 bits the ENOB specification. A binary-scaled recombination array of 2 fF MOM capacitors and 2 bits of redundancy was used in order to relax the settling requirement of the voltage reference. Taking advantage of redundancy, the weights of the DAC MSB capacitors are estimated using the LSB array, thus it is possible to digitally compensate the mismatch non-linearity over the ADC output. A core area of 300 µm × 500 µm in 180 nm CMOS technology and power consumption of 2 mW at 25 MS/s of sampling frequency were achieved.

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